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# TOO **HOT** TO TEST

Thermal Management  
of ICs During Testing

F E B R U A R Y 9 - 1 1 , 2 0 2 1 **O N L I N E**

# Too Hot To Test

February 9 - 11, 2021

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**ADVANTEST®**

# Our Best-Known Methods for the Testing of High-Power ICs

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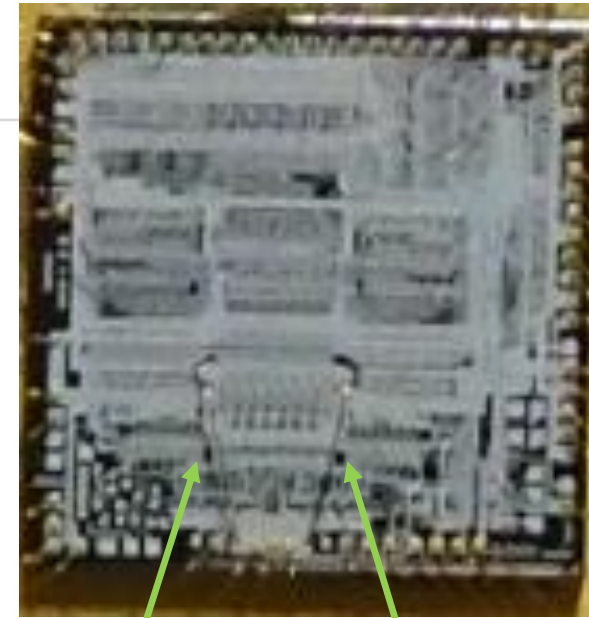
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# Who is Dave Armstrong?

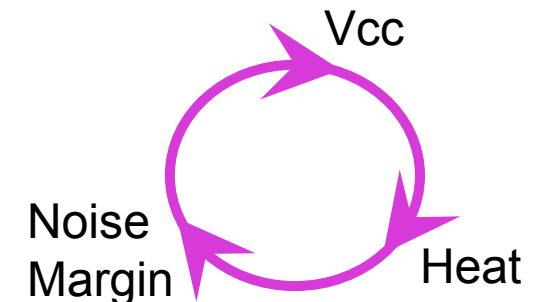


Electrical Engineering  
Computer Engineering  
Environmental Engineering



Center of die bonds

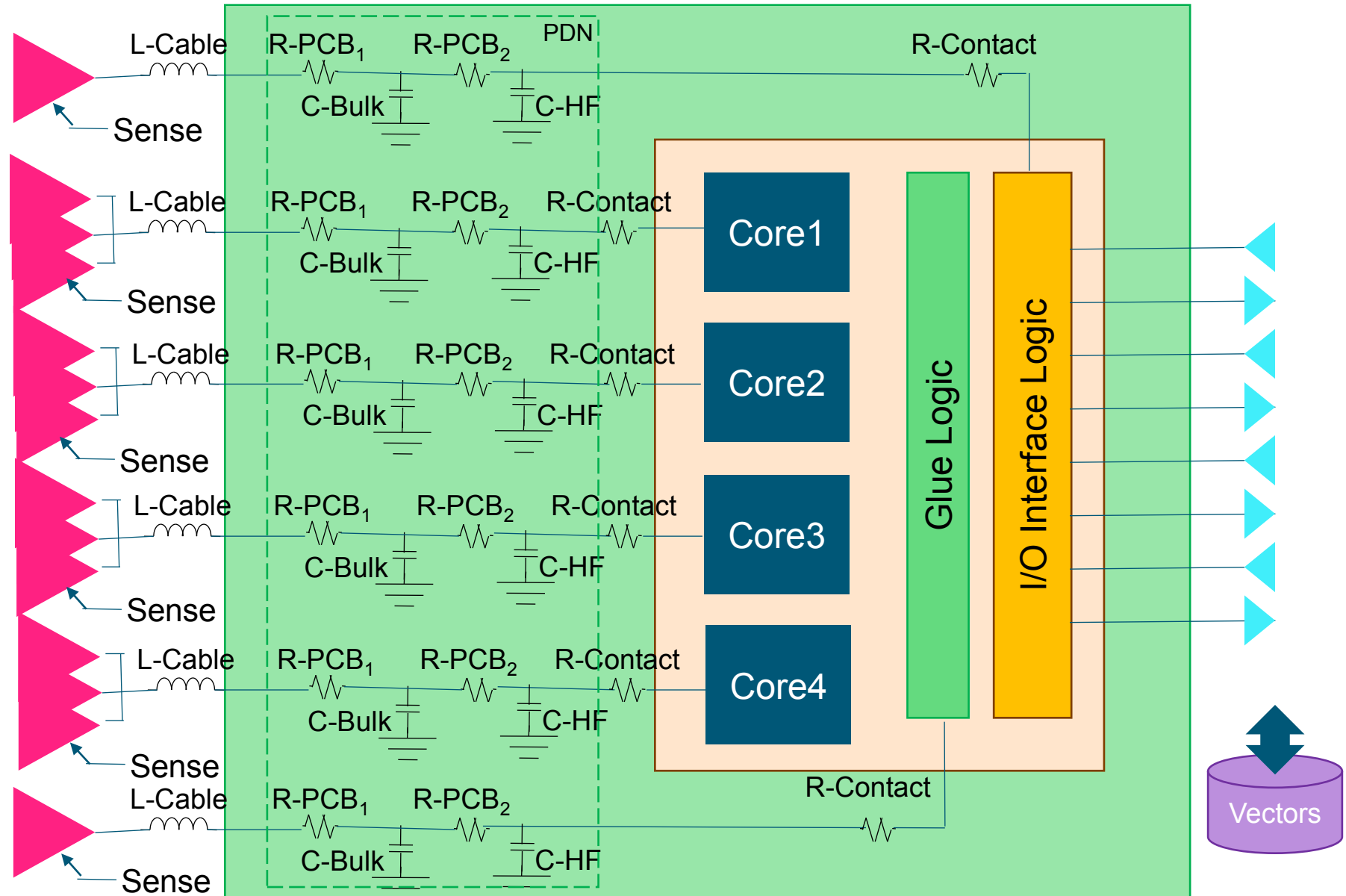
Reduced on-die V drops  
Improved noise margin  
Allowed Vee supply to reduce  
→ Allowed less cooling



# ADVANTEST®

# The Problem Statement

1. What power & cooling is really needed for my DUT.
2. How to configure an ATE to meet this need.
3. How to interconnect these power sources to my DUT.
4. How to control & bring up my supplies.
5. How to interface and control an Active Thermal Control system.
6. How to avoid burning up expensive probes.

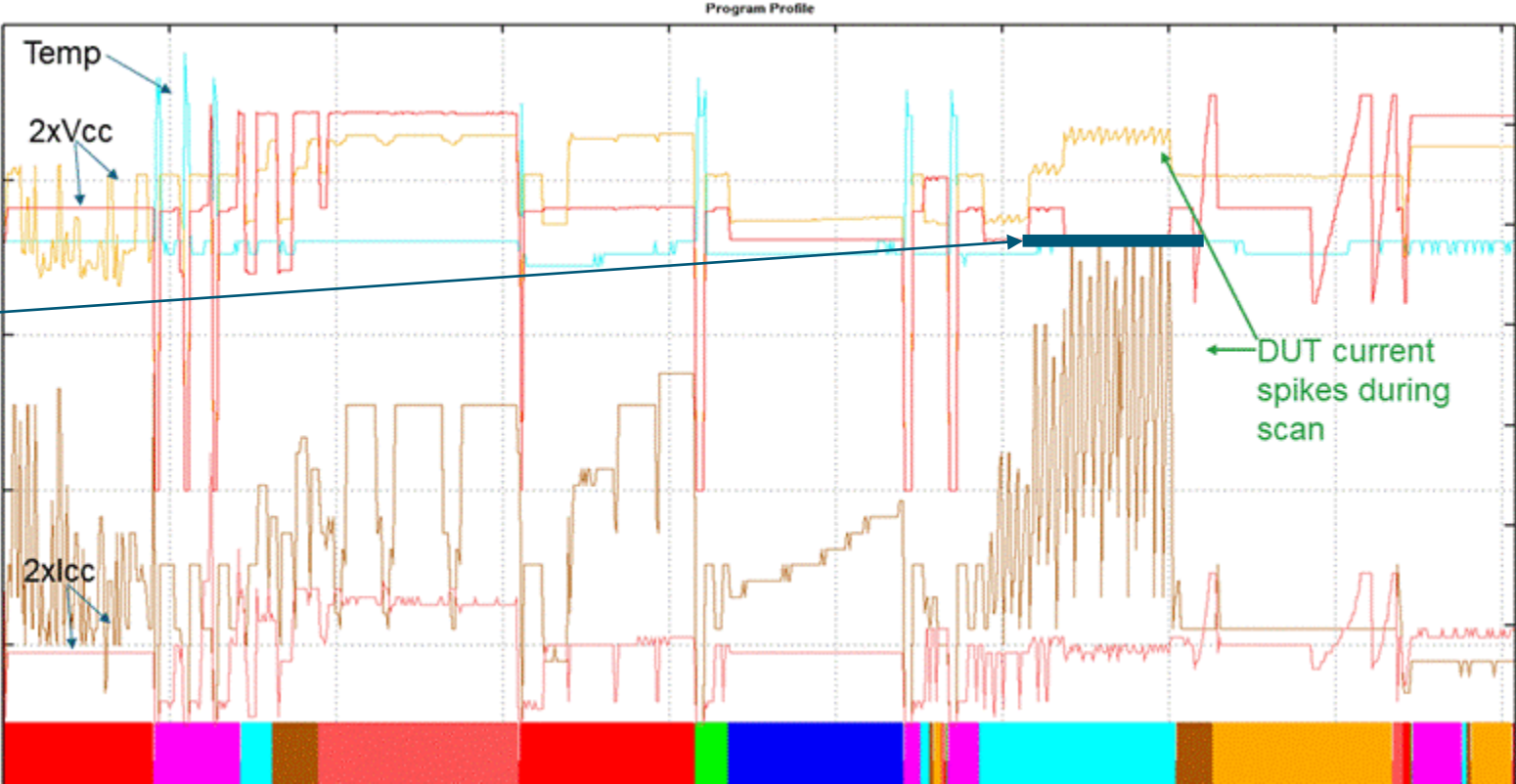


# How Much Power is Really Needed?

Real world data is very “messy”.

The maximum current consumption is typically driven by scan test vectors.

Power aware scan pattern generation can reduce the peak current consumption significantly.

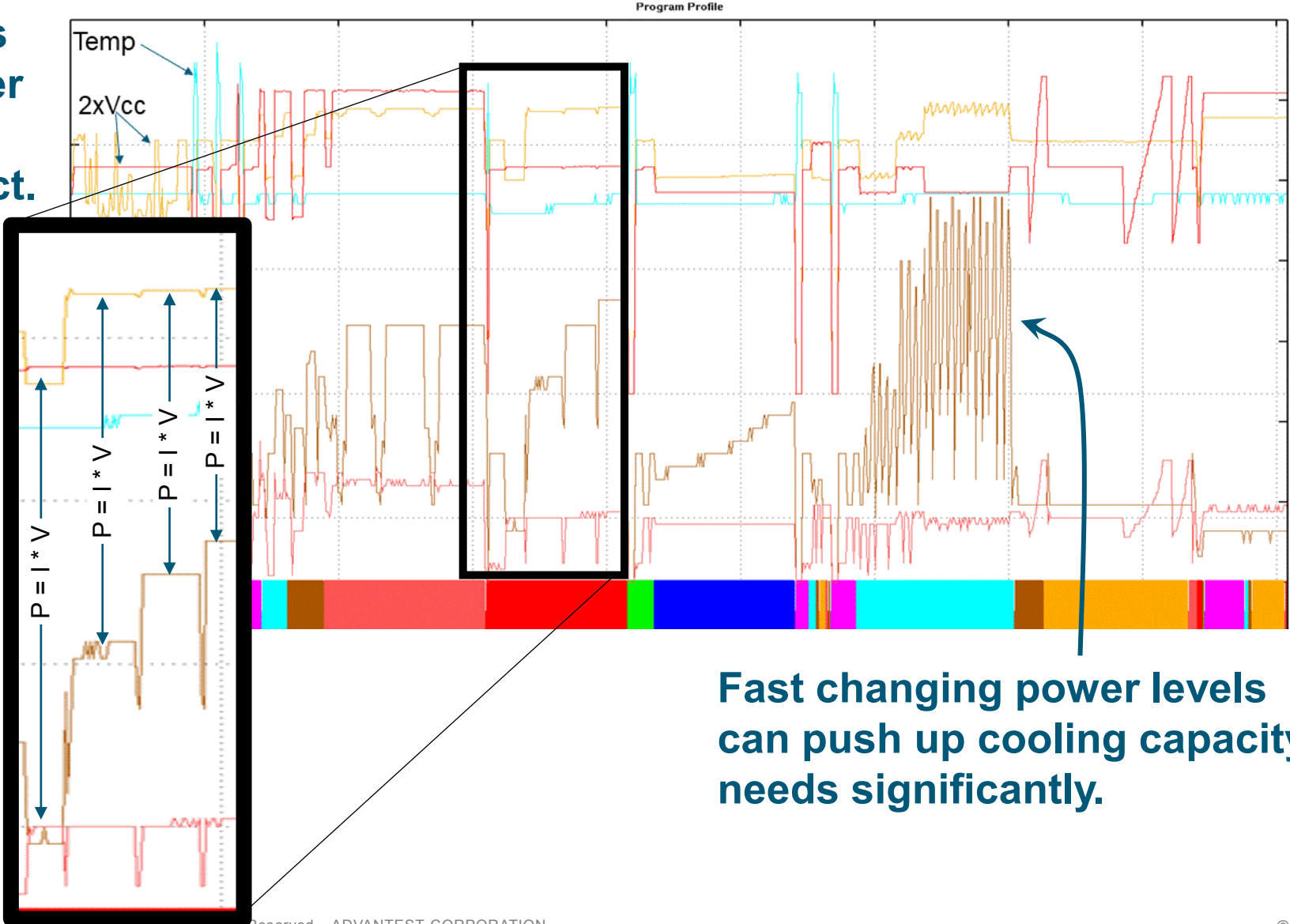


# How Much Cooling is Really Needed?

The cooling system capacity is designed for the average power consumption. This may be higher or lower than you expect.

First one needs to look at all the tests and calculate voltage \* current levels.

More discussion of control signals for Active Thermal Control (ATC) in later slides.



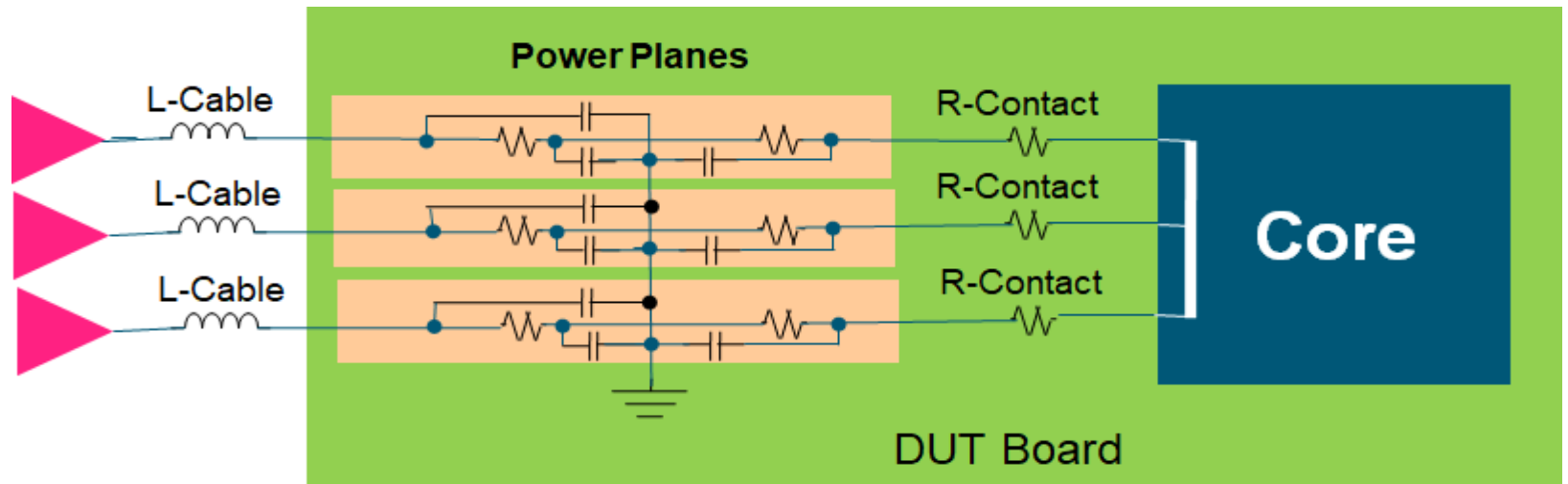
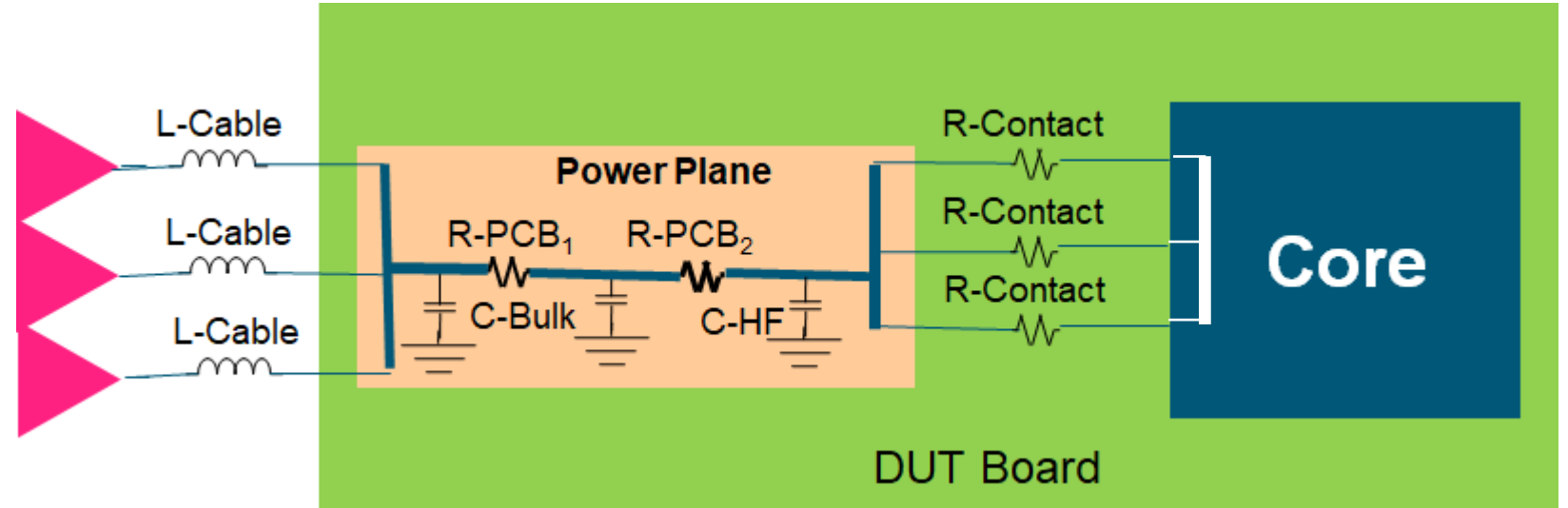
Fast changing power levels can push up cooling capacity needs significantly.

# Ganging With Control

Like a fire-hose, DPS ganging needs to avoid bottlenecks.

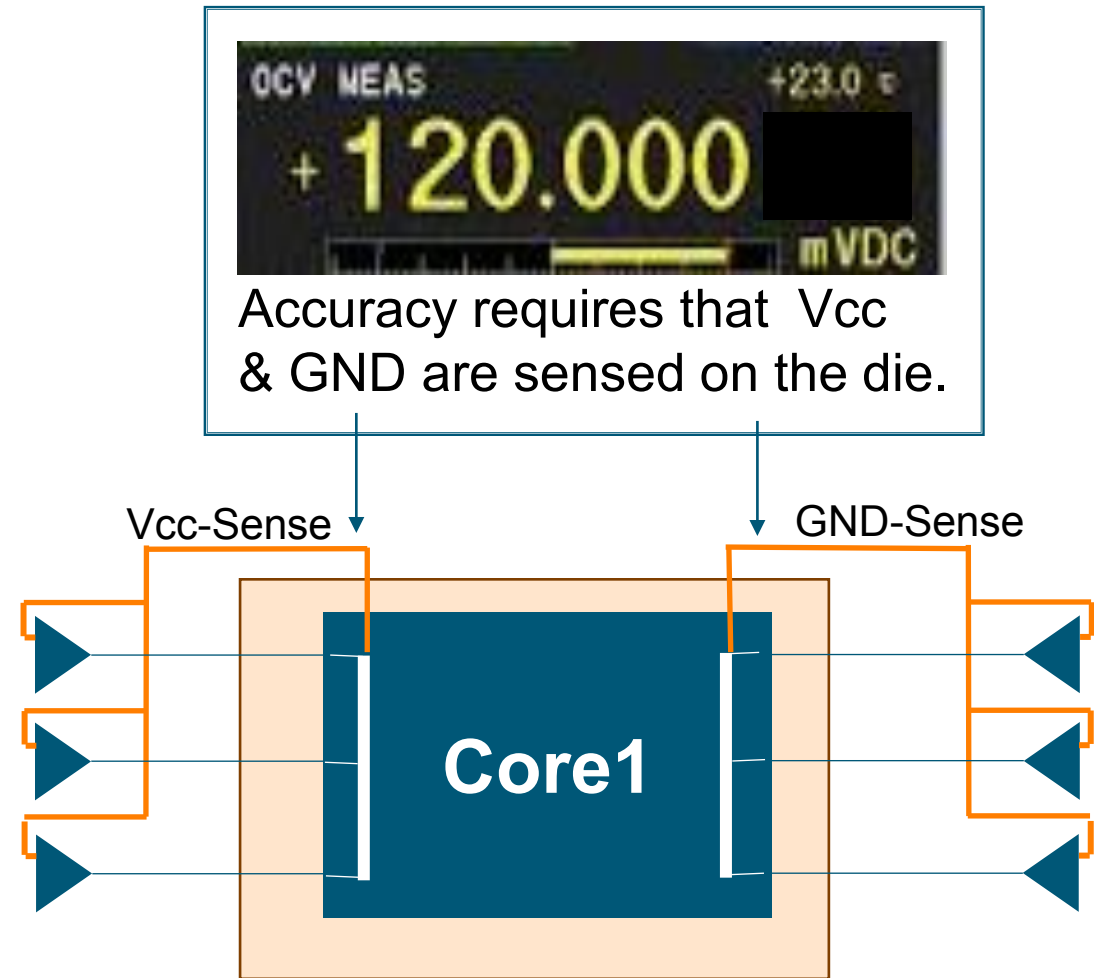
## Approach Summary for High Current Testing

1. Merging in supply Module
  - Terrible approach
    - Risks cables
    - Risks probe/socket
2. Merging on DUT Board
  - Bad approach
    - Risks probe/socket
3. Merging both on chip & DUT board
  - Bad approach
    - Risks probe/socket & chip
4. Merging only on chip
  - > Best approach



# Accurate Sensing

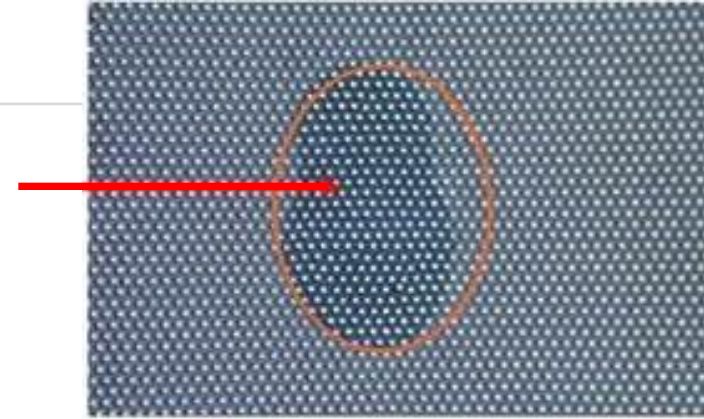
- Power supply voltage are dropping <1V.  
→ Voltage accuracy is critical.
- Dividing up powers and ground keeps current paths clear, and noise compartmentalized.
- Having separate supplies allows better control and lower noise levels.
- Ground and supply sensing should be done on the device near the individual cores.
- If you have supply and/or ground paths feeding multiple cores, consider switching to different sense lines as different cores are being tested.



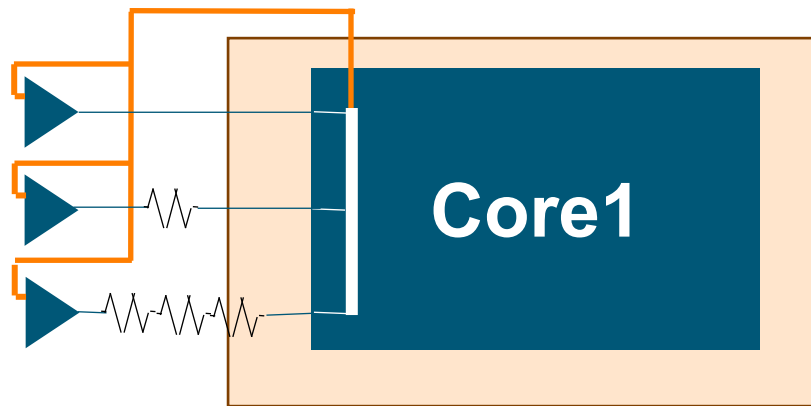


# Avoiding Burnt Probes – (1<sup>st</sup> of 3 Key Tasks)

Burnt probe cards is a major cost factor to the industry



## 1. Ensure that probe current is well controlled

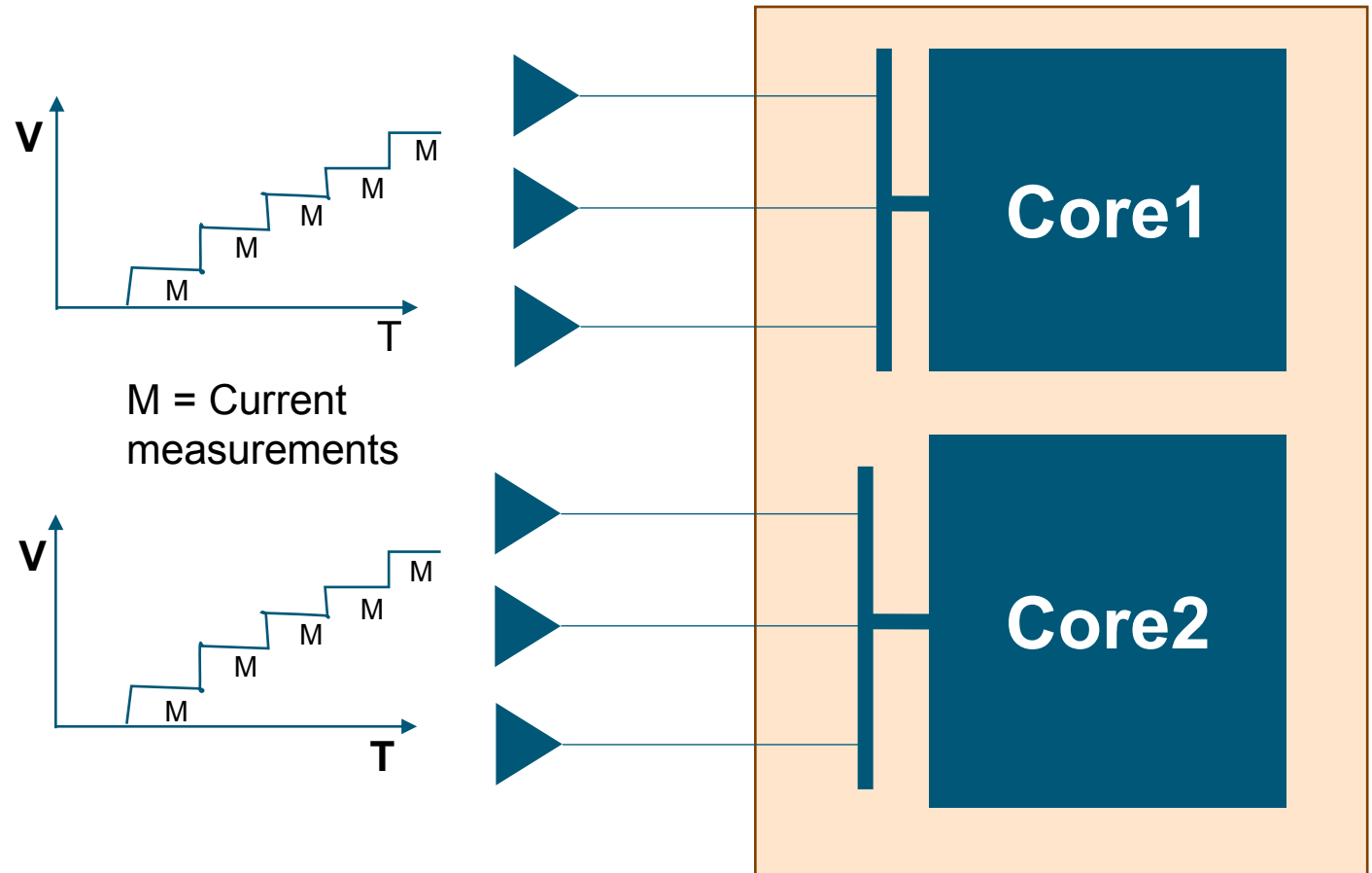


- Segmented power planes allow accurate contact resistance measurements for preventative maintenance.
- Active current balancing between the parallel channels avoids exceeding CCC.
- If contact resistance becomes too high on one of the channels current can be re-distributed within design constraints. If excessive an alarm can be raised.

# Turn Supplies on Carefully & Check Currents (2<sup>nd</sup> of 3 key tasks)

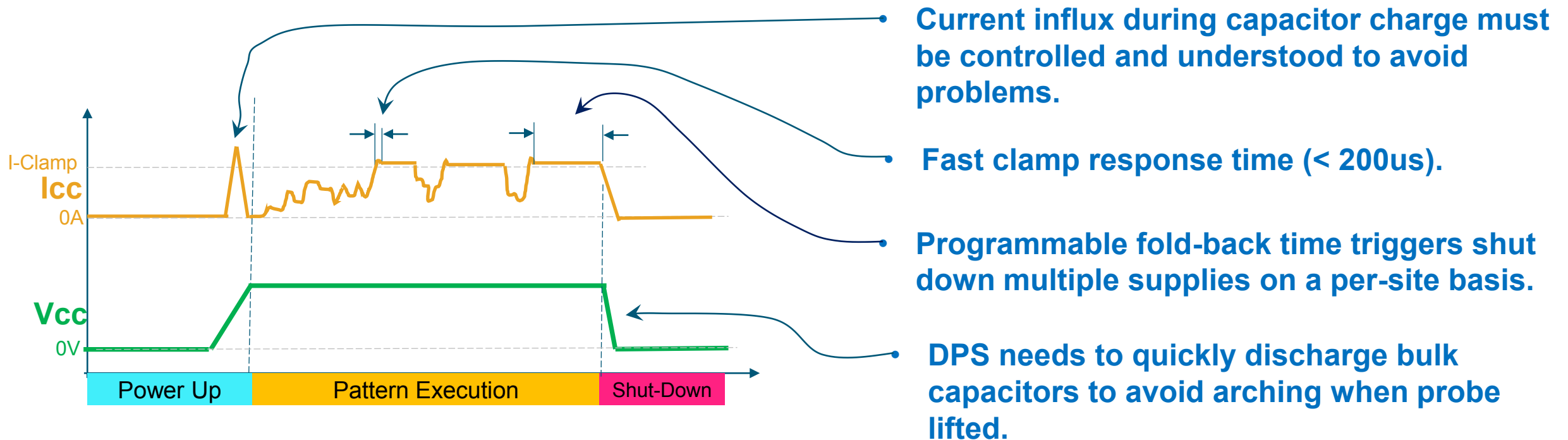
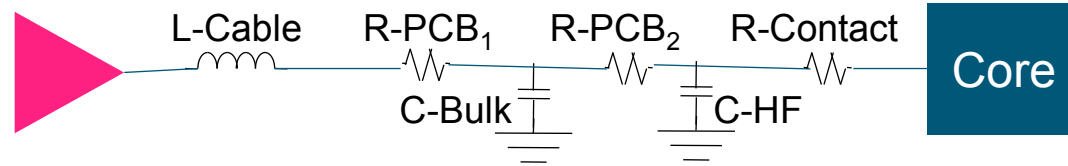
## 2. Turning on high-current supplies must be done very carefully.

- Since shorts can occur between power and ground as well as between cores, multiple cores with separate supplies must be powered up in lock-step.
- Using a small voltage step (typically <100mV) gives time for everything to settle.
- Checking the current draw after each step allows sequence to stop if a problem is noted.



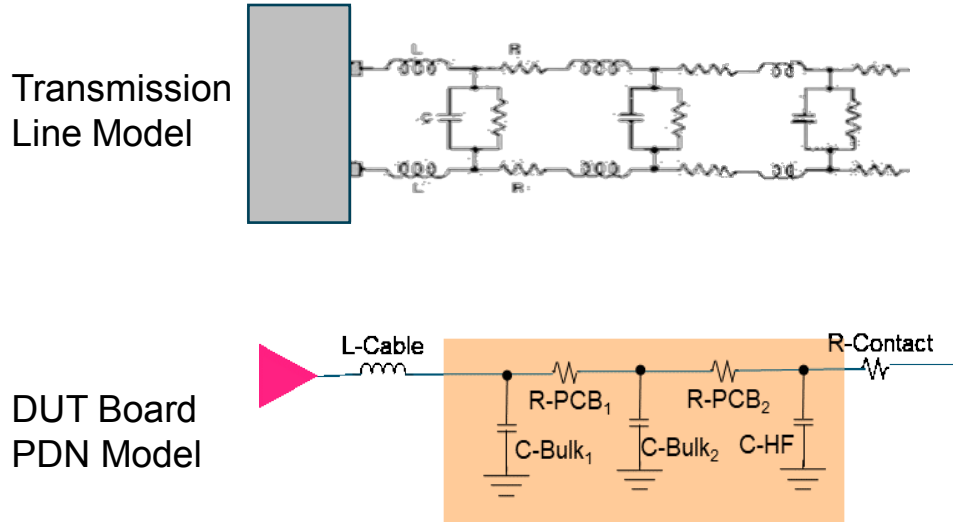
# Avoiding Burnt Probes (3<sup>rd</sup> of 3 Key Tasks)

## 3. Respond in a fast and well-controlled way.

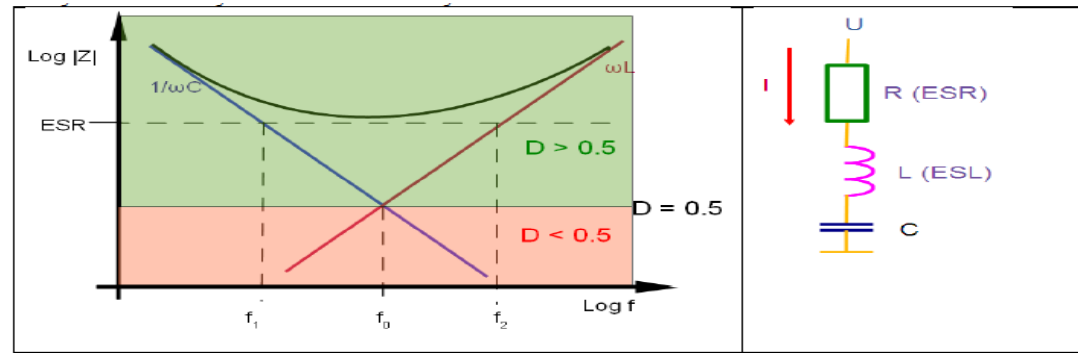


# Power Distribution Networks

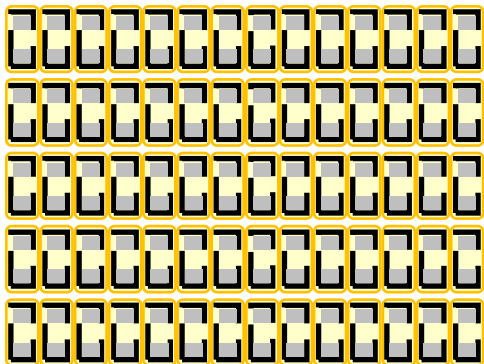
The DUT board circuitry is very similar to a transmission line.



When designing a DUT board selecting the right capacitors in the right quantity is critical. “Too Little” C is certainly bad . . . And “Too Much” C can also be worse.



The next challenge is DUT board area & component costs.



- All high-power DUT-Boards need the right amount of tantalum bulk capacitance for optimal droop performance.
- All DUT-boards need good high-BW ceramic bypass capacitors near the DUT.

- Tantalum capacitors provide superior value for bulk-C:
  - ✓ Pros: Wider temperature range  
Higher uF/mm<sup>2</sup>  
Lower \$\$/uF
  - ❖ Cons: Higher ESR @ High F  
Polarized

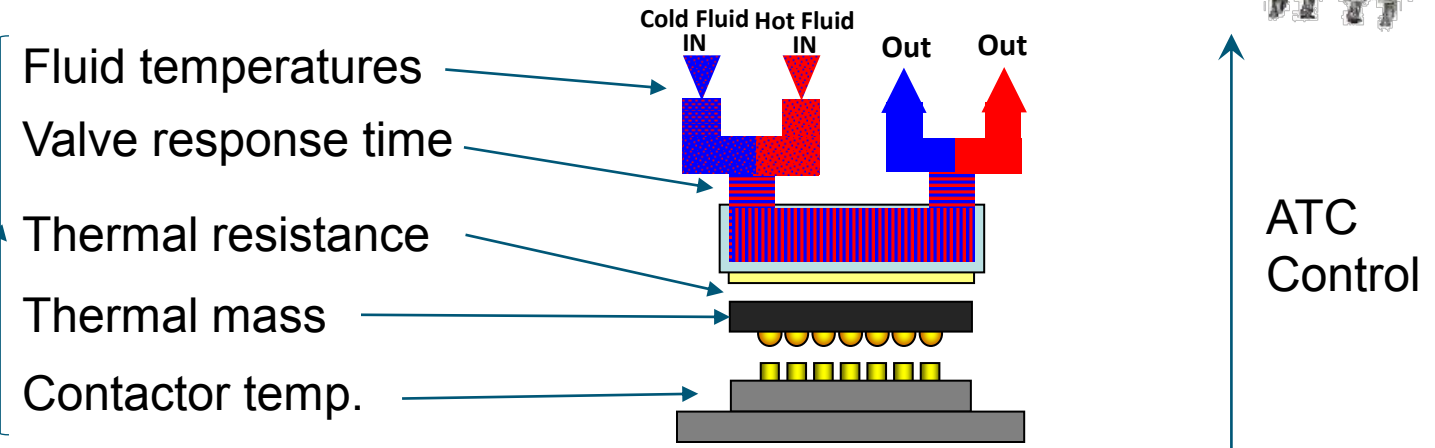
# The Art of Active Thermal Control

Advantest has very fast responding high-power handlers and a die-level prober available.

Fundamental constraints limit the response time to milliseconds.

The ATC control signal is key to avoiding over and under temp conditions. Three methods are available:

1. Thermal diodes
2. Power Following
3. Power Anticipating



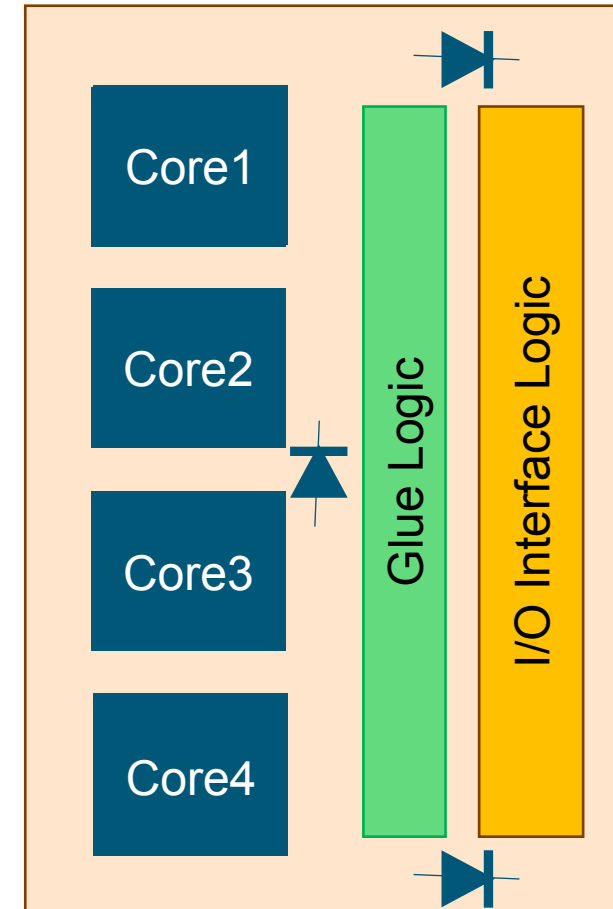
# ATC Interfaces – Thermal Diodes

Adding a thermal diode into the chip is quite standard today.

**Single** diode feedback is inadequate for high-power designs as different areas of the die heat up with different amounts at different times.

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**Multiple** diode feedback is strongly recommended for high-power device testing. These signals can be combined in different ways: Max temp, average temp, targeted/switched temp to name a few.



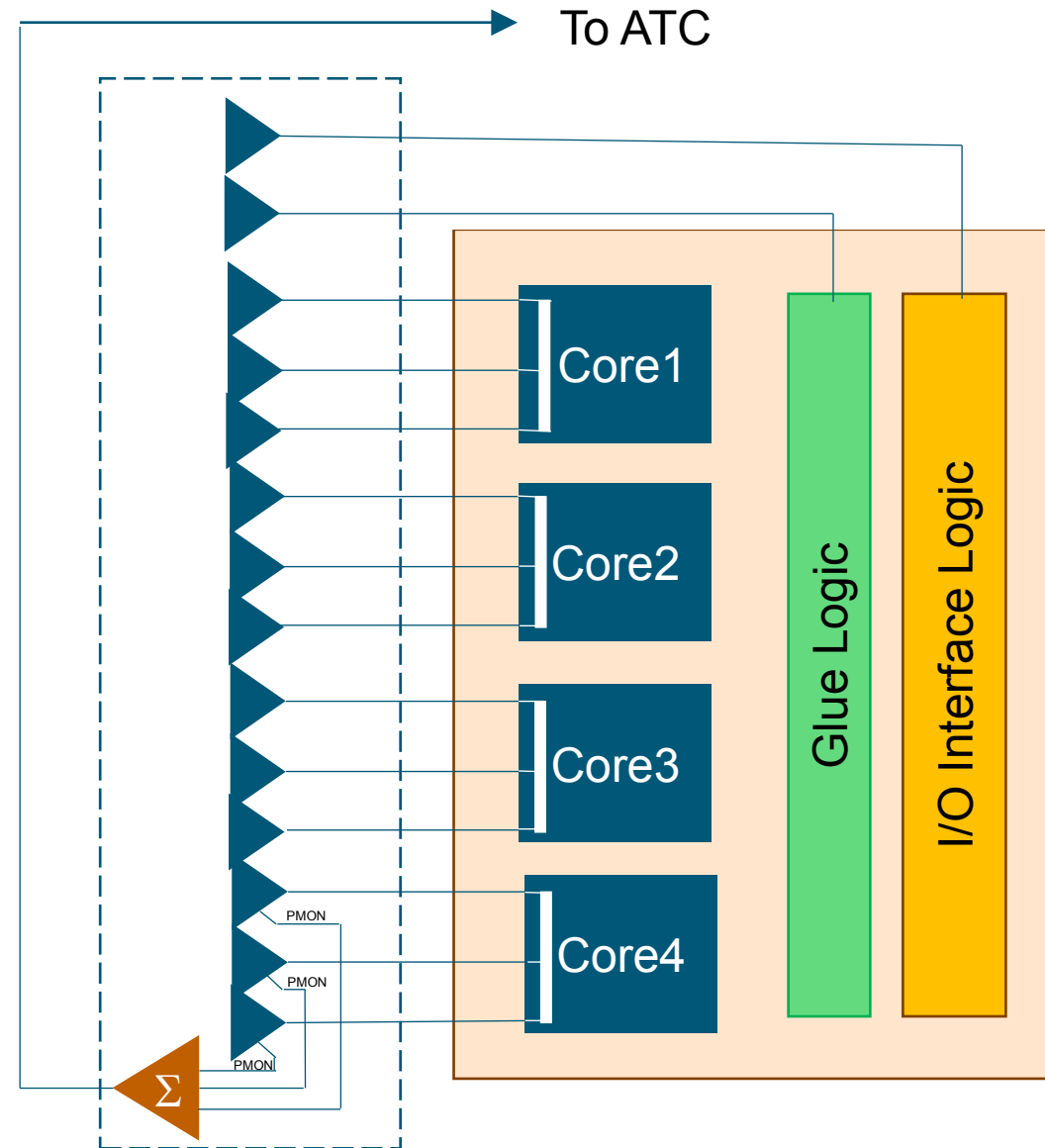
# ATC Interface – Power Following

Supply current feedback has been used for years in “Power Following” applications.

Best case this gave the ATC system a few microsecond head-start and feedback was only current not power.

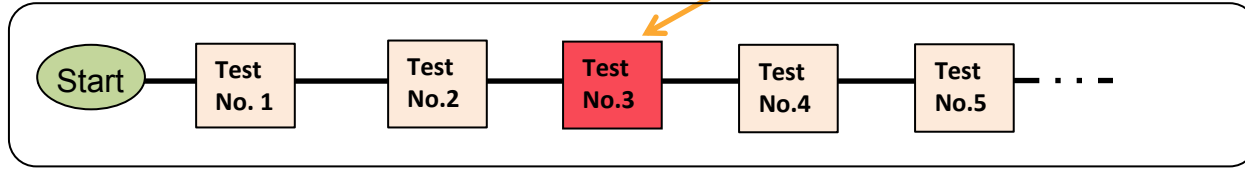
New ATE power supplies can send a tracking signals proportional to actual power consumption out to the thermal control system.

This allows the ATC response to be focused by the test flow on the core(s) active in the test at that time.



# ATC Interface – Power Predicting

Test suite which causes thermal spike!

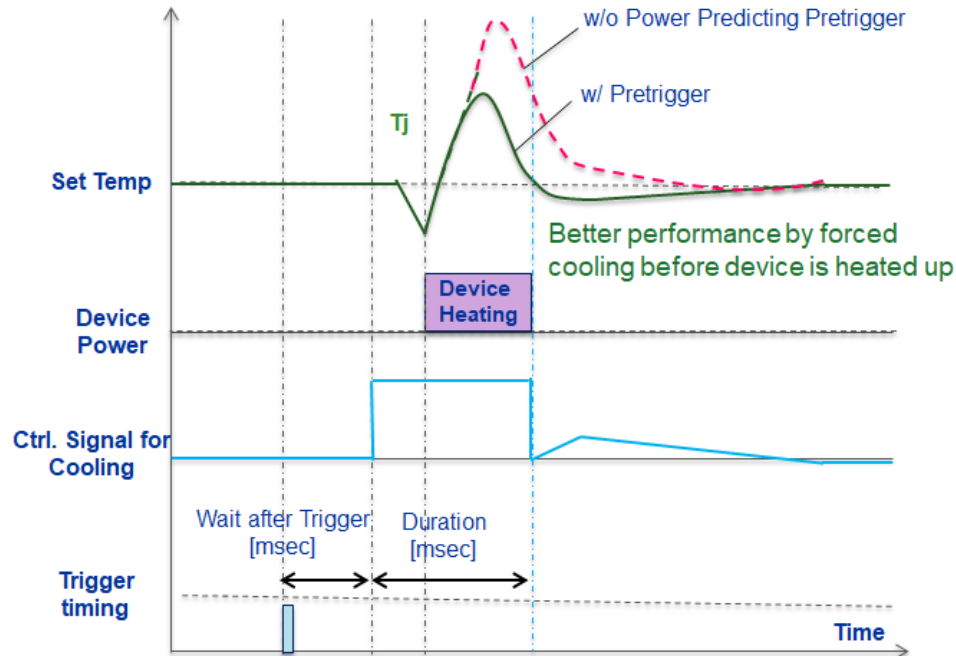


Cooling  
Ctrl Signal



The test system knows when more cooling is going to be needed.

The V93K can send the ATC system a pre-trigger so that temperature extremes are avoided.



(10) United States  
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(43) Pub. Date: Sep. 11, 2014

(54) ADAPTIVE THERMAL CONTROL (52) U.S. CL. CPC ..... G05D 23/2017 (2013.01); G01R 31/2874 (2013.01) 324756.03  
(71) Applicant: Advantest Corporation, Tokyo (JP) USPC .....  
(72) Inventor: David H. ARMSTRONG, Lafayette (US); Mike C. CALLAWAY, La Mesa, CA (US) (57) ABSTRACT

(73) Assignee: Advantest Corporation, Tokyo (JP)  
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G01R 31/28 (2006.01)

ABSTRACT  
An adaptive thermal control system maintains and regulates an accurate and stable thermal environment for a device under test. The adaptive thermal control system includes (1) pre-trigger communications from automatic test equipment (ATE) to automatic thermal control (ATC) allowing slow-responding ATC to start responding to an imminent thermal change before the thermal change occurs, (2) a control profile which indicates to the ATC, prior to anticipated thermal change, that a change is imminent and the nature of the change over time. The generation and fine-tuning of the control profile can be done by two different methods: (i) with the semi-automatic approach the tester does some pre-tests in order to determine a typical response profile which the test program then adjusts using adaptive techniques, (ii) With the fully automatic adaptive capabilities some typical response profile is algorithmically adjusted and utilized to control the ATC.

Advantest Patent  
#9291667



# BKM's for High-Power Device Testing

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## 1. Plan Ahead!

- a. Select the right ATE, handler, prober, probes, contactors, and thermal control systems.
- b. Calculate maximum current draw considering scan patterns plans & power-aware EDA tools to config ATE.
- c. Work with cooling system experts to size capacity based on  $V_{max} * I_{max} * DC$  + uplift for fast power changes.

## 2. DUT Boards need lots of attention!

- a. Use tantalum bulk capacitors of the right  $C_{total}$  per the calculator.
- b. Use good high-frequency ceramic capacitors near the DUT.
- c. Each high-consuming sub-circuit (core) likely needs its own supply current path as well as sense feedback.
- d. If you have extra DPS channels – gang them with your highest current channels for faster settling times.
- e. Explore possible usage of high current-carrying probes or pogos.

## 3. Careful test programming is critical!

- a. Slowly step the various core voltages up while monitoring the current draws for any problems.
- b. Utilize power-aware EDA tools to create patterns which minimize high-power transients.
- c. Space out your high-power events to minimize average power dissipation.

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