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TOO **HOT** TO TEST

Thermal Management
of ICs During Testing

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Too Hot To Test

February 9 - 11, 2021

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Hot Packaging Solutions

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Ack. Madhusudan Iyengar (Google) on behalf of HIR Thermal TWG

February 2021

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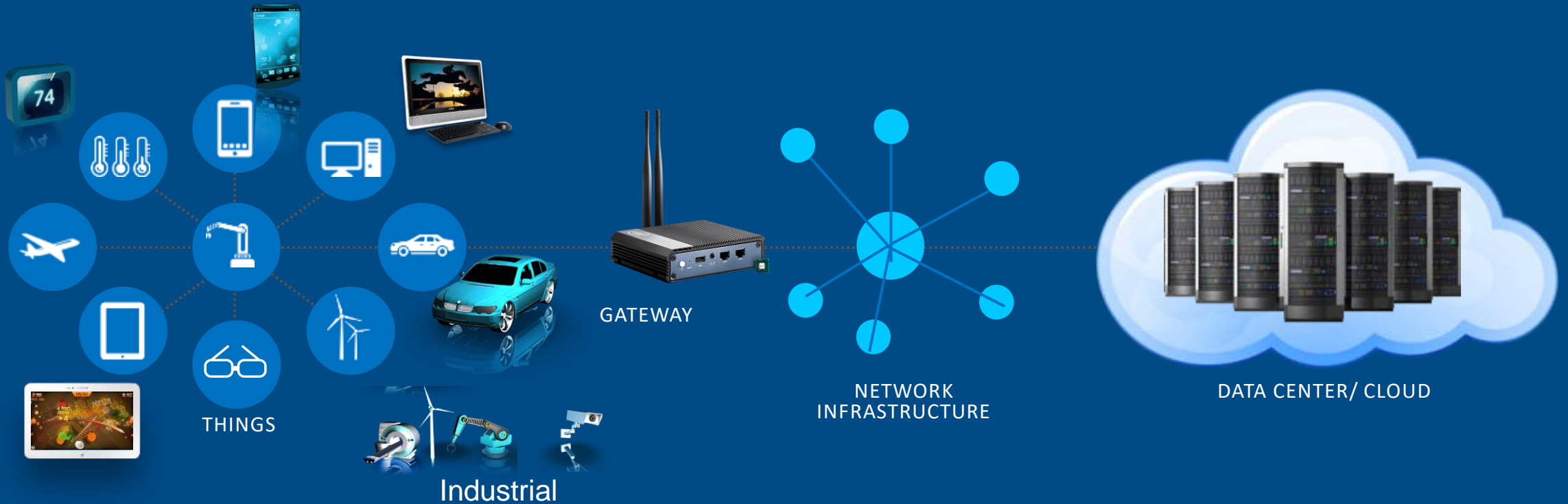
FEBRUARY 9-11, 2021 ONLINE

Agenda

- Overview of the Evolution of Electronic Packaging
- Advanced Packaging & Associated Thermal Challenges
- Addressing Thermals at the Silicon, Package and System-level
- Call to Action

The Diversity of Connected Devices

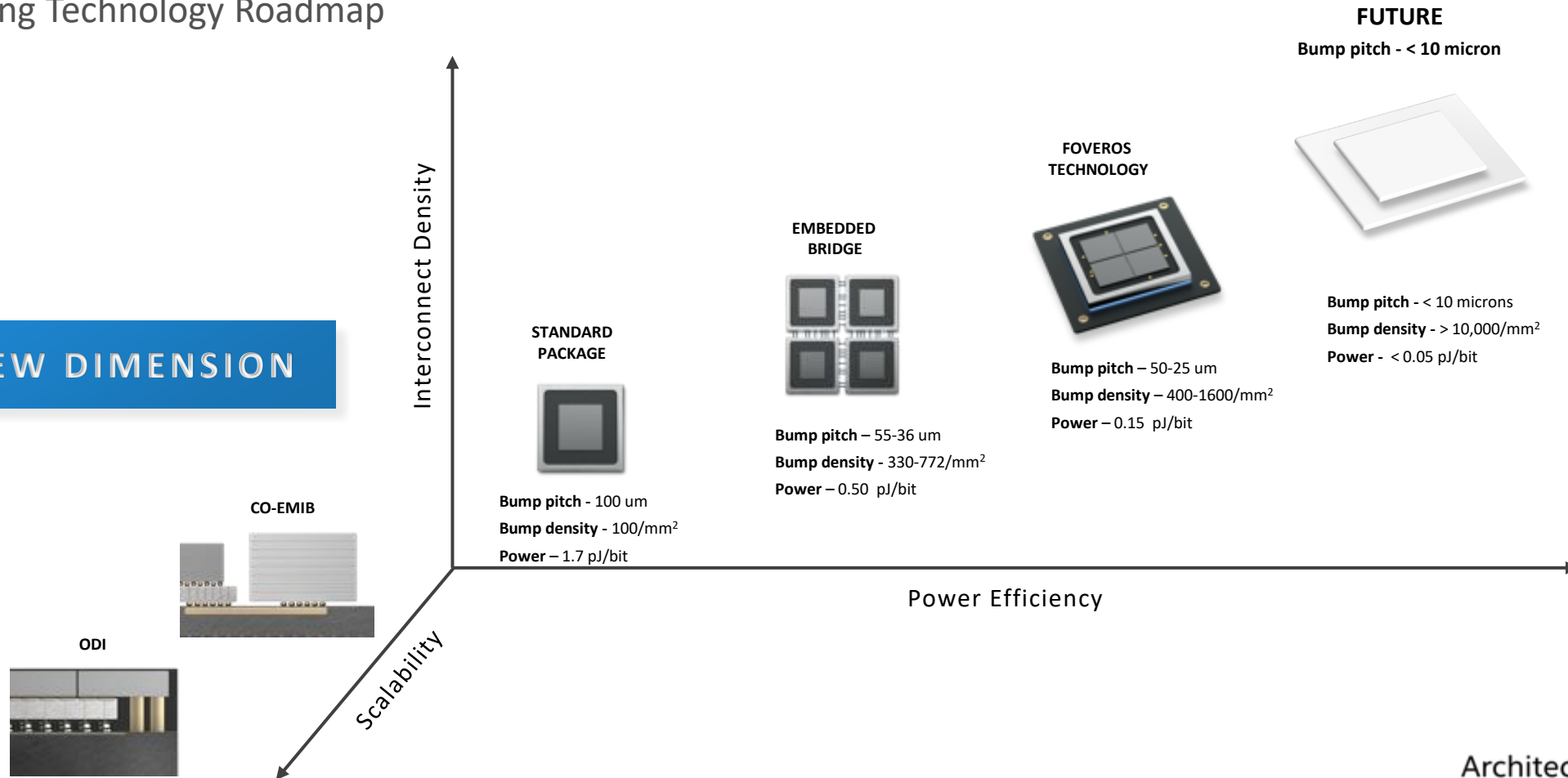
- Broad Spectrum of Devices, Packages & Form Factors
- Power consumption from a few watts to several hundred watts
- Cooling solution and system boundary conditions are quite different and diverse



Packaging Technology Driven by Si Scaling, IO density and Heterogeneous Integration

Packaging Technology Roadmap

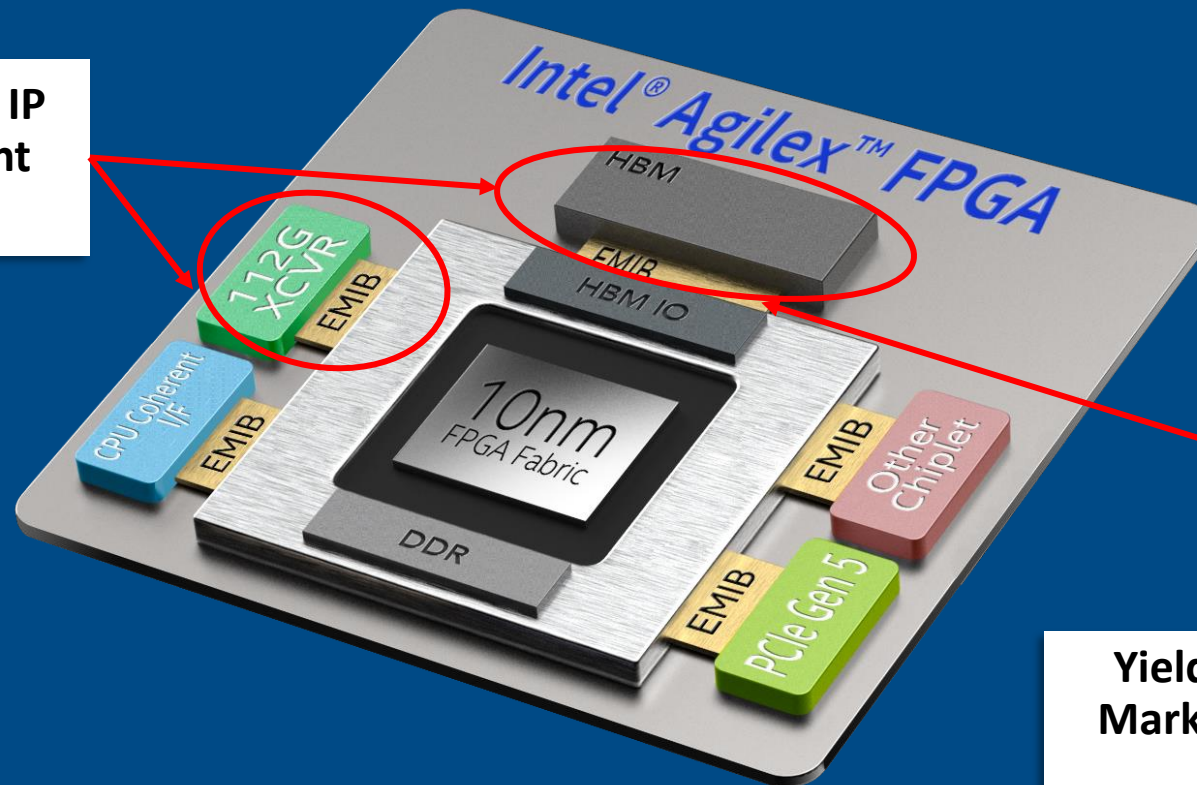
A NEW DIMENSION



Architecture Day 2020

Increased Interest in Heterogeneous Integration: Power, IO, Resiliency and TTM

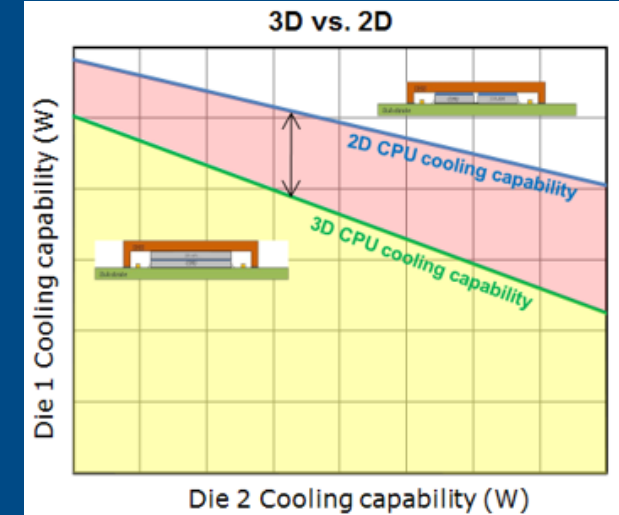
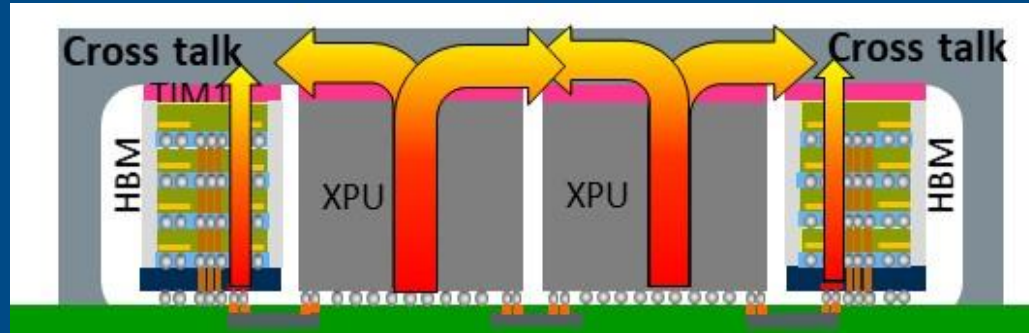
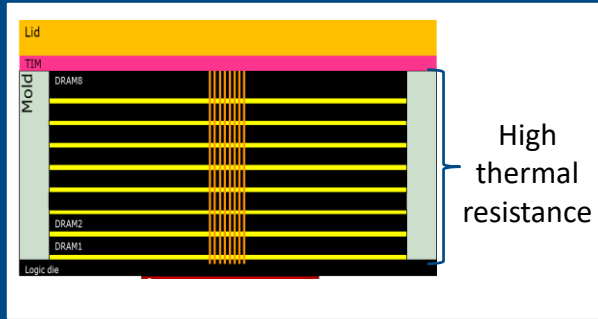
Integration of Diverse IP Optimized on different processes



Need for High BW Memory with a low power Interface

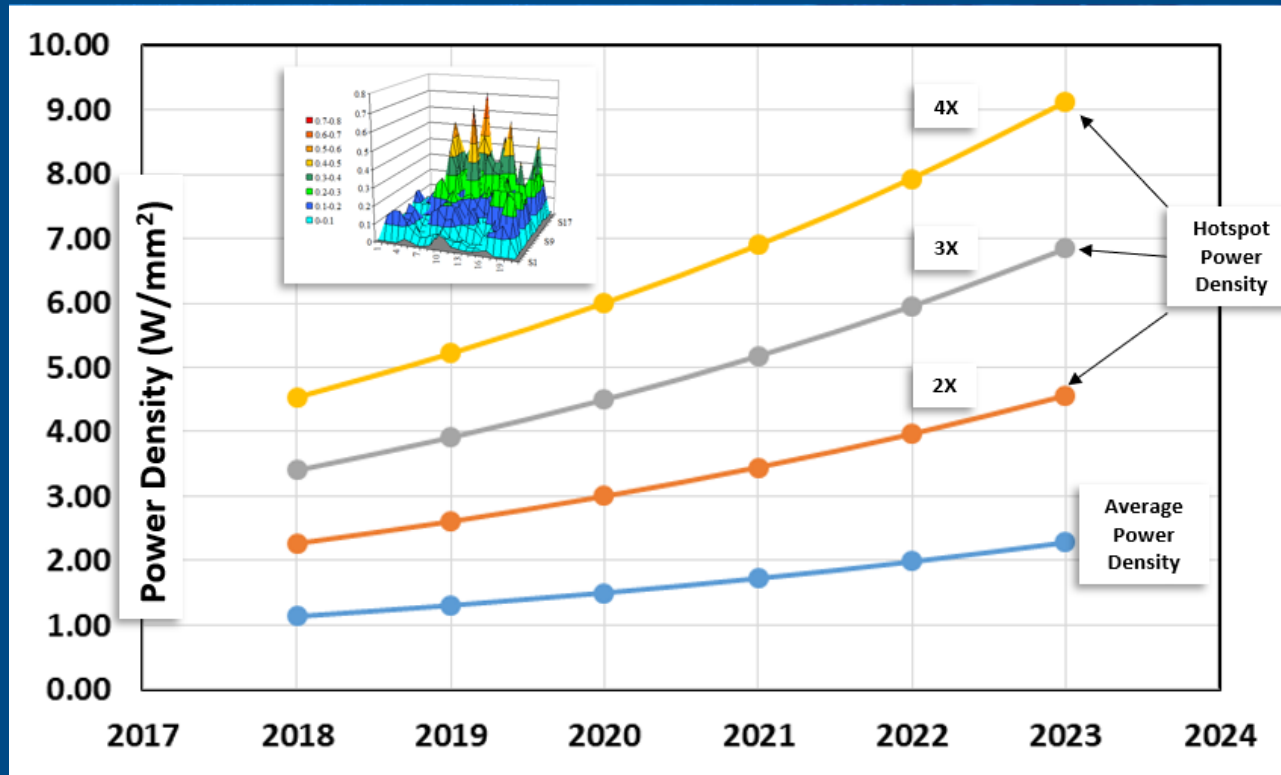
Yield Resiliency and Time to Market are other Factors that make HI Attractive

Heterogenous Packaging: Thermal Challenges



- Increasing power and power density
- Increasing package thermal resistance
- Thermal cross-talk, including thermal isolation
- Different thermal (T_j) requirements for each functional IC
- Thermo-mechanical enabling

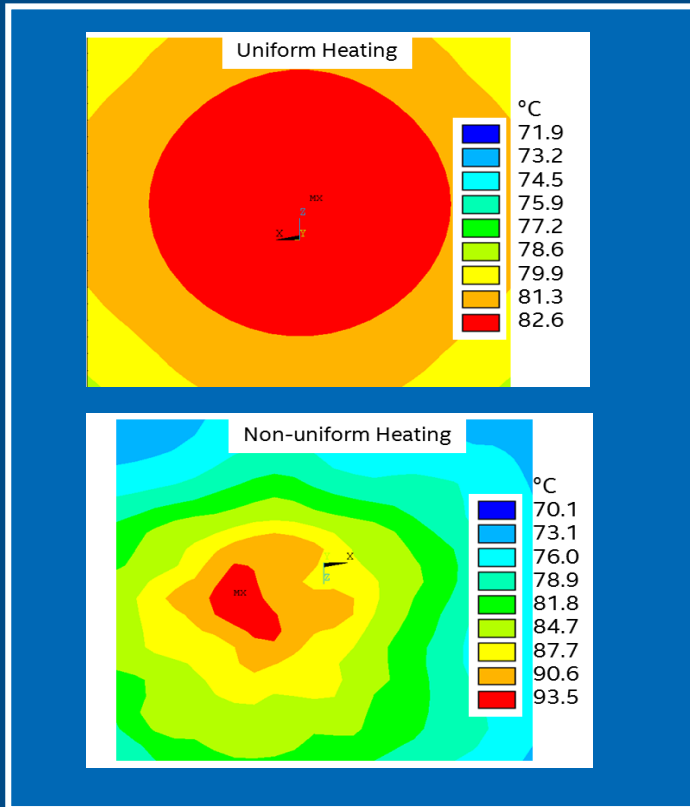
Thermal Demand Envelope



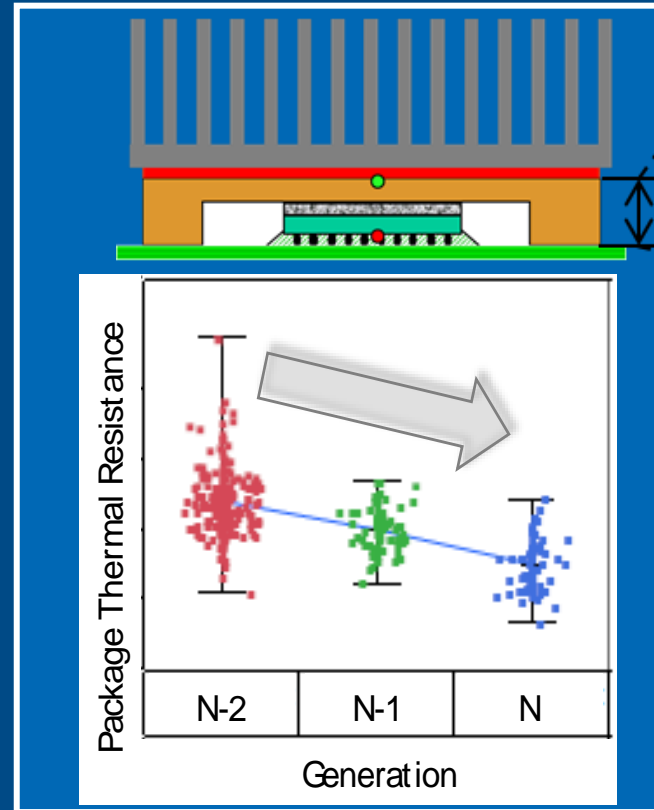
Thermal Technologies must typically cover a Hotspot Density Envelope in the (3x-4x)* range with an understanding of upside capability for both 2D & 3D Architectures

* It is important to recognize that these ranges are architecture and use case dependent. Thermal technologists must focus on developing technology building blocks to provide maximal, cost effective cooling

Need Holistic Thermal Solutions



Thermally Aware Design

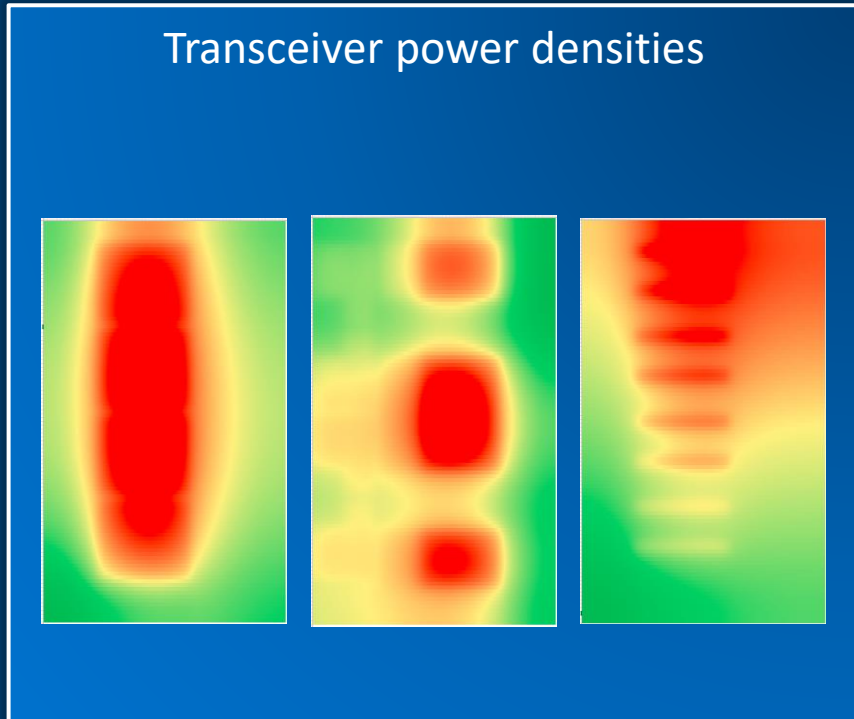


Package Thermal Improvement

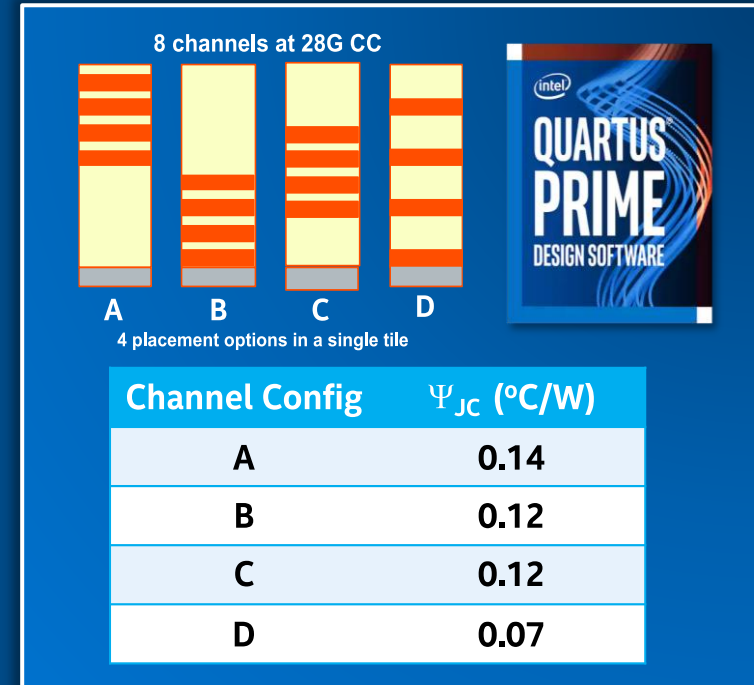


Cooling Solutions & System Design

Thermally Aware Design: FPGA Example



programming affects power density



Tools to minimize power density

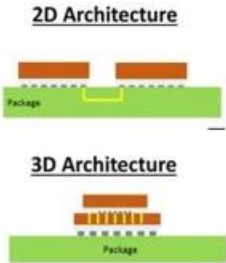
Heterogeneous Integration Roadmap: Thermal TWG

Heterogeneous Integration Roadmap Workshop

Heterogeneous Integration Roadmap Thermal Technical Working Group (TWG)


Presented by
Madhu Iyengar (Google)
On behalf of the Thermal TWG

ECTC 2020



2D Architecture

3D Architecture



HIR Thermal TWG - Work Status

- Year 1 (2018-2019)
 - Thermal effort kicked off in March 2018.
 - ~30 industry and university expert contributors.
 - Final Chapter completed in June 2019.
 - Published on EPS Website
- Year 2 (2019-2020)
 - Receive and implement cross-TWG content.
 - Address feedback received on 2019 edition.
 - Opportunistically add new content if possible.

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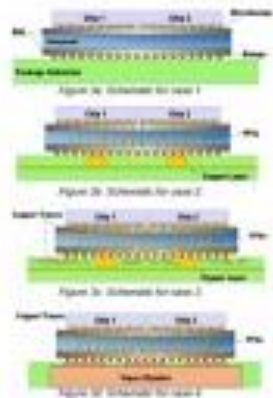
2020/2021 Chapter Thermal HIR Potential Topics

1. Hotspot thermal management
2. High Bandwidth Memory (HBM) cooling
3. Photonics thermal control
4. Power and power density trends
5. Silicon microchannels manufacturing
6. Thermal test protocols for heterogeneous packages

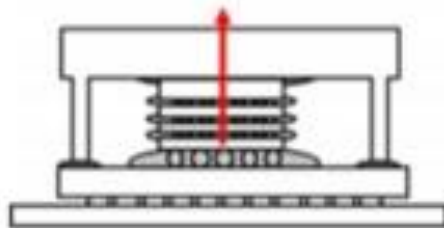
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Thermal Problems Identified

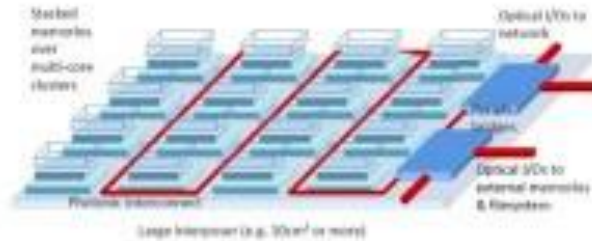
IEEE HIR Thermal TWG - ECTC 2020



1. 2D chip with stacked memory on a silicon/glass interposer

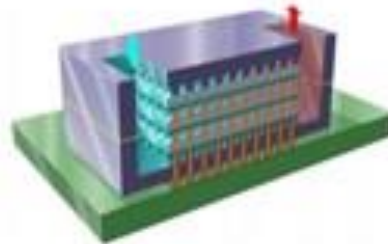


2. 3D stacked die with conduction interfaces



4. Optics/photronics based Heterogeneous package

2019 Chapter Canonical Thermal HI Problems



3. 3D stacked die with embedded liquid cooling

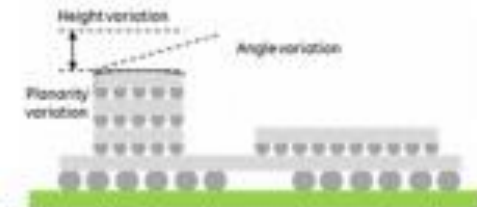


Figure 11: National 3D chip architecture and anticipated topology challenges

5. Harsh environment (military, aerospace, automobile)

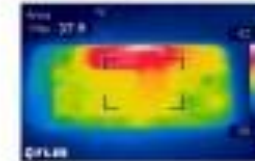


Figure 14: Temperature contour data for the external surface of a heat pipe (1W)

6. Mobile application chipset (package on package, fan out, bridge)

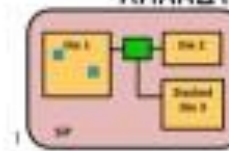


Figure 16: Package level DC to DC 1.8V converter

7. Voltage Regulators in a Heterogenous Package

2019 Chapter - Advanced Technologies & Research

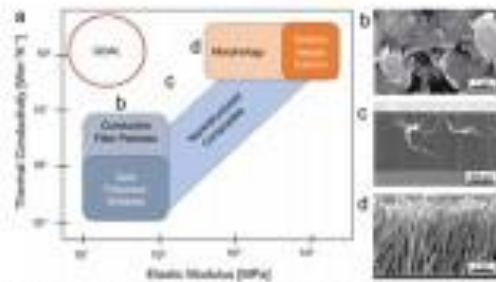


Figure 17: (a) Two common strategies used to engineer for greater high-performance TIM composition: (1A) an example of graphene/polymers composite (1A), (b) vertically grown nanowires (1B,1C), (c) vertically electrospun nanowires (1C, 1D)

1. Thermal Interface Materials

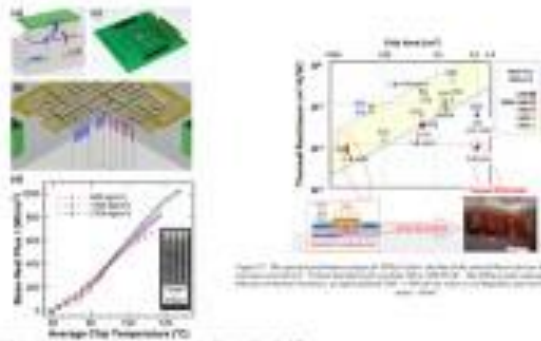


Figure 18: (a) Schematic diagram of a chip-to-chip interface with a TIM. (b) Schematic diagram of a chip-to-substrate interface with a TIM. (c) Graph showing the thermal conductivity of a TIM as a function of temperature. (d) Photograph of a chip stack.

3. Embedded liquid cooling of chip and chip stacks

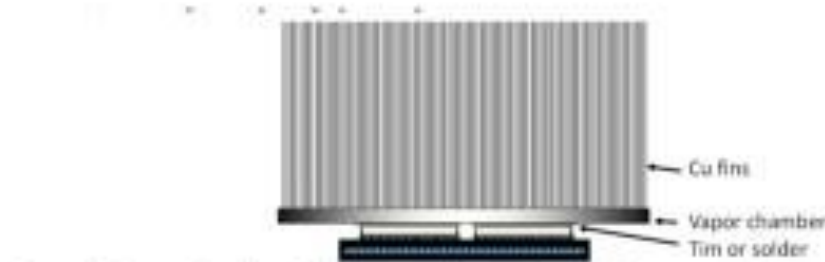


Figure 19: Figure adapted from [23] showing a schematic diagram of a heterogeneously integrated multi-chip module with a Thermal Interface Material (TIM) or solder attachment and a vapor chamber

2. System thermal limits for HPC multi-chip modules

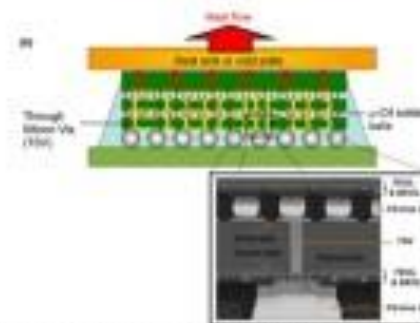


Figure 20: 3D chip stack with advanced materials in conductive heat flow path (19)

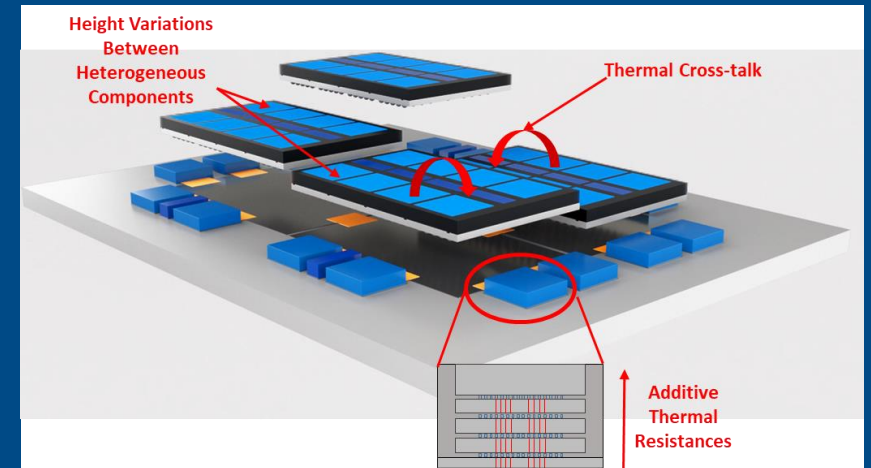
4. Advanced Thermal Materials for Thermal Management



5. Thermomechanical Modeling for Heterogeneous Integration

Call for Innovation on Thermal Management

- **Better TIMs and heat spreaders for MCPs**
 - $\geq 2.5x$ Rjc reduction – Near Term Target
 - 10x reduction should be a target for the next decade
- **Dual-purposed TIMs as a warpage control solution**
- **Complement package level solutions with System level solutions**
 - Research in liquid cooling (including immersion) material/design options
- **New Materials & Cooling technologies**
- **Improved metrologies**
- **Increased focus on transient responses**
- **Strengthen Co-Design Interfaces**
- **New technologies such as photonics, quantum computing**



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