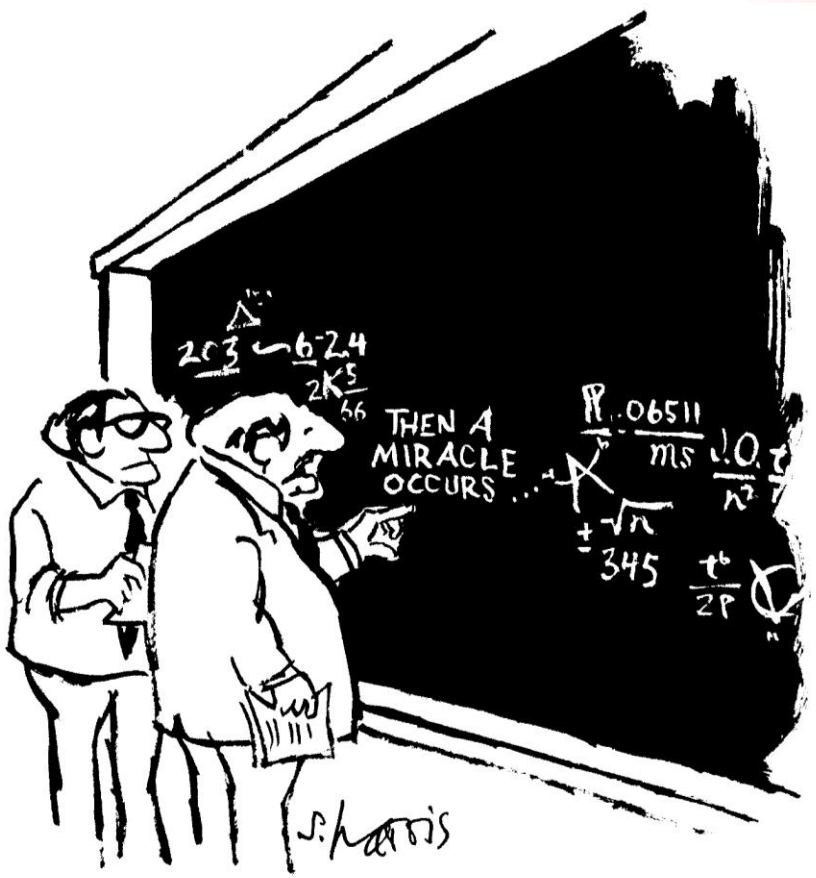
Known Not Bad Die Success: Repair, Redundancy, and Pragmatism

September 17, 2020

NHANCED SEMICONDUCTORS

How to Solve KGD for Advanced Packaging?



"I think you should be more explicit here in step two."

What's so Funny about Science? By Sidney Harris (1977)

→Design For Repair!

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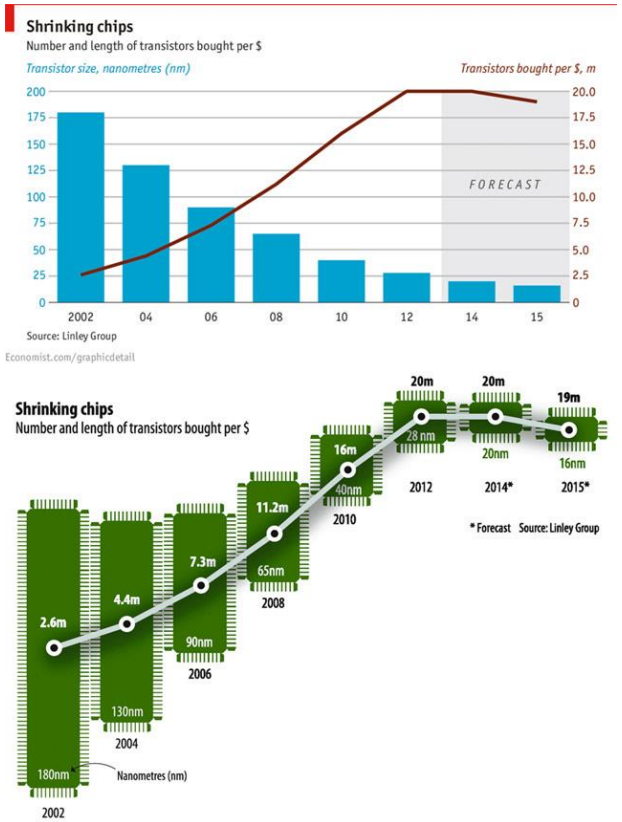
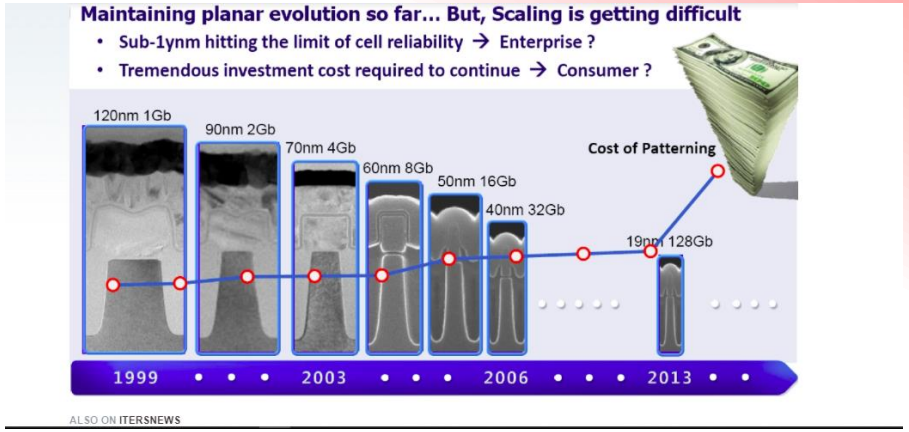
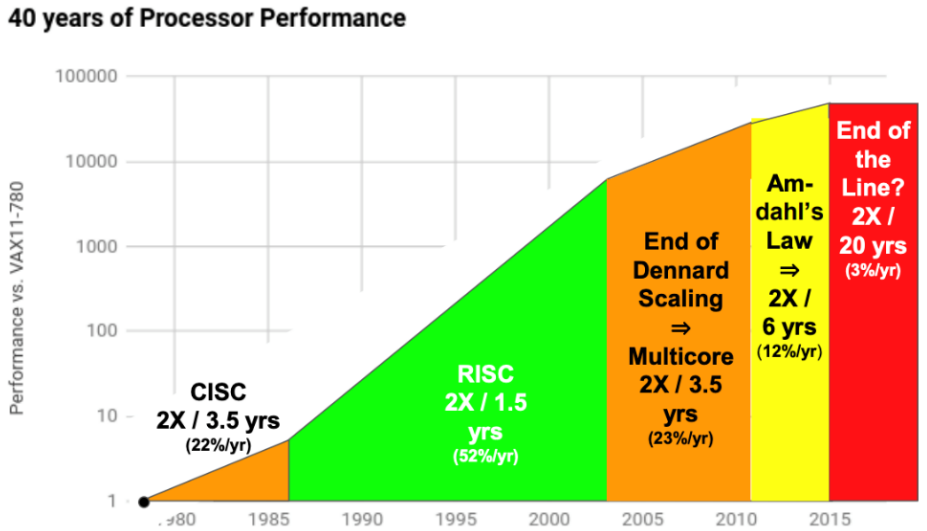
HOW DID WE GET HERE??

End of Moore's Law





End of Growth of Single Program Speed?



Apple A12 single thread performance (RISC ISA) = x86 Skylake single thread perf (SPEC), at much lower power, *Anandtech* 10/8/18

Based on SPECintCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018 **15**

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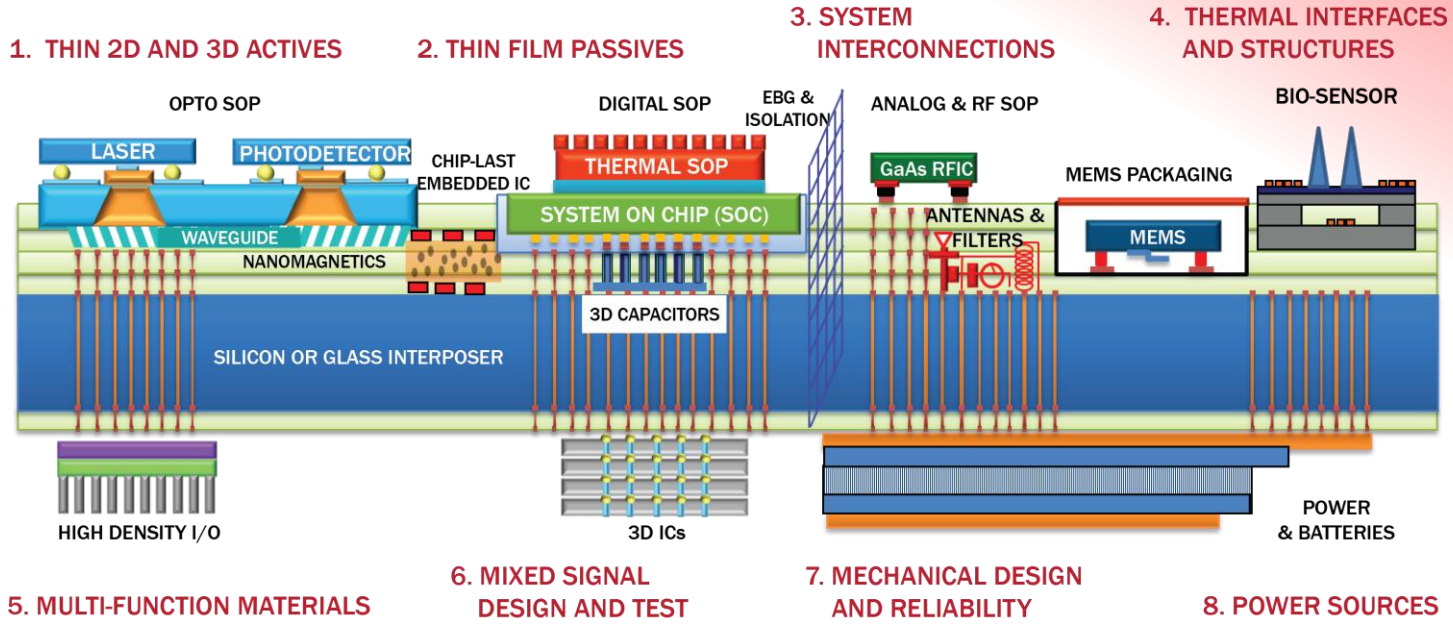
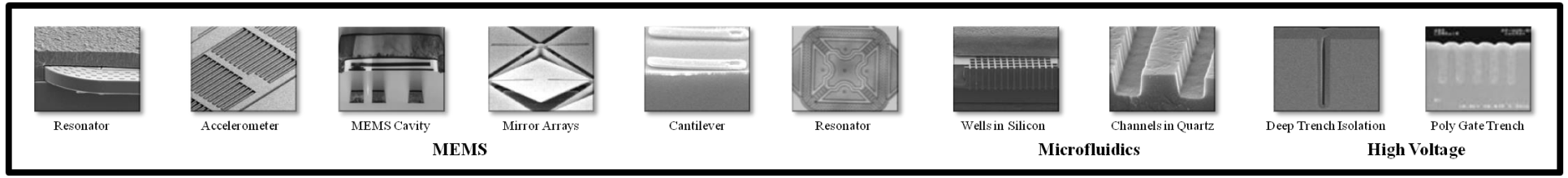
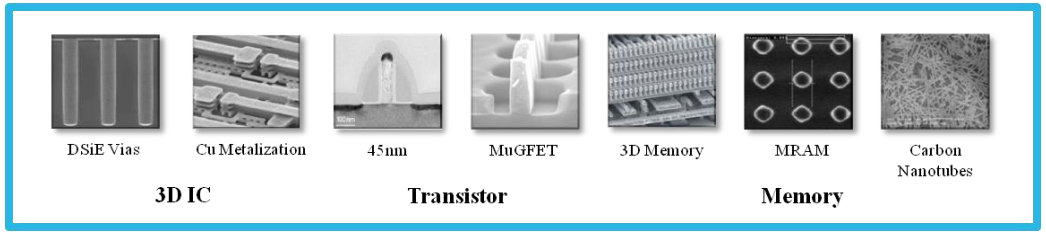
Internet Of Things

More Than Moore



GEORGIA TECH PRC





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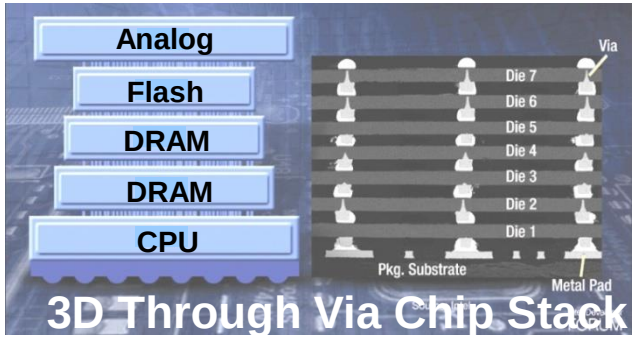
WHAT IS ADVANCED PACKAGING?

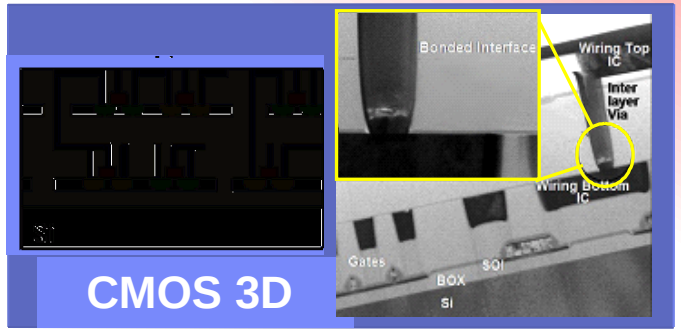
Span of Advanced Packaging

Packaging



IBM/Samsung

Wafer Fab



IBM

3D-ICs

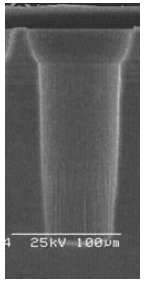
100-1,000,000/sqmm

1000-10M Interconnects/device

1s/sqmm

Peripheral I/O

- Flash, DRAM
- CMOS Sensors



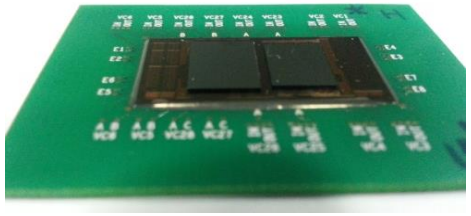
100,000,000s/sqmm

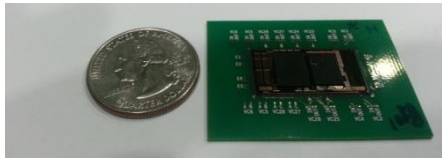
Transistor to Transistor

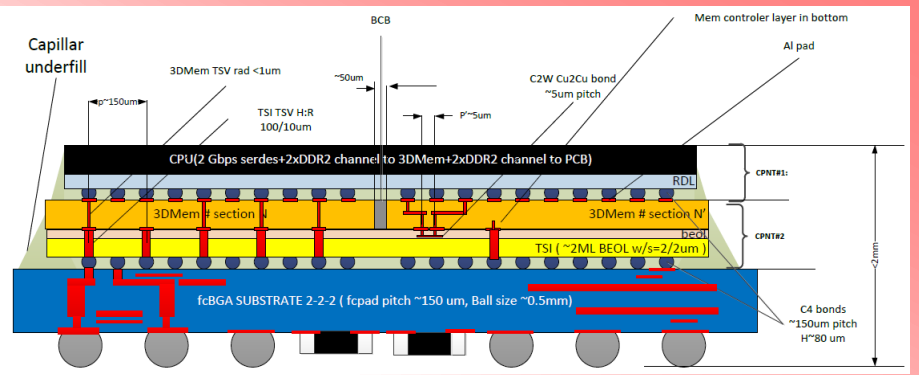
- Ultimate goal

Many Choices!

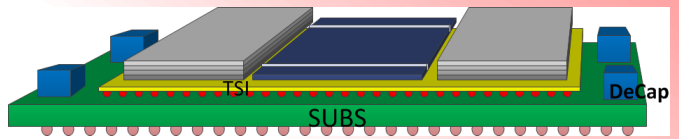
IME A-Star / Tezzaron Collaboration

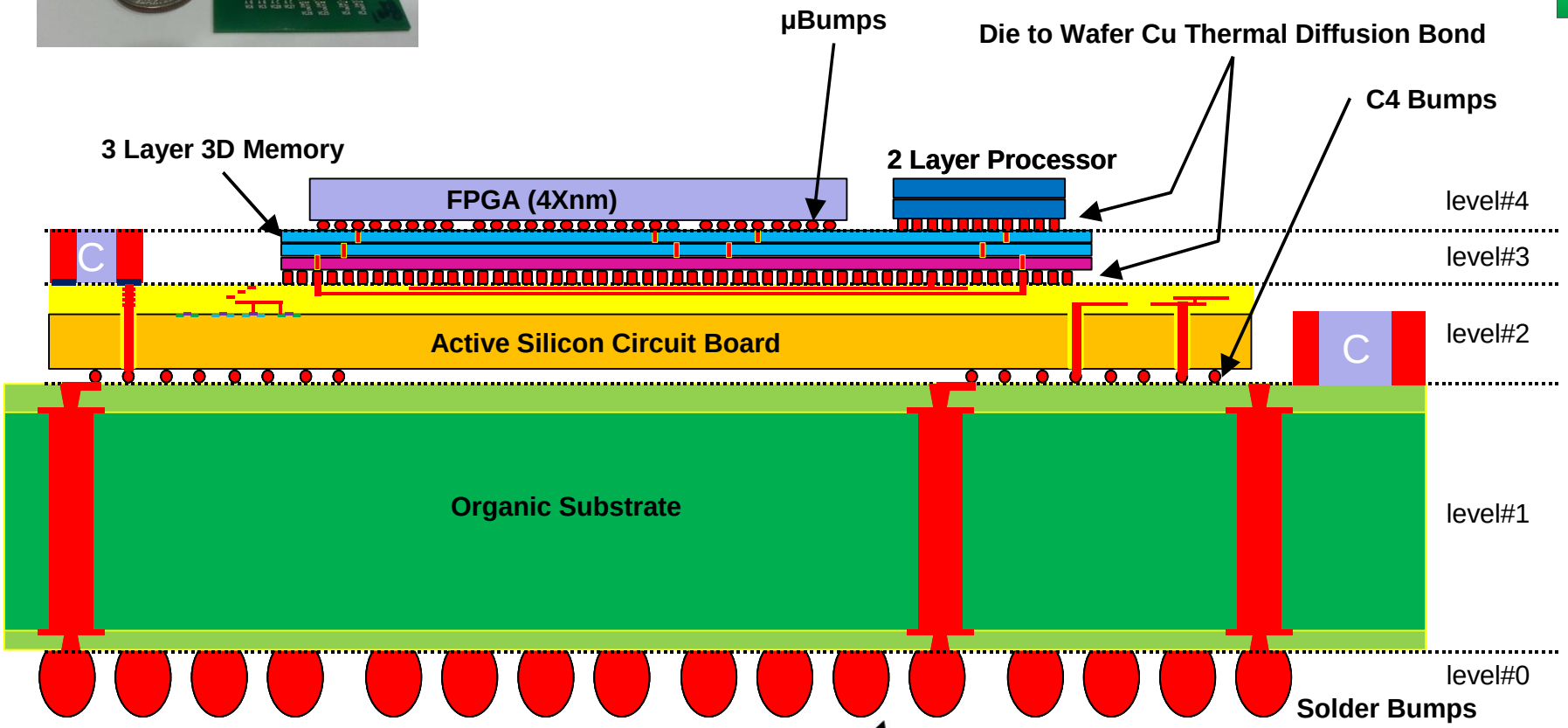






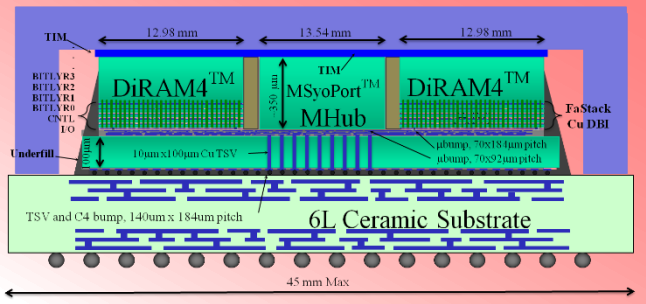
IME A-Star / Tezzaron Collaboration

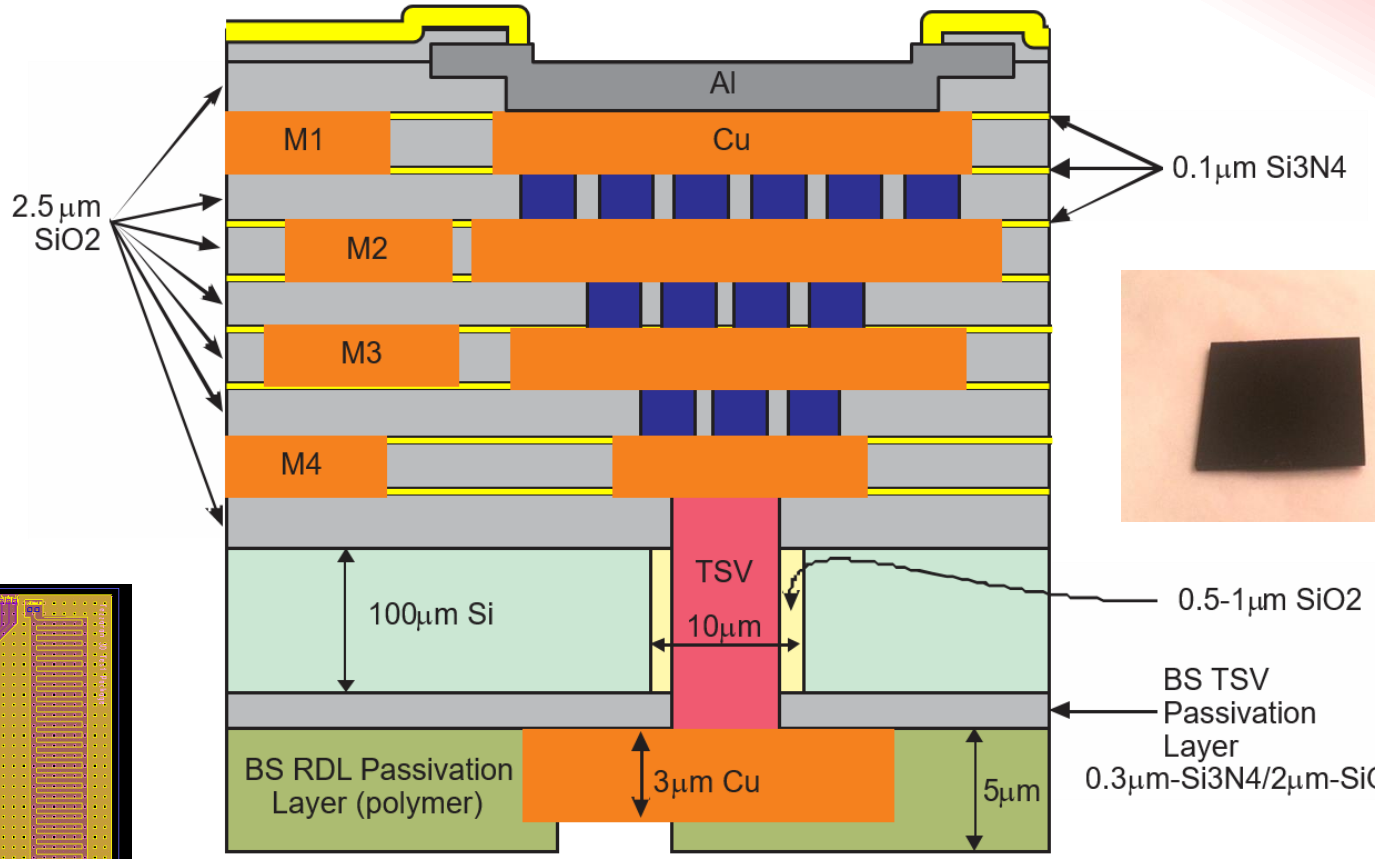


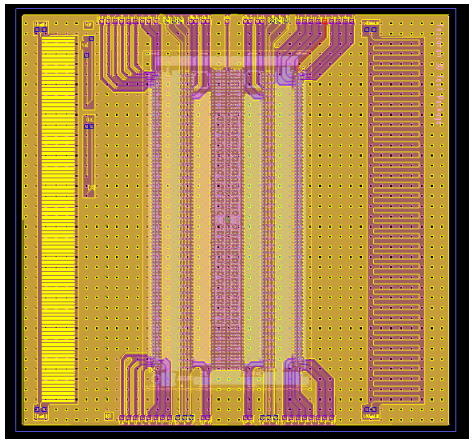


Si Interposers

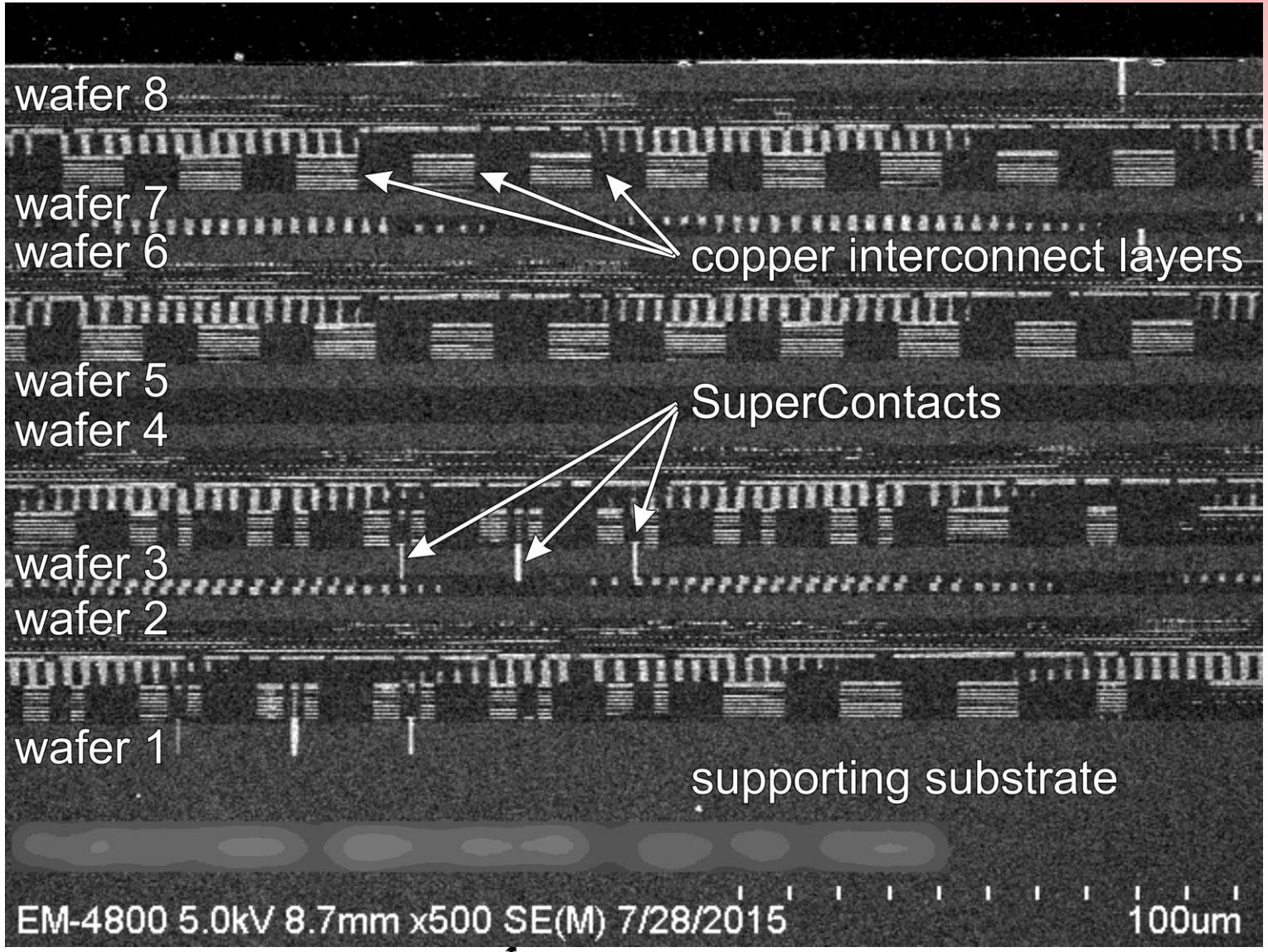
Bigger, Better, Faster
>50x50mm, Up to 6 layers, Lower R,C





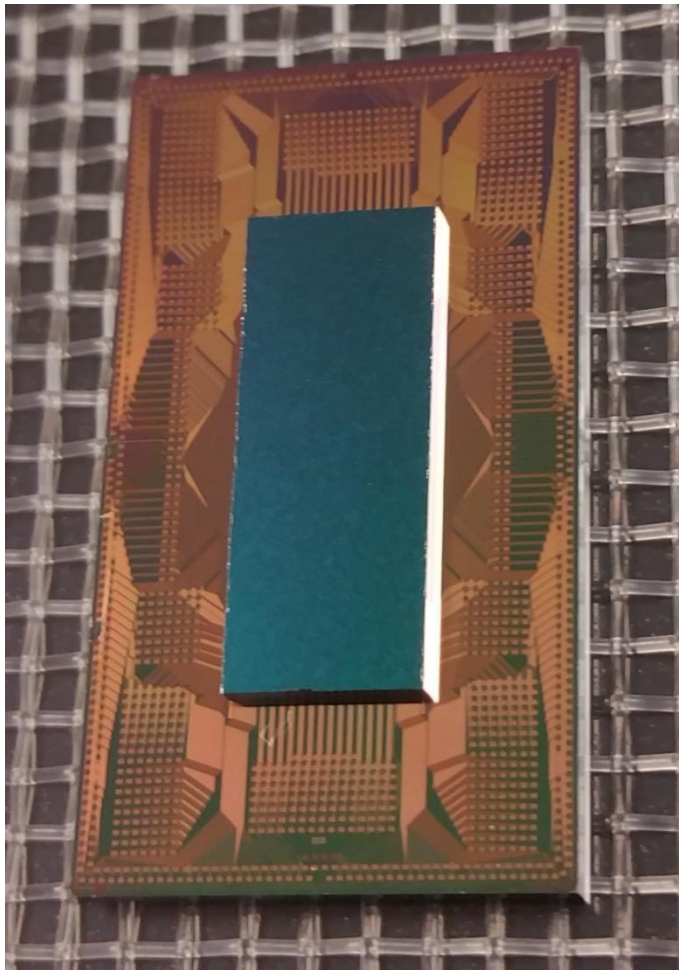


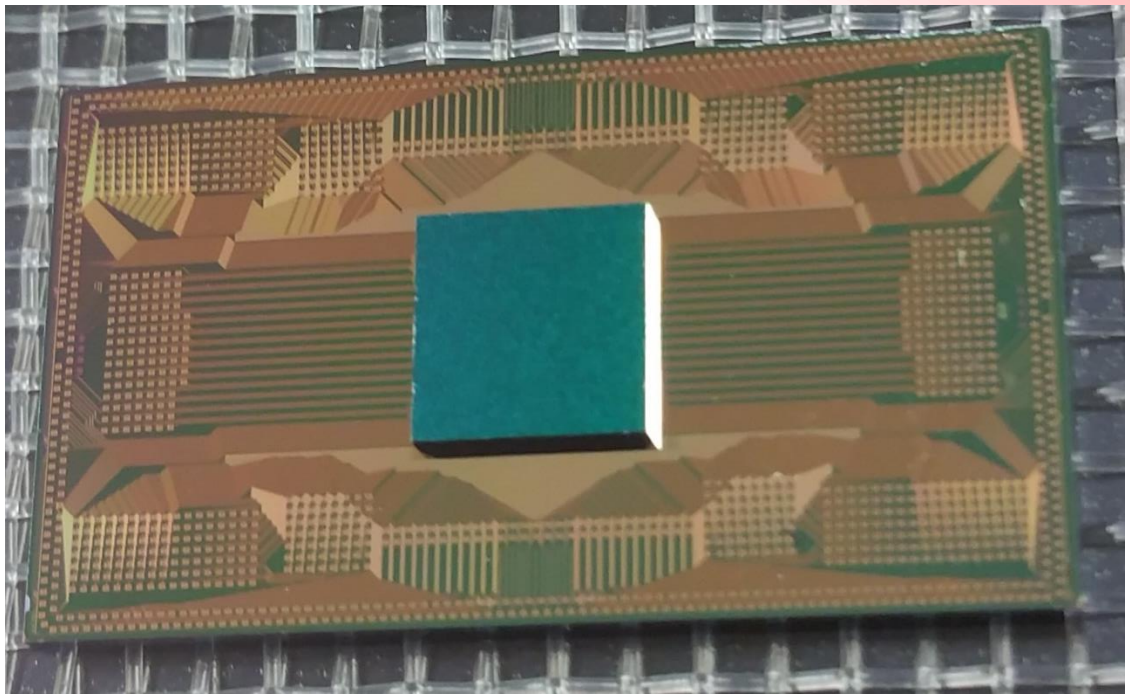
8 Layer Logic Stack



NHANCED SEMICONDUCTORS

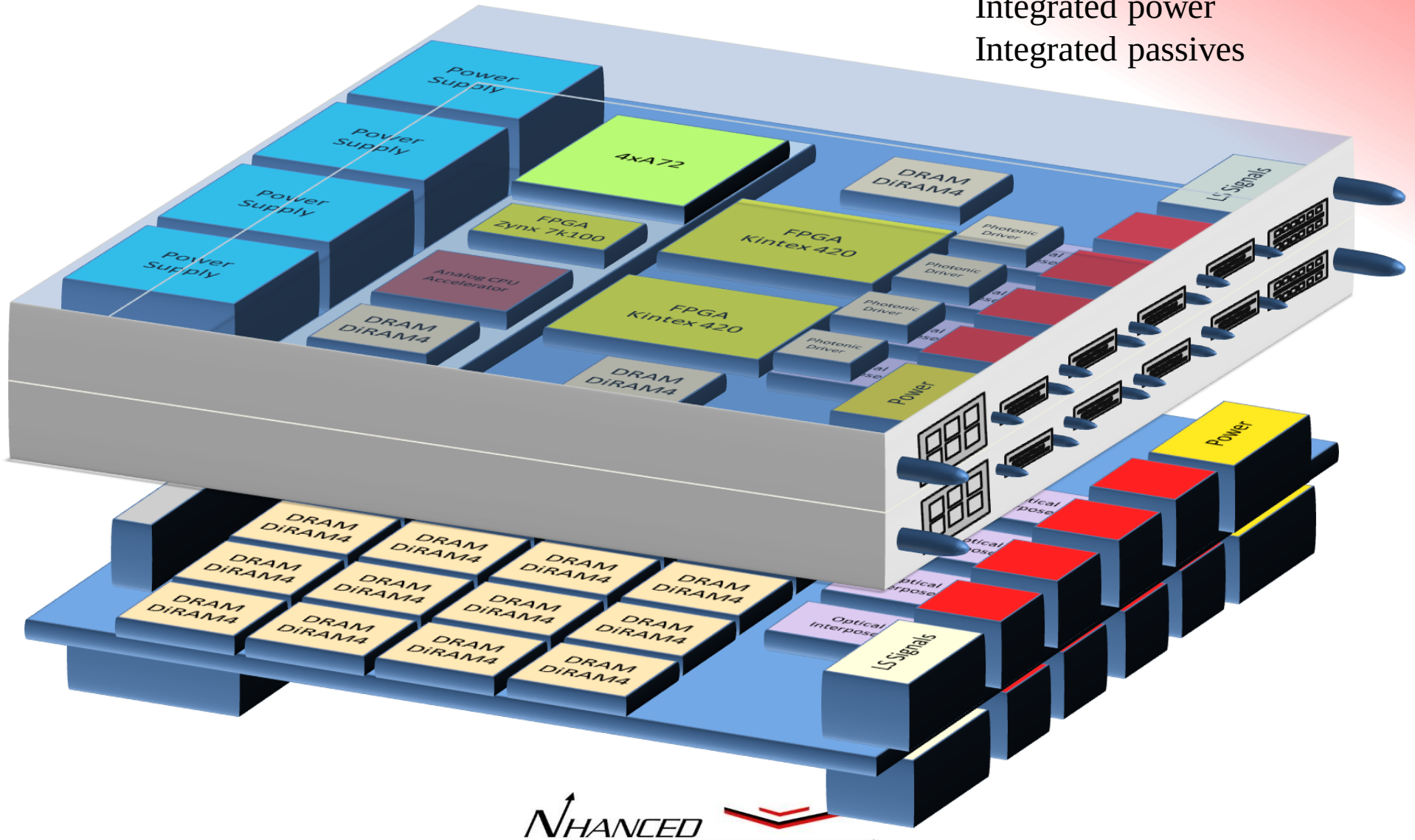
5.5D Systems





System Densification

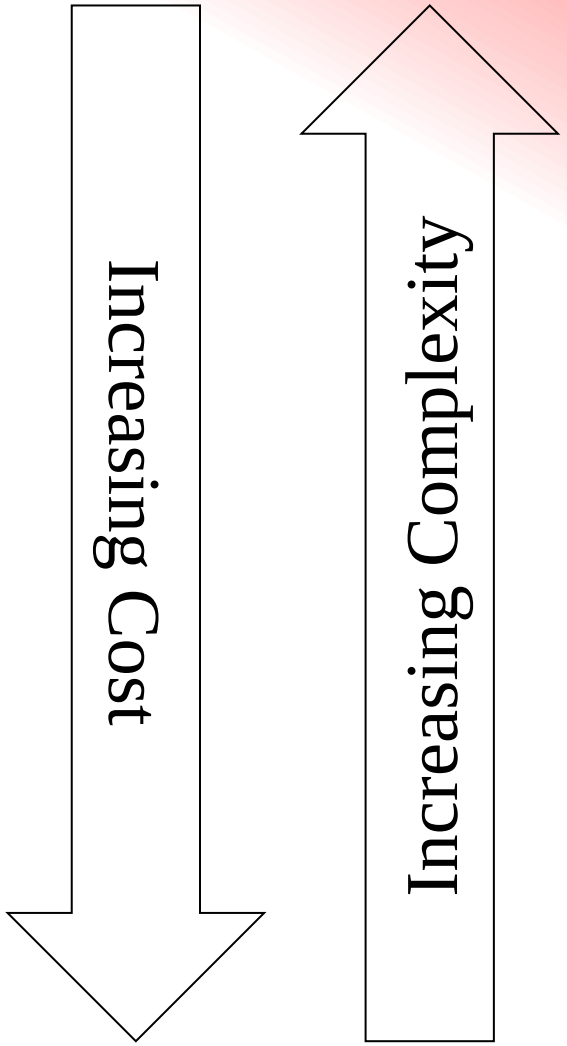
Integrated Photonics
2.5D
3D
Integrated power
Integrated passives



SOUNDS GREAT!
WHAT'S THE CATCH?

Choices

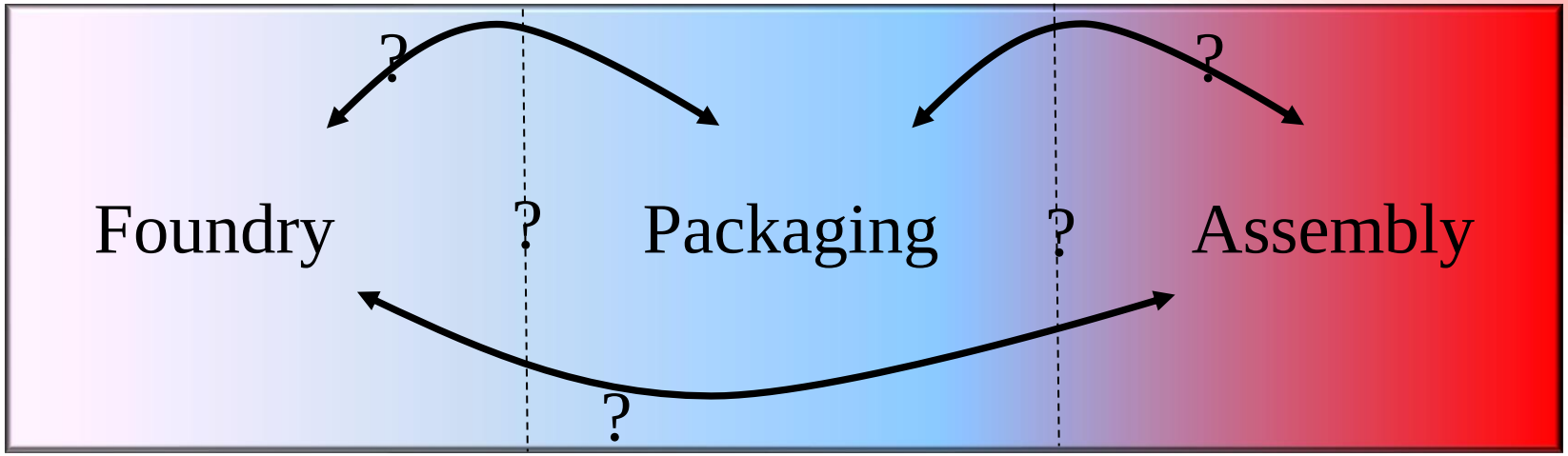
- Wafer-to-wafer / Monolithic 3D
  - Best cost structure
  - Highest density interconnect
  - Fab processes
    - A messy fab issues
      - Particles
      - Materials
      - Non-standard sizes
      - Novel materials
      - Novel processes
- Interposers
  - Mixed fab and packaging flow
  - Add TSVs
- Chip Stacking - POP
  - Limited interconnect
  - Cost



Materials Opportunities

- Silicon Interposers
  - 2-3um L/S/D
  - Rs and Cs
  - Active is the future
  - Handling & handoff
- Organics Interposers
  - 5-6 um
    - Litho limits
    - Material planarity limits
  - Great cost structure
  - CTE Challenges
  - Large substrate
- Glass Interposers
  - Large substrate

Mixing Fab, Packaging and Assembly



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Test what where when ?

Big hidden cost

Testing

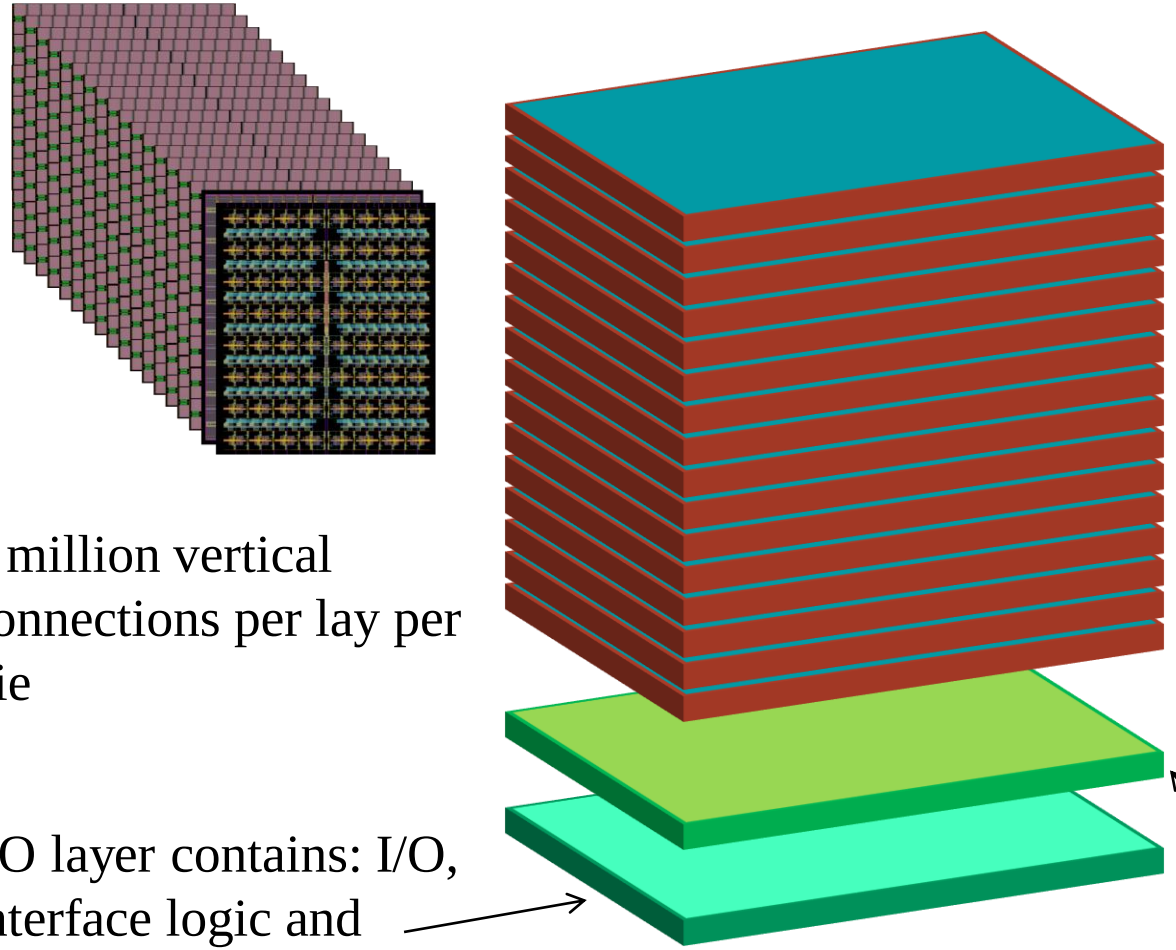
- Significant planning required
- Careful analysis of yield cost
- New methodologies
  - High I/O count requires self-test
  - Deep embedding requires more effort for visibility
  - At speed test alternatives
- Embedding memory has numerous test issues
  - Standard test interface required.
- Self-repair / Self-redundancy

Data Points

- The future is chiplets… or at least really sophisticated multi-die packaging
  - Highly customized assembly flow
  - Provides:
    - Product Flexibility
    - Faster time to market
    - Reuse
    - Enables cost effective low volume production

- We don't build enough of a given module type to get statistical reliability data
- We can't inspect the latest generation of assembly technologies for defects
- KGD really is KNB – Known Not Bad
  - Probably as good as it gets
- 2.5/3D solutions have lots of I/O
  - Hard (many times impossible) to test
  - Costly to test
- Die probing is more difficult than wafer or package testing
- Probing causes damage
  - Can have worse effects than simply doing blind assembly

“Dis-Integrated” 3D Memory



DRAM layers
4xnm node

2 million vertical connections per lay per die

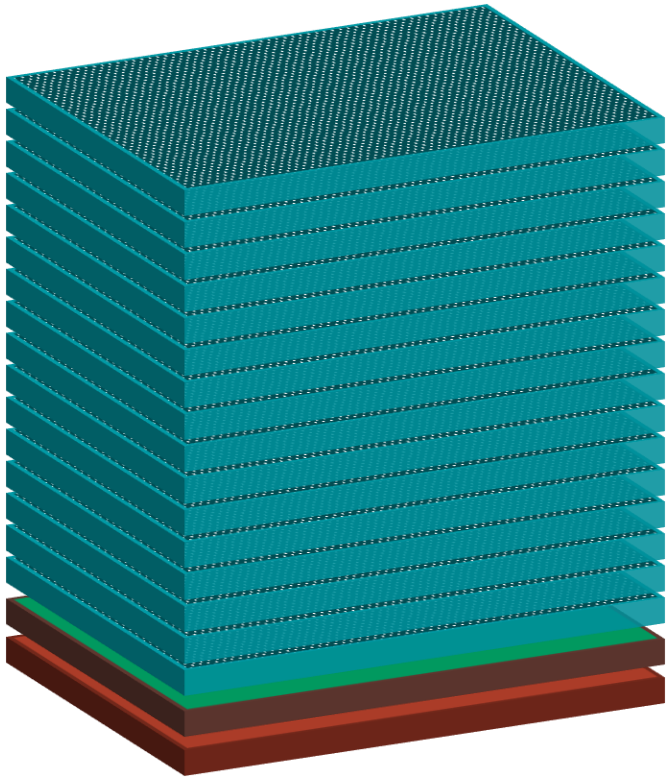
I/O layer contains: I/O, interface logic and R&R control CPU. 65nm node

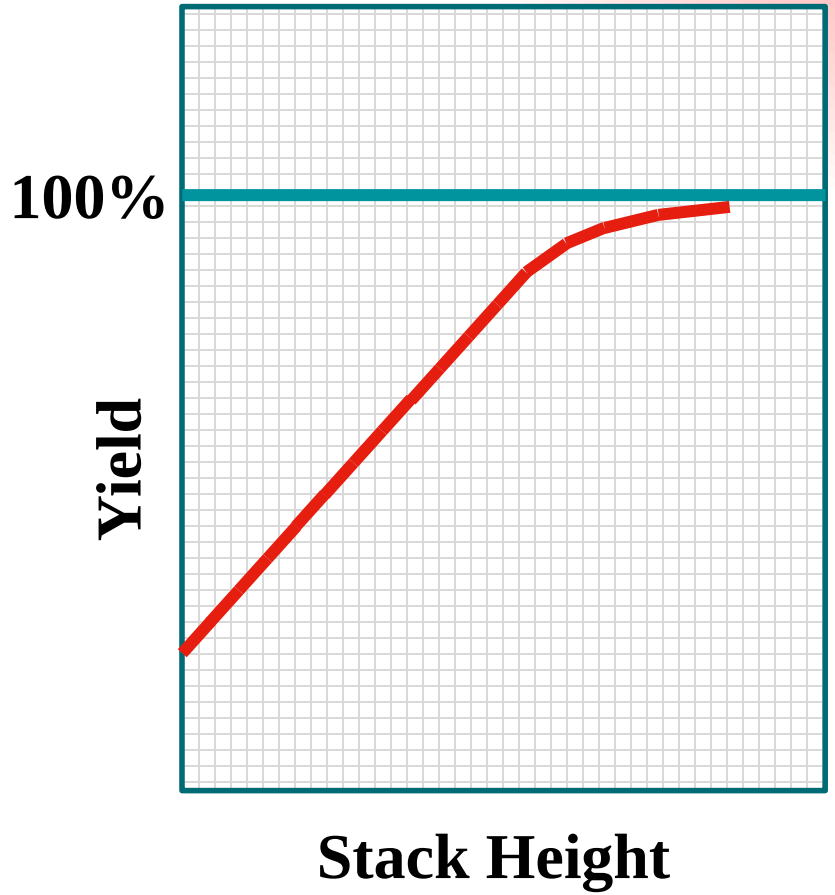
Controller layer contains: sense amps, CAMs, row/column decodes and test engines. 40nm node

Better yielding than 2D equivalent!

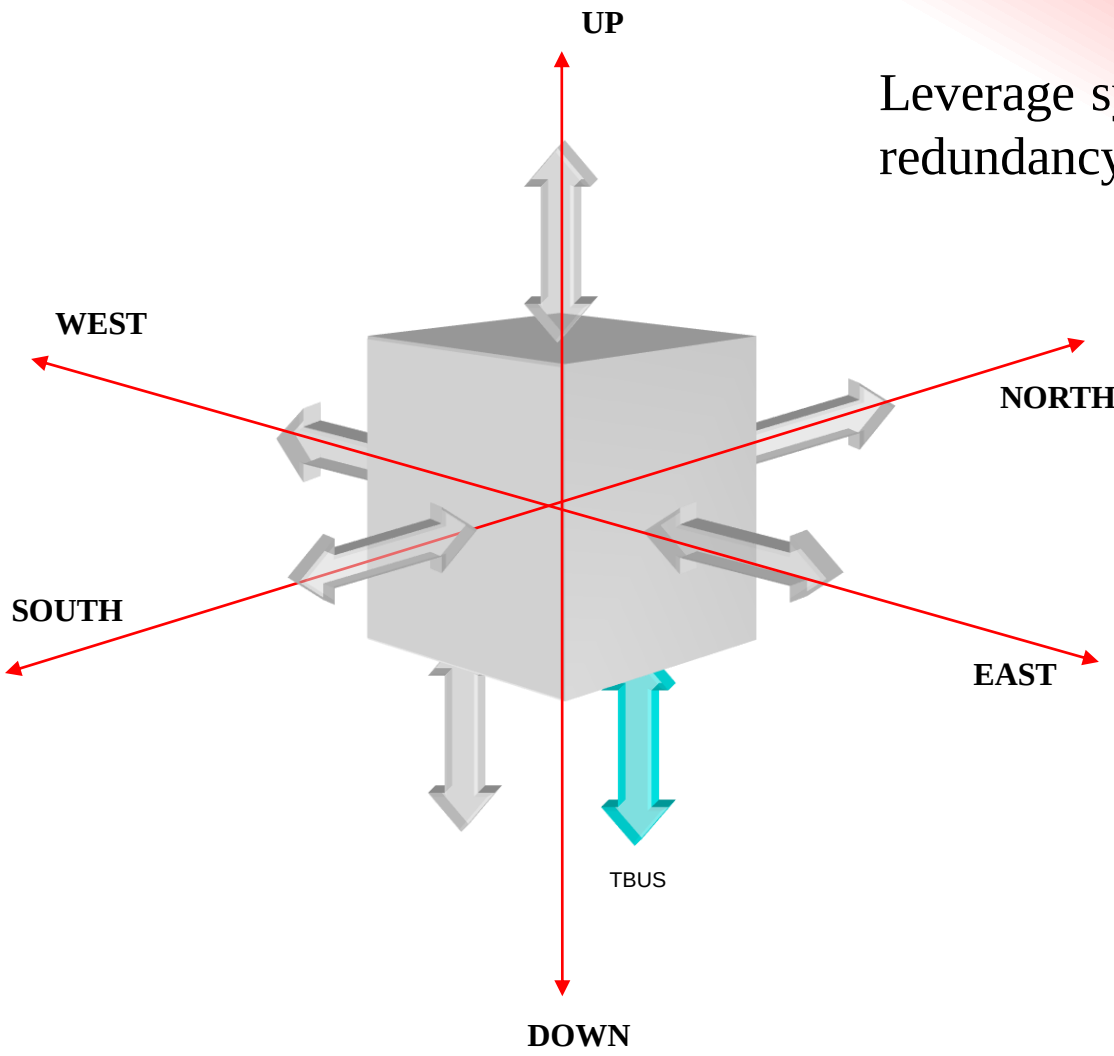
NHANCED SEMICONDUCTORS

Bi-STAR Repair Improves Yield



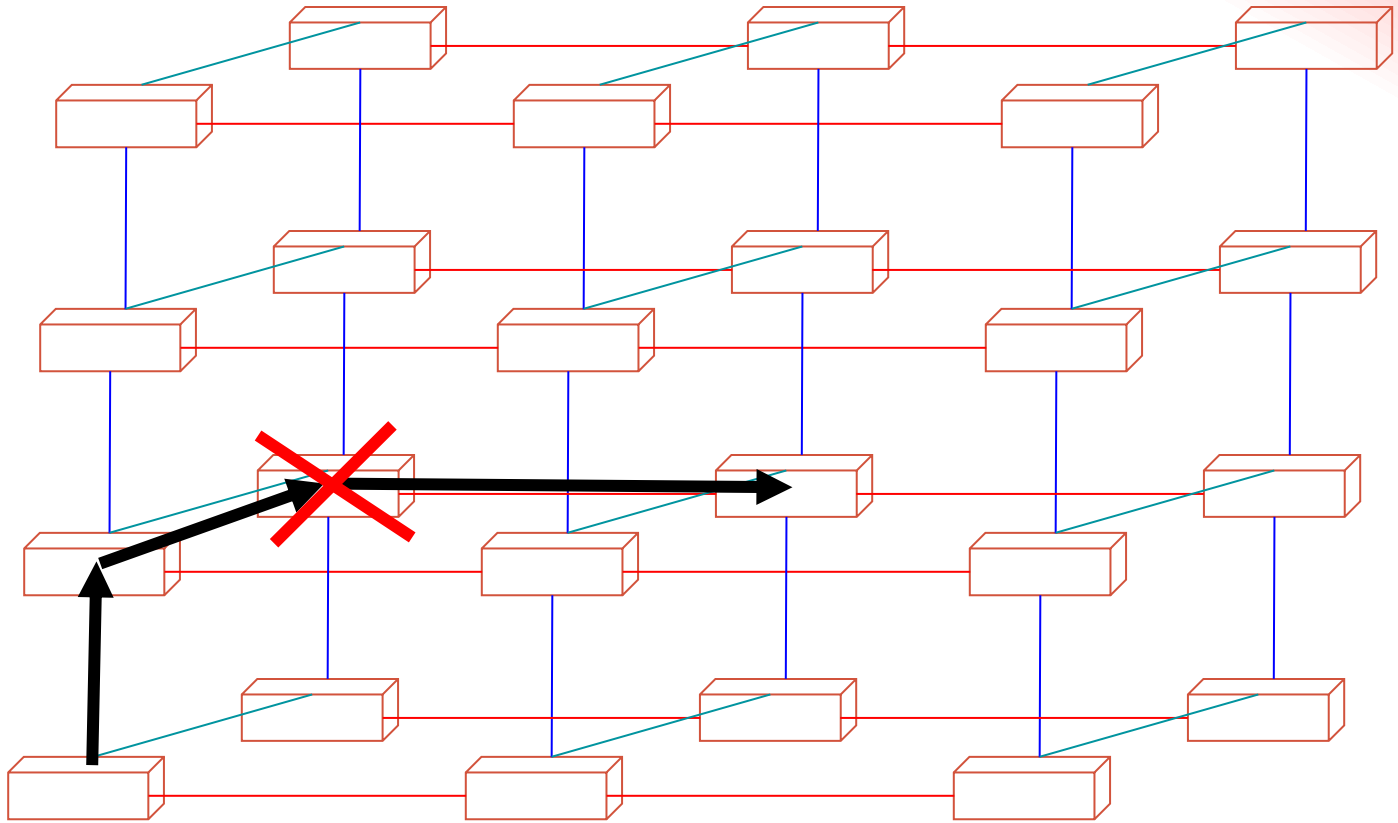


3D-Routing Node (NOC)

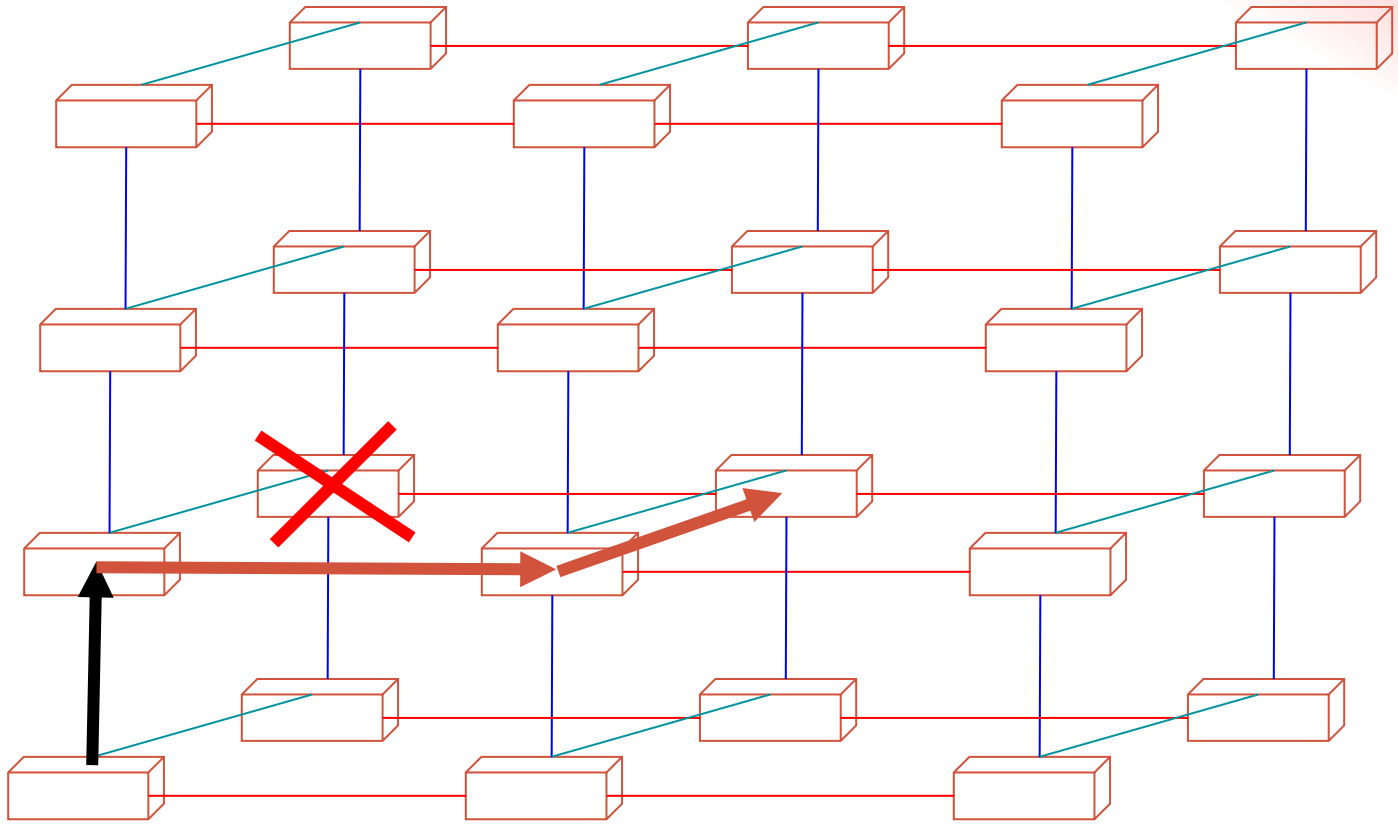


Leverage system level like redundancy schemes

3D NOC Interconnect



3D NOC Interconnect



Extensions of R&R

- Spare Processors
  - Virtually all advanced processors today
- Smart Interposers
  - Programmable routing
  - Intelligent power control
- FPGA Repair Kits
  - A logical extension of current chip repair kits
- Redundant I/O
  - Like HBM devices

NHANCED SEMICONDUCTORS

RELIABILITY

How Do We Know If This Device Is Reliable?

- Hypothesis:
  - If we can measure the “Quality” of the assembly, we can infer the Reliability of the specific device tested.

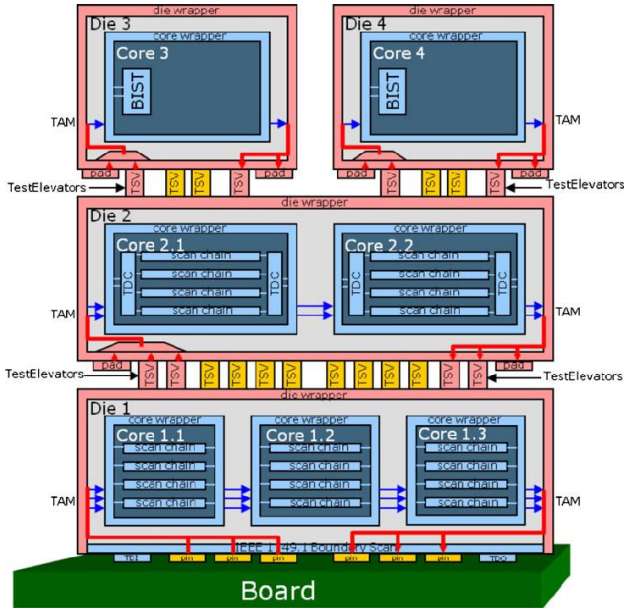
A Plan

- Create universal test structures that are accessed via JTAG 1394 (IEEE1500).
- Measure R's and C's of alignment structures and interconnects using 1149.4 analog JTAG extension.
  - Electronic Verniers
  - Via Chains
  - Temperature sensors
  - PCM data
- Create ala carte test plans that bracket what tests are required based on the module content and assembly technologies employed
- Build a database of historical evidence to correlate actual reliability to measured "Quality" data
  - Starting with test devices that are built to validate the premise

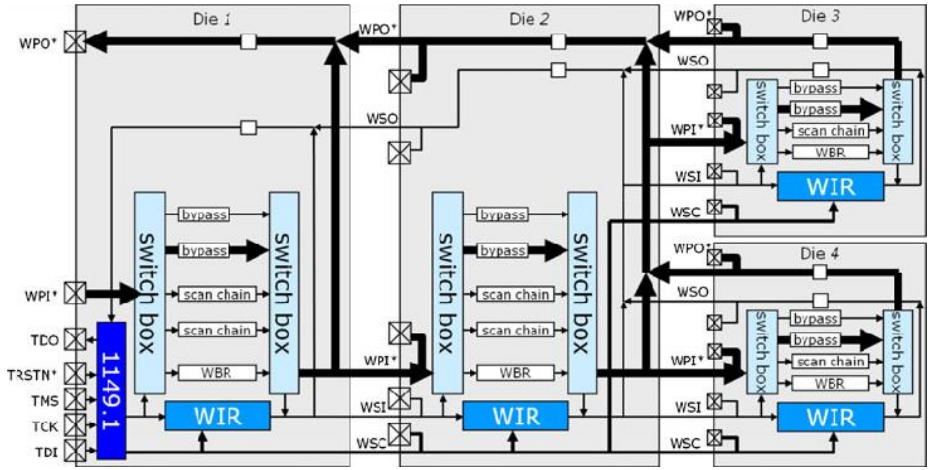
One Slide:

Use Standardized DFT + 2.5/3D PCM methods to test Quality and derive Reliability
Use repair and redundancy to create KGD and obtain yield.

Images from: A DFT Architecture for 3D-SICs Based on a Standardizable Die Wrapper; Erik Jan Marinissen et al



Physical



Logical

IEEE 1500 is well defined 2.5/3D DFT starting point building on 1394 standard. Plan is to add 1149.4 analog features targeting device manufacturing integrity.

Augmented JTAG based on IEEE 1500: Add alignment sensing, 3D interconnect R/C measurement, power, temperature …
System level test, configuration, repair and validation
Objective is to “prove” specific device quality and improve reliability data.