Systematic Identification of Key Design Factors for Chiplet Eco System Enabling

Thomas To, Ph.D., AMD Fellow
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Speaker

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Thomas is an AMD Fellow focusing on System Memory & IO Platform Architecture Development. Prior to AMD's acquisition of Xilinx, Thomas was a Distinguished Engineer in System Memory Signal Integrity group. Before joining Xilinx, Thomas was a principal engineer in NVIDIA Advanced Technology Group focused on highspeed circuits & system channel designs. Before NVIDIA, Thomas worked for Intel for more than 16 years covered and led many different types of system memory IO development. Thomas received his PhD degree in Electrical Engineering from the Ohio State University in 1995 & he is the inventor of over 38 patents in the fields of mixed signal IO circuits and system memory configurations as well as high speed clocking for highspeed memory designs.

Abstract

With so many features of interest at play in computing, adding all the features of interest in the most advanced silicon process node to meet the ever-growing computing demand is very challenging. Chiplet implementation uses a selection of modular dies, referred to as chiplets, to provide a heterogeneous integration approach and to offer best-in-class feature combination. However, identifying the key system design factors to enable a successful system is complicated.

In this talk, a design factor sensitivity methodology will be presented. Chiplet system channel jitter is used as the desired optimized result and the impacts of different design factors on the result are examined. Based on a behavior jitter model, this method first correlates the model to an actual measurement of a High Bandwidth Memory (HBM) system.

The model is then extended to represent different input factors for the system output data path jitter. These input factors include the multiple supply power frequencies, their corresponding noise amplitudes, signal transition slew rate, as well as channel routing configurations such as different ground signal configurations. A set of output jitter response surface model, with different power tone frequencies and noise amplitudes, is then developed, with an optimal channel interconnect. The response surface model provides a contour to identify critical input parameters such that system platform designers can evaluate the effects of multiple input factor and their interactions. This approach allows for a holistic consideration for optimizations & specification.

Outline

- *Background*
  - *ASIC Development Costs and Return of Investment Trends*
  - *Overview of Chiplet Integration as a Solution & its Challenges*
- *Chiplet Connection*
  - *What are the key design factors?*
  - *How to determine these key design factors for development design & for specification?*
- *Design Factors (Specification Parameters) Sensitivity Analysis*
  - *Unified System Jitter Model for Design Factor Gradient Quantification.*
- *A Case Study: Performance Evaluation based on Input Design Factor Sensitivity Results*
- *Summary and Conclusions*

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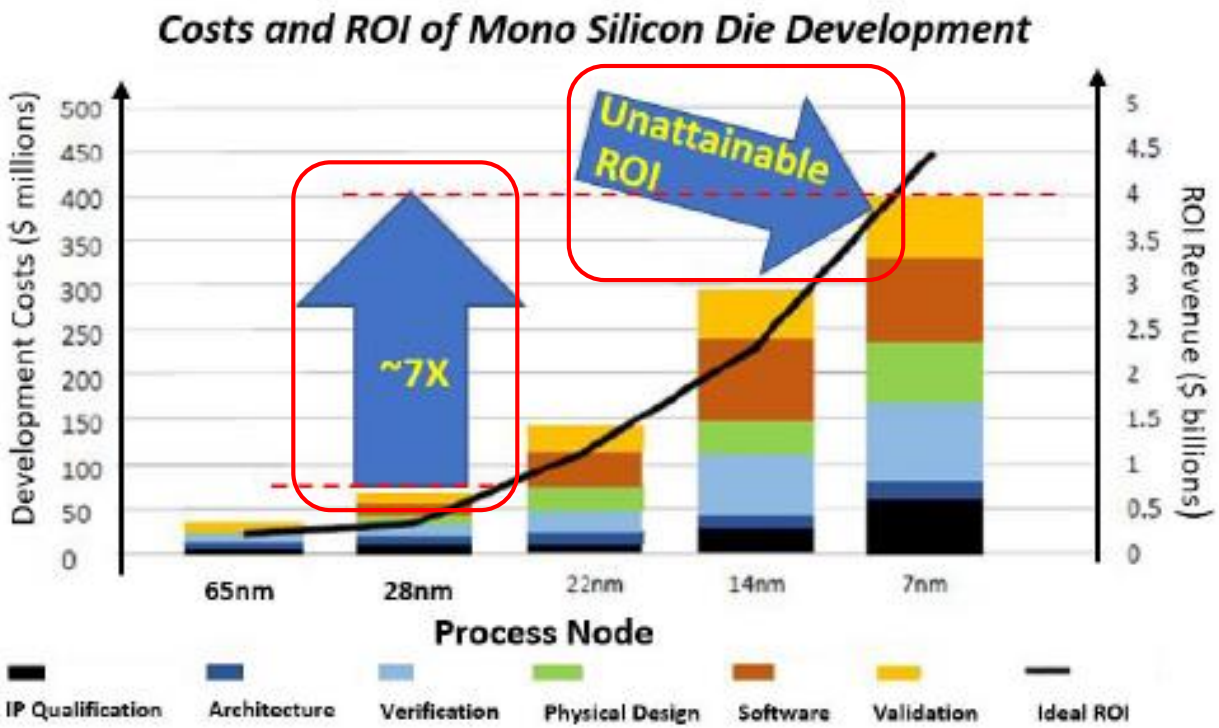
ASIC Development Costs and Returns of Investment Comparison

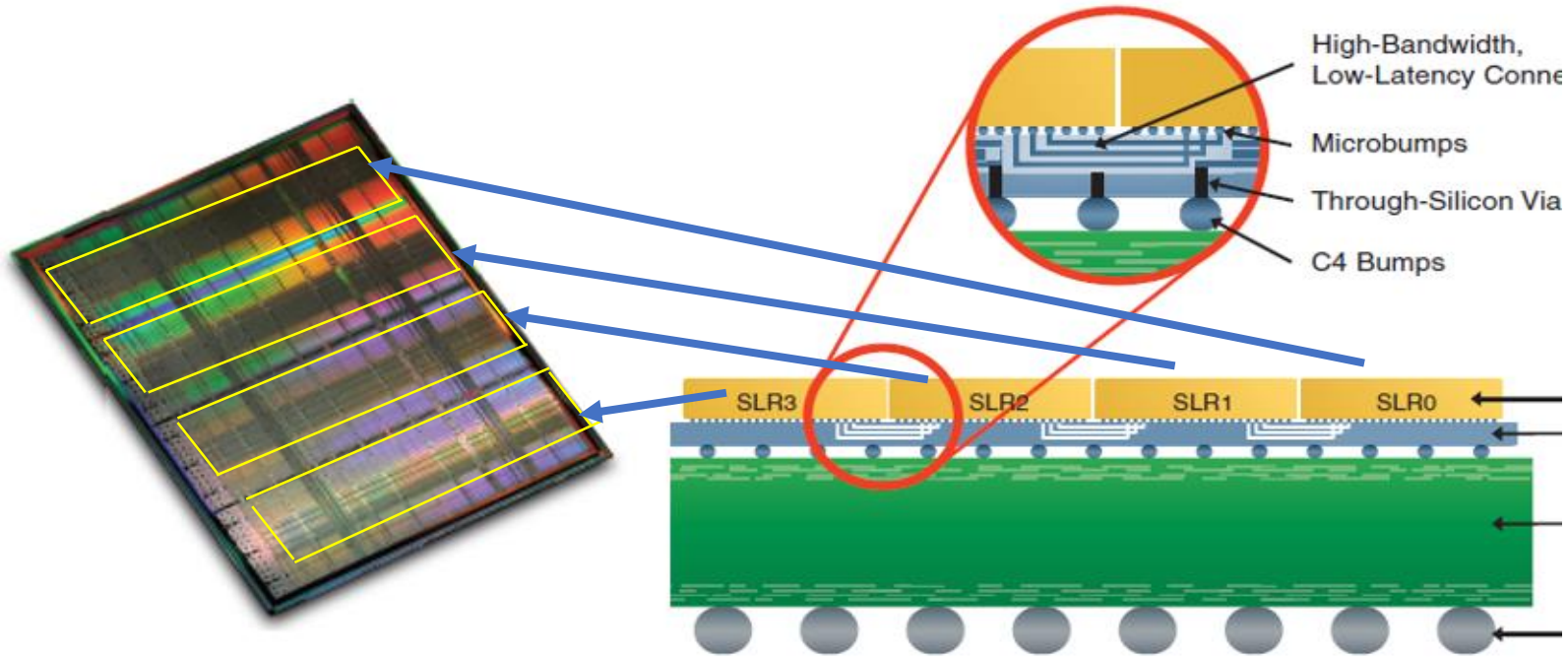


→ *The cost of monolithic IC integration and scaling has skyrocketed in recent years as the process node shrinks.*

→ *The Return of Investment of monolithic IC compared to its development cost is unattainable for process node of 7nm and beyond.*

→ *Adding all the features of interest in one IC and one process node, increases complexity and cost.*

Chiplet Implementation Example

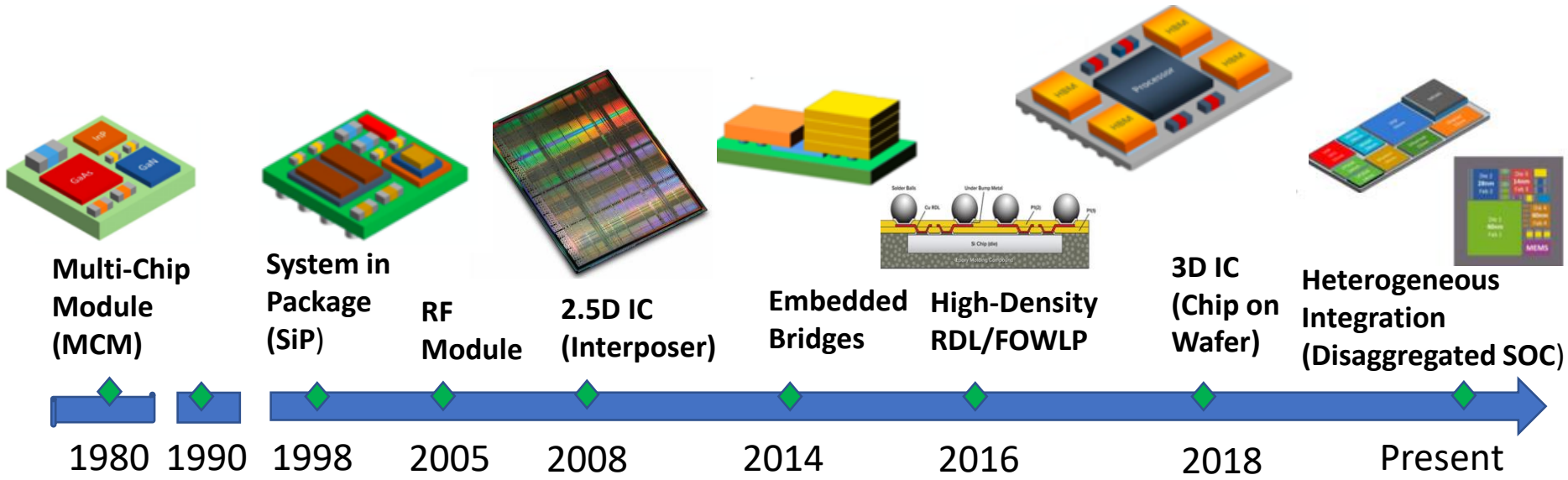


→*Chiplet implementation uses a selection of modular dies called chiplets.*

→*Chiplets may have different functions and can be developed on different process node.*

→*Mix and match of chiplets can meet the feature and performance needs.*

Chiplet Integration TimeLine



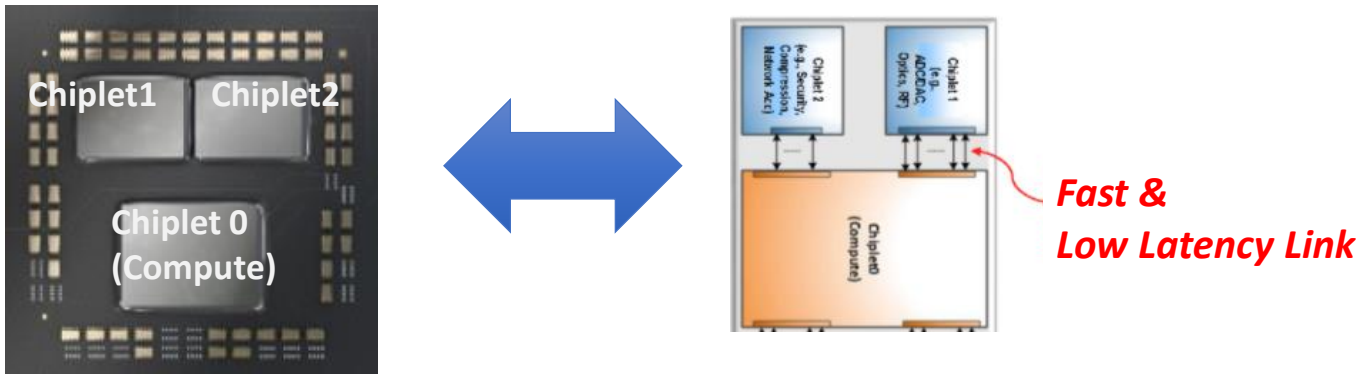
→*Chip to Chip integration has been continuously evolving and accelerating the revolution.*

→*More Development Challenges from many different aspects, such as*

→*Combining 3rd party design & Optimize Completed System Holistically.*

→*How to identify and quantify key design factors that matter ?*

Chiplet Connection/ Integration Challenges



High Speed/Bandwidth Data Transmission between the chiplets → Low Latency & High Throughput

→ Chiplets can be developed by One or Multiple Companies.

→ Optimized System Integration requires Identification of Critical Design Factors.

A Unified Chiplet Interconnect Jitter Analysis Approach:-

→ Combined System Jitter from Tx to Rx serves as the Figure of Performance Merit.

→ Model is based on analytical expression of power supply induced jitter and jitter accumulation along the path.

→ The sensitivity of each Design Factors will be quantified and compared.

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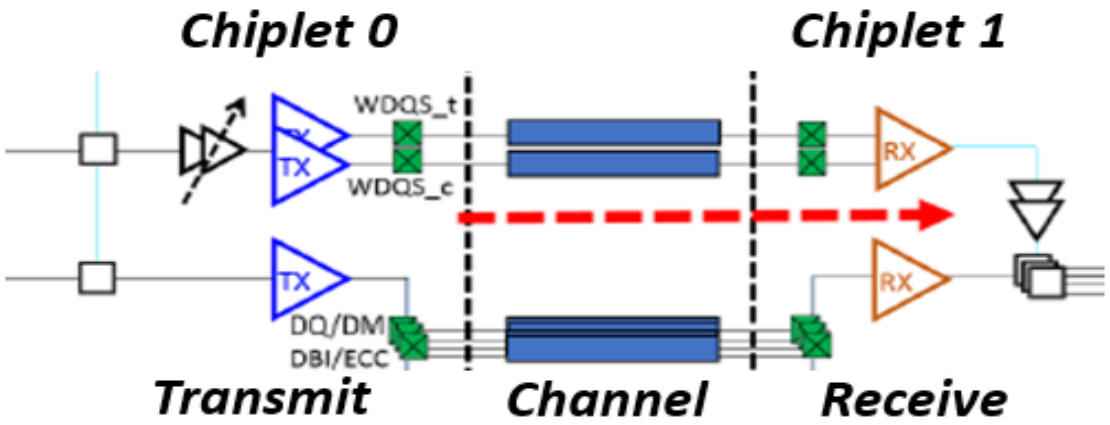
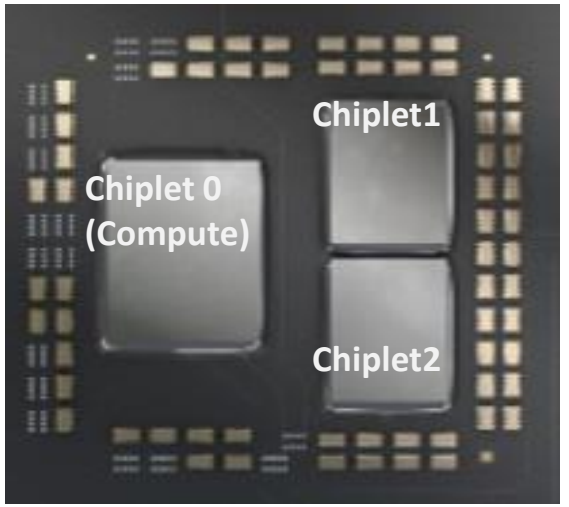
Typical Chiplet Connection



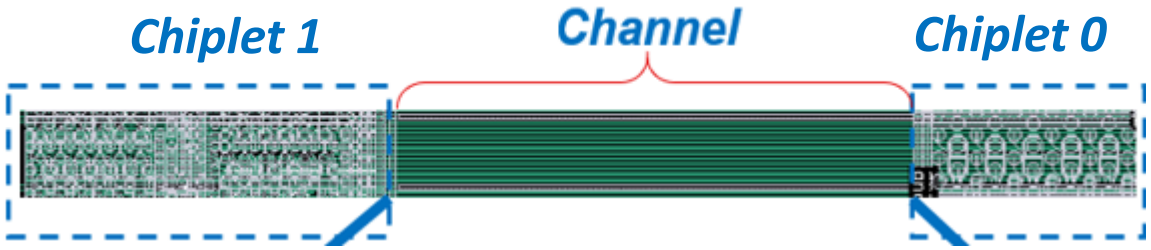


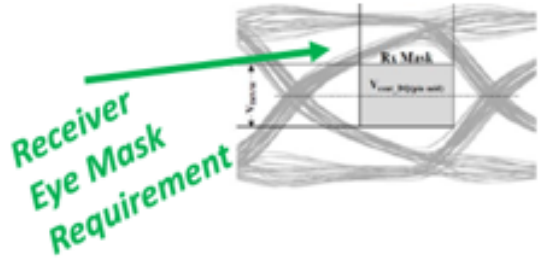
→*Chiplet Connection Transmit Speed ties to how to control link Jitter.*

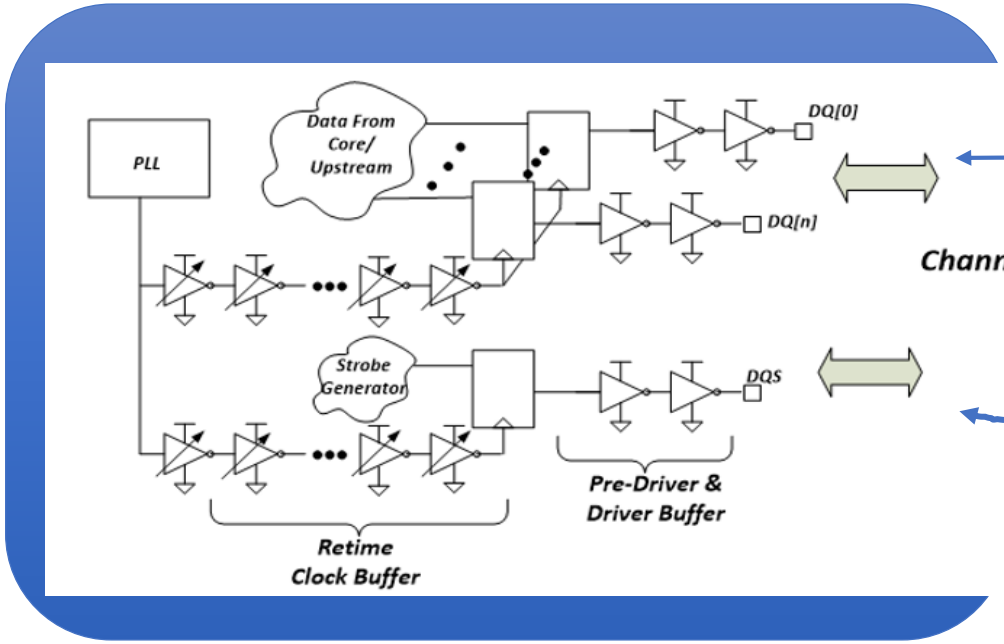
→*Jitter at each stage is integrated with the previous stage jitter as input.*

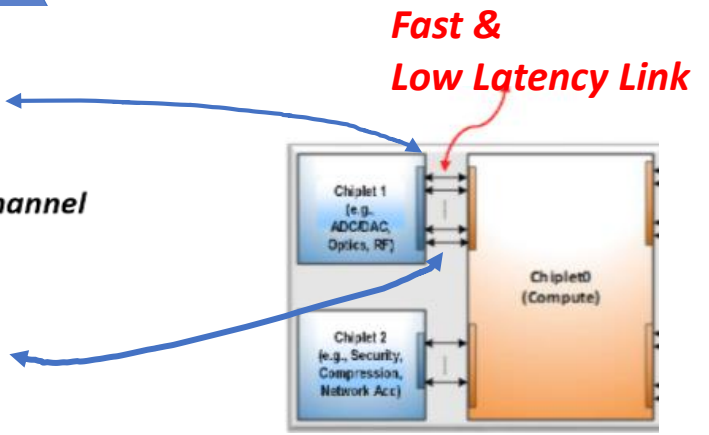
→*Jitter output is an Accumulative Jitter number.*

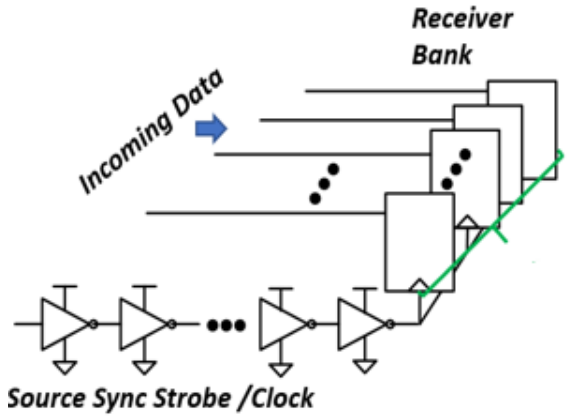
Chiplet Connection Link Factors











→ *Data Transmit has Multiple Stages of Induced Jitter & Accumulation from end to end.*

→ *Jitter has many underlining contributed factors such as power noise etc.*

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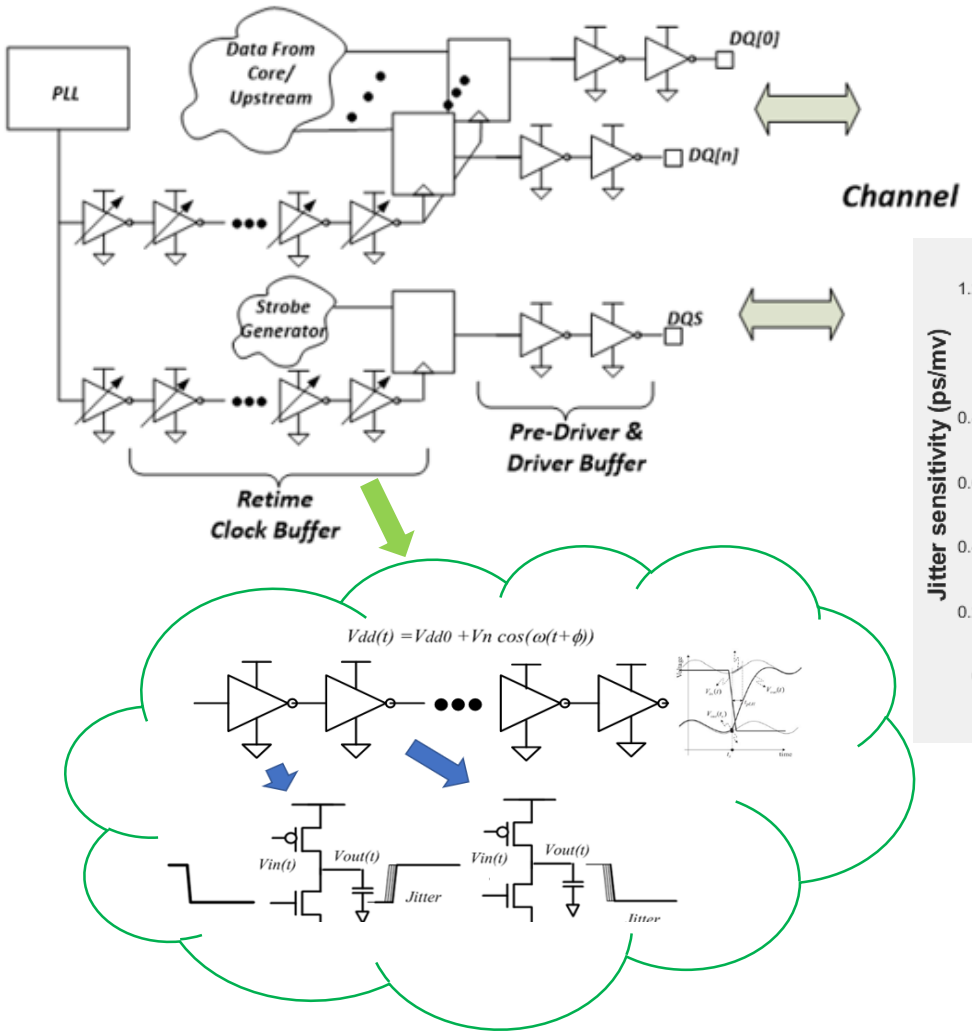
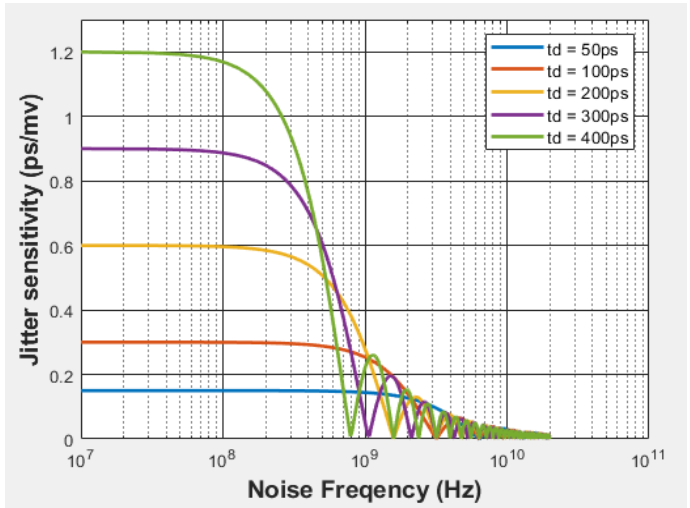
Power Noise to Jitter Transfer

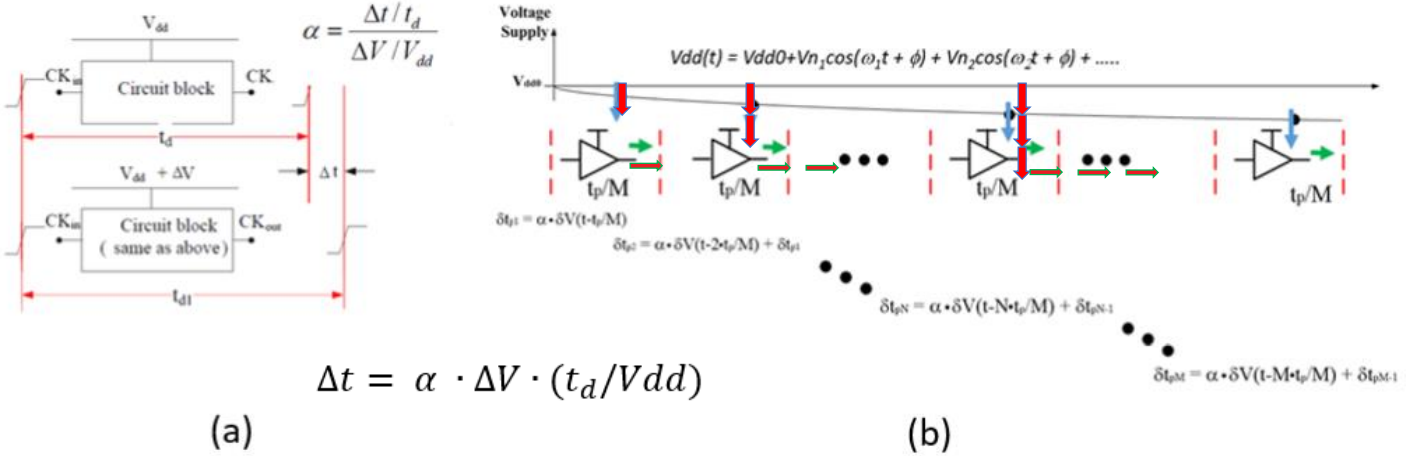




- → *Relatively constant jitter sensitivity below a certain noise frequency.*
- → *Above knee frequency the response of buffer is not fast enough.*
- → *A longer delay clock buffer has higher jitter sensitivity.*

- → *Noise Tone Frequencies, Noise Tone Amplitudes, Buffer Delay and Process Characteristic are the Critical Factors.*

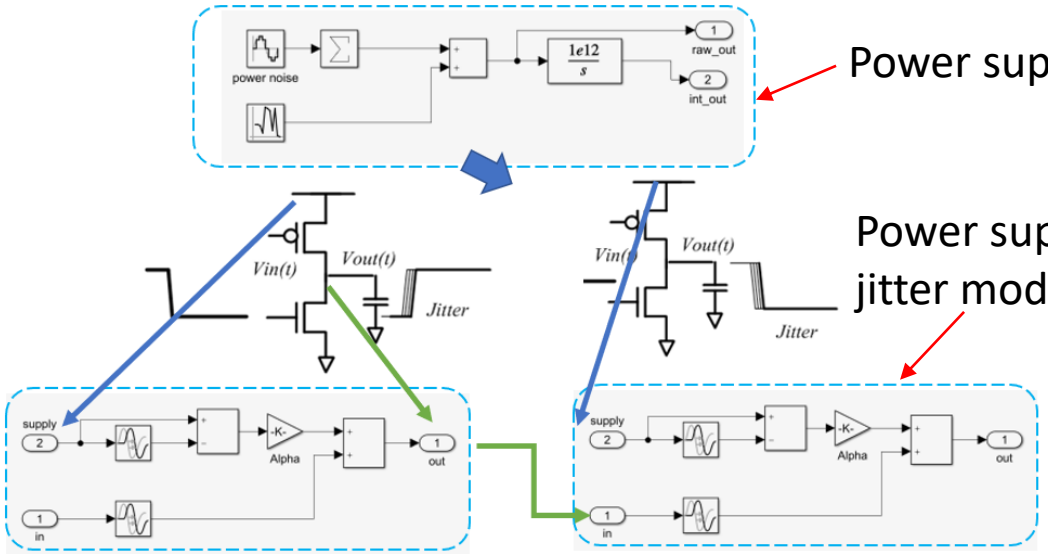
Power Noise Induced Jitter & Accumulation



$$\Delta t = \alpha \cdot \Delta V \cdot (t_d / Vdd)$$

(a) (b)

→ *Power Noise Modulates the Buffer Delay.*
→ *Each Stage experiences different Noise and will induce Jitter accordingly.*
→ *Each Stage will also accumulate Jitter.*

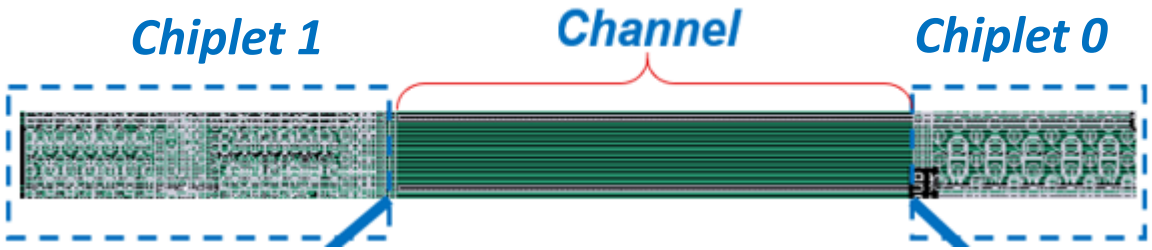


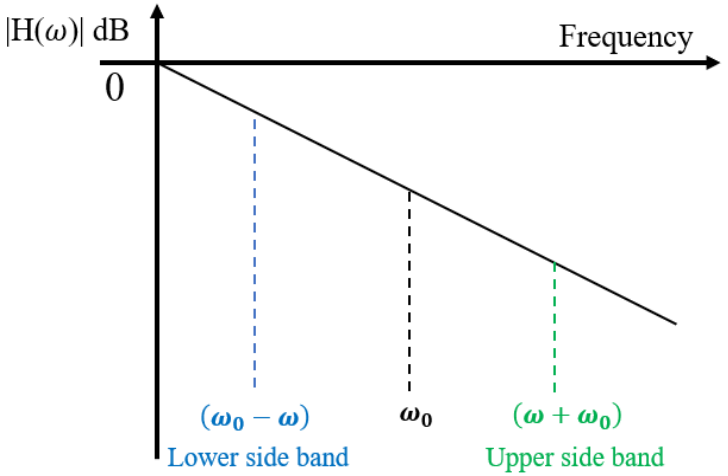
Power supply noise model

Power supply induced jitter model

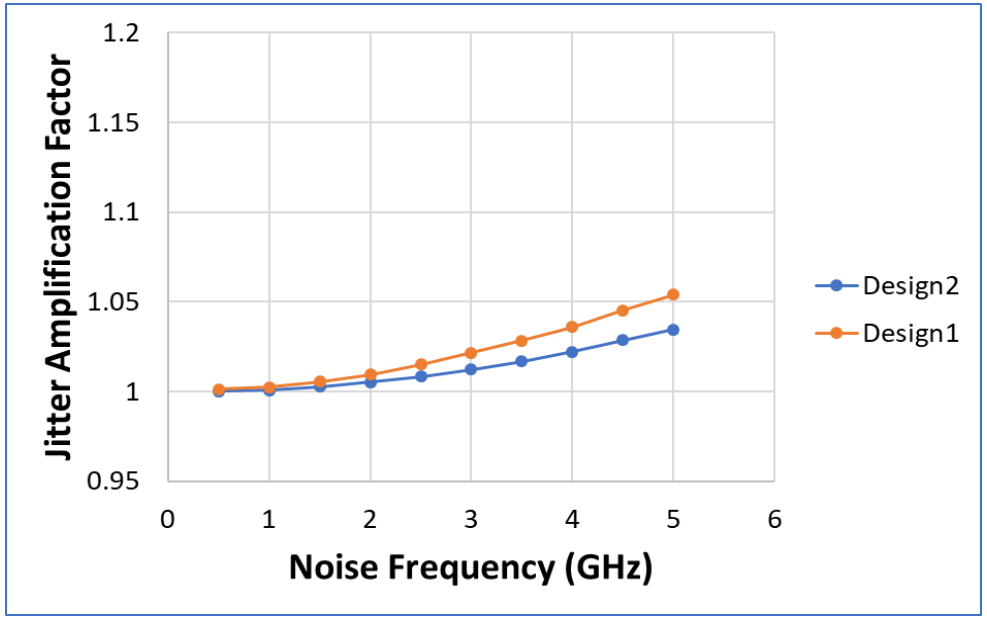
→ *A First Stage Buffer with Power induced Jitter model.*
→ *Power noise can be modeled with different Noise Frequencies and Amplitudes.*
→ *Jitter of first stage is added to next stage.*

Channel Jitter Amplification





$$F_{SJ}(\omega) = \frac{1}{2}\left|\frac{H(\omega+\omega_0)}{H(\omega_0)} + \frac{H(\omega-\omega_0)}{H(-\omega_0)}\right|$$



→ *Transfer function of a Lossy Channel decays with Frequency.*

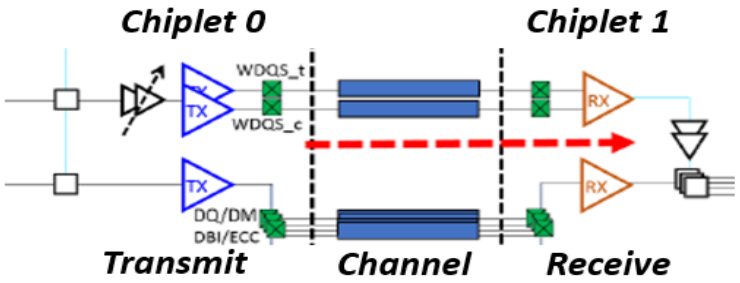
→ *Jitter passing through a Lossy Channel amplifies due to higher Jitter Attenuation at Higher Sideband.*

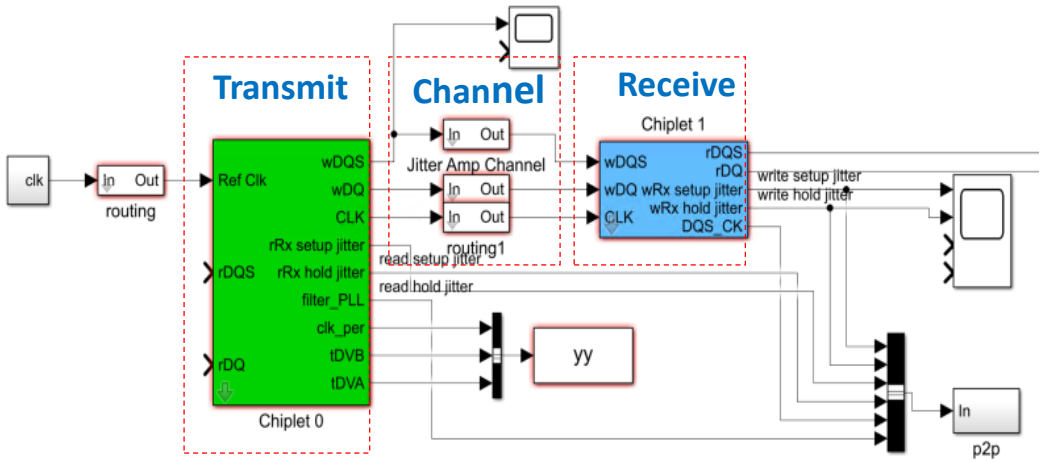
→ *Design1 is a Silicon Interposer channel.*

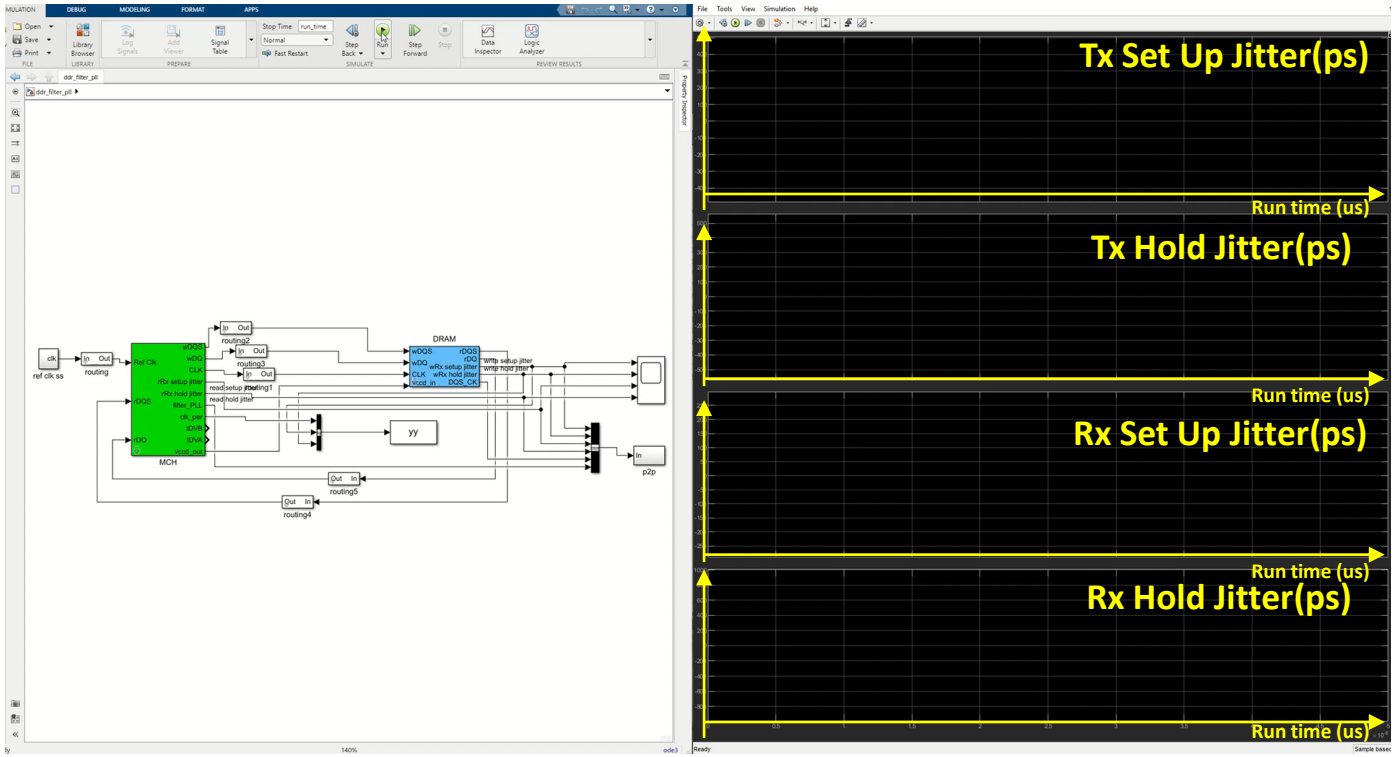
→ *Design2 is an InFO media Channel.*

→ *Interconnect Choice shows Different Characteristics*

Combined System Jitter Model



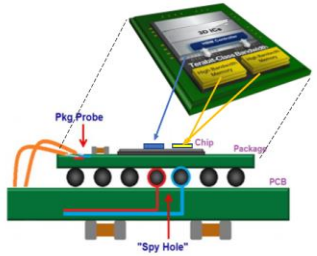




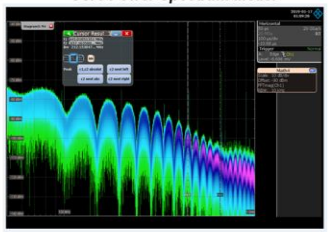
→*Unified model is used to create response surface model using critical input factors.*

→*The sensitivity of gradient of each input factor is studied and optimized.*

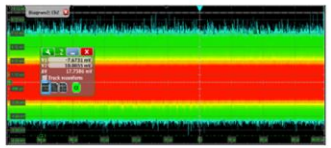
Unified Jitter Model Correlation

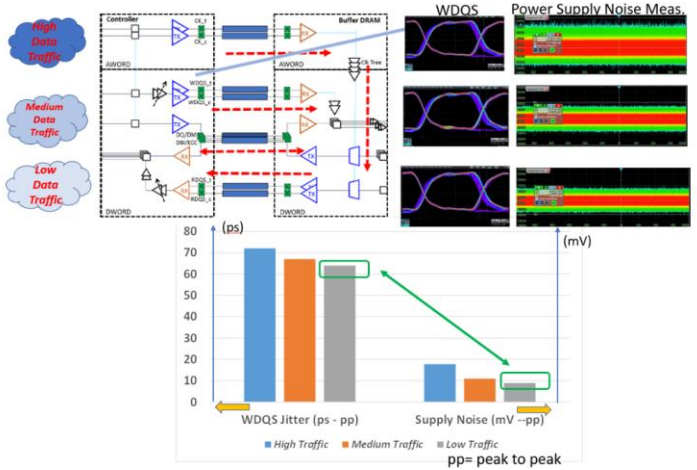


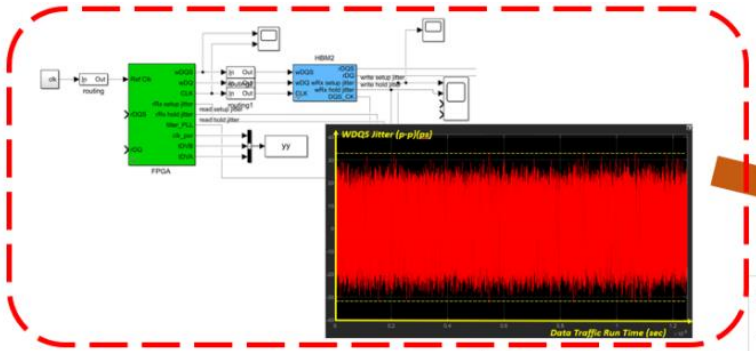
Core Power Spectrum Meas.

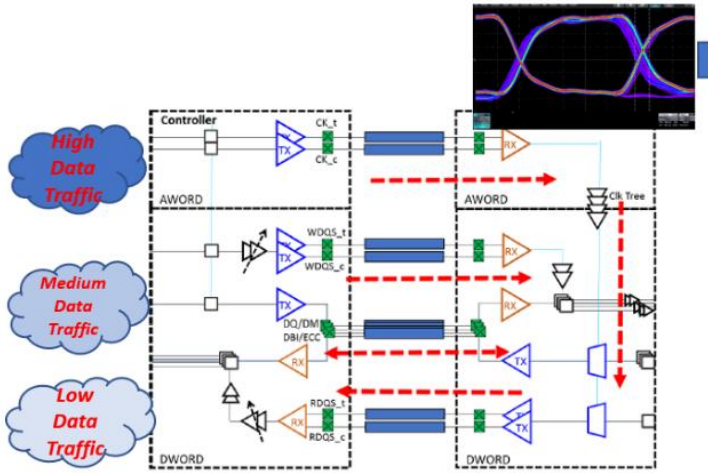


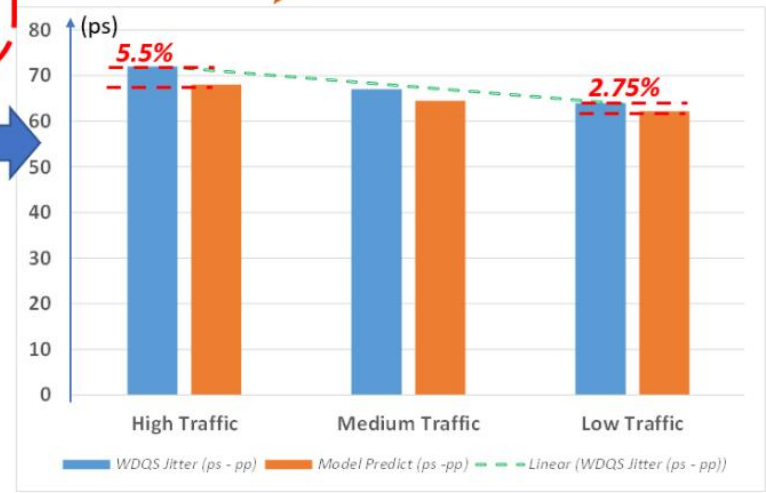
Core Power Time Domain Meas.







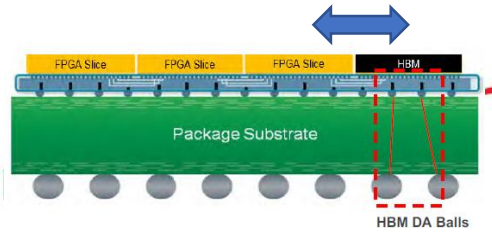


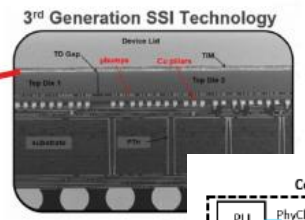


→ *System Jitter Measurements with different traffic excitations.*

→ *System Jitter Model predicted peak to peak jitter with different traffic excitations & show reasonable match.*

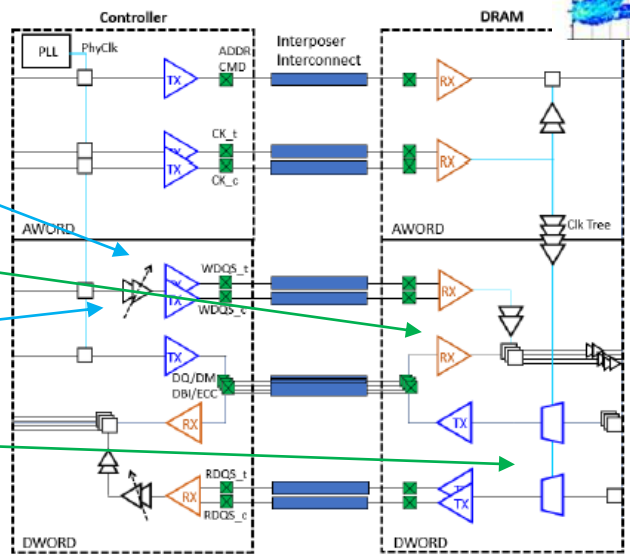
Input Design Factors Generation of Training Examples

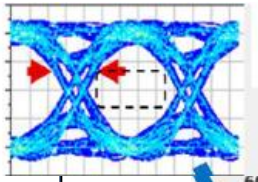


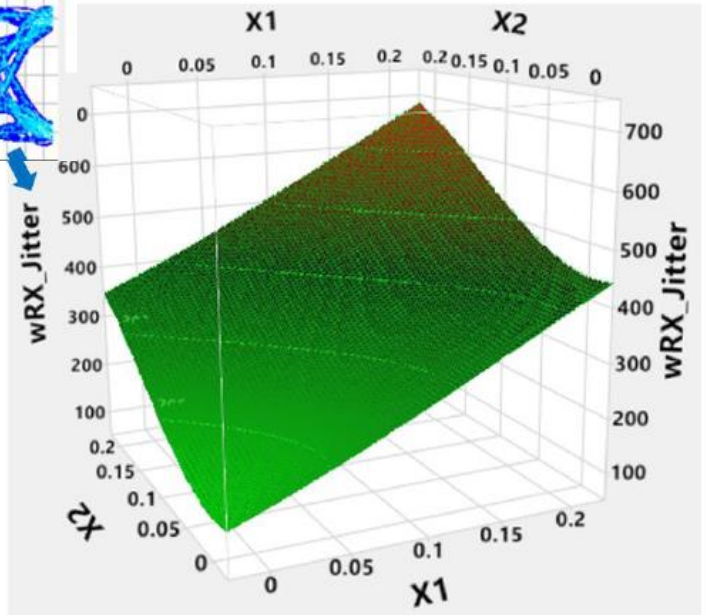


Input Design Factors	Descriptions
x_1	Power Noise Amplitude on Tx clock buffer at Noise Frequency 1
x_2	Power Noise Amplitude on Tx clock buffer at Noise Frequency 2
x_3	Power Noise Amplitude on Tx clock buffer at Noise Frequency 3
x_4	Power Noise Amplitude on Tx clock buffer at Noise Frequency 4
x_5	Power Noise Amplitude on Tx clock buffer at Noise Frequency 5
x_6	Power Noise Amplitude on Driver & RCV at Noise Frequency 1 *
x_7	Power Noise Amplitude on Driver & RCV at Noise Frequency 2 *
x_8	Power Noise Amplitude on Driver & RCV at Noise Frequency 3 *
x_9	Power Noise Amplitude on Driver & RCV at Noise Frequency 4 *
x_{10}	Power Noise Amplitude on Driver & RCV at Noise Frequency 5 *
x_{11}	Channel Jitter Amplification (Interconnect Choice)
x_{12}	Tx On-Die Clock Delay
x_{13}	Tx Driver Delay
x_{14}	Rx DQS Delay
x_{15}	Rx DQ Delay

*Assuming the Tx Driver Voltage Rail and Rx Receiver Voltage rails are connected.







→ *Integration involves different IP from Different Companies*

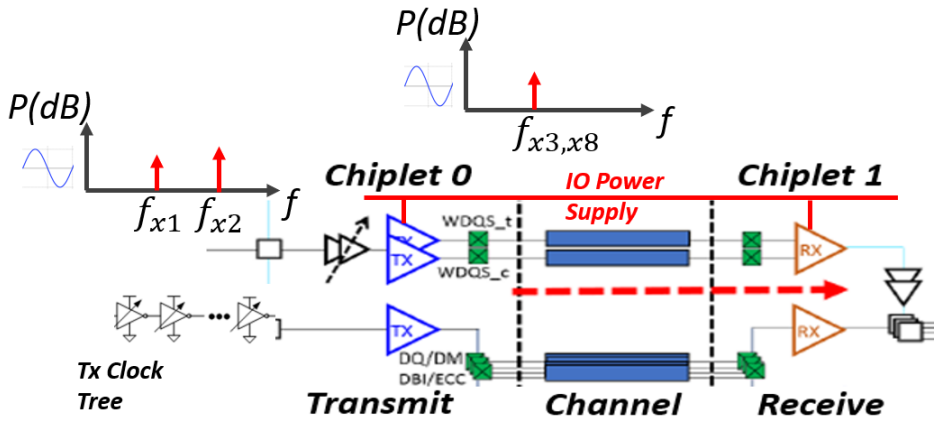
→ *System Design needs to guarantee Targeted Performance*

→ *System Design needs to Identify Critical Factors for Optimization*

	x_1	x_2	x_3	x_4	...	x_{14}	x_{15}
y_1	$x_1^{(1)}$	$x_2^{(1)}$	$x_3^{(1)}$	$x_4^{(1)}$	:	$x_{14}^{(1)}$	$x_{15}^{(1)}$
y_2	:	$x_2^{(2)}$	:	:	:	:	:
y_3	:	:	$x_3^{(3)}$	:	:	:	:
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
y_{m-1}	:	:	:	:	:	$x_{14}^{(m-1)}$	:
y_m	:	:	:	:	:	:	$x_{15}^{(m)}$

$$y = b_0 + \sum_{i=1}^{n} b_i x_i + \sum_{j=1}^{n} \sum_{k=1}^{n} b_{jk}\, x_j\, x_k + \epsilon$$

Input Design Factor Effect Summary



Response wRX_Jitter

Effect Summary

Source	LogWorth
X3*X8	9.416
X1(0,0.2)	8.298
X2(0,0.2)	8.221
X8*X8	7.027
X14(240,360)	6.830
X1*X14	6.348
X6(0,0.2)	6.144
X2*X7	6.028
X8*X14	5.940
X6*X14	5.159
X2*X2	5.136
X2*X14	4.774
X8*X13	4.623
X8(0,0.2)	4.467
X2*X7*X14	3.855
X2*X2*X2	3.825
X3*X14	3.657
X2*X4*X12	3.464
X1*X7*X10	3.318

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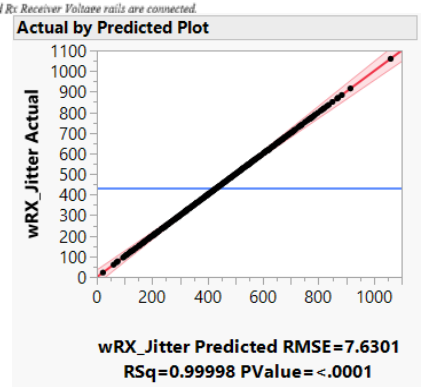
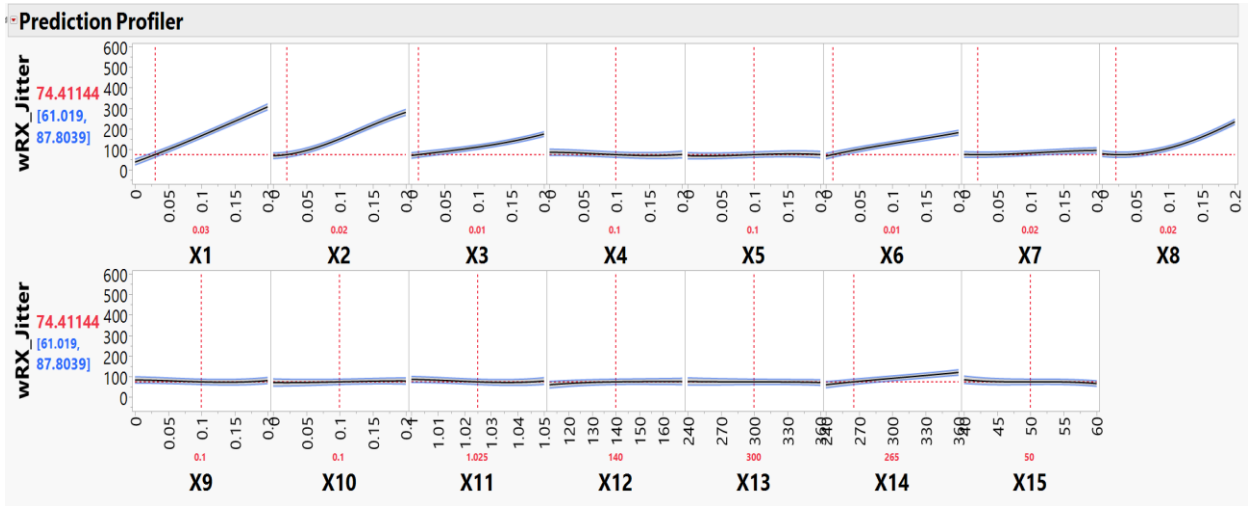


→*Actual by predicted plot show a good model fit.*

→*Effect summary table show x1, x2 and interaction of x3 and x8 as most significant factors.*

Input Design Factor Sensitivity Read Out



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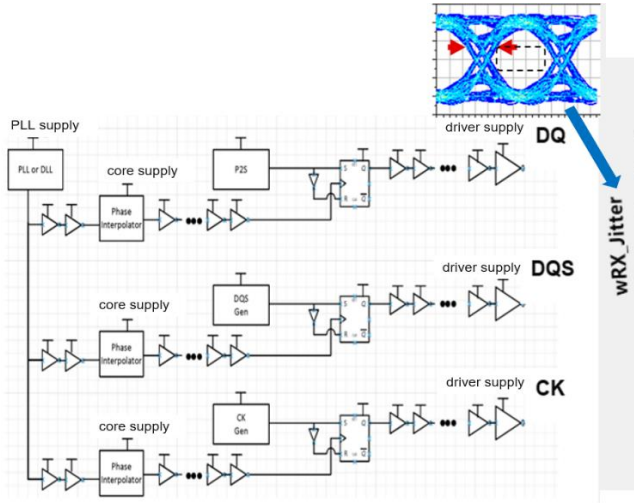
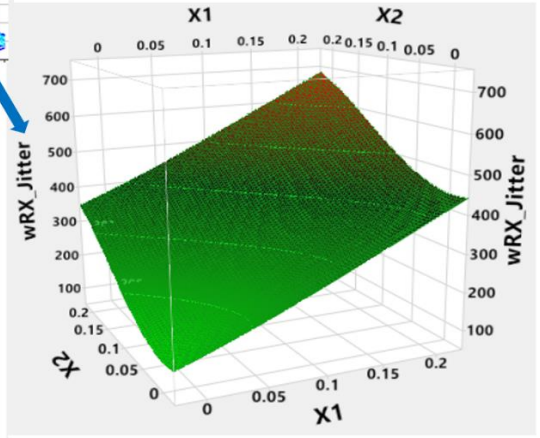
x_{10}	Power Noise Amplitude on Driver & RCV at Noise Frequency 5 *
x_{11}	Channel Jitter Amplification (Interconnect Choice)
x_{12}	Tx On-Die Clock Delay
x_{13}	Tx Driver Delay
x_{14}	Rx DQS Delay
x_{15}	Rx DQ Delay

*Assuming the Tx Driver Voltage Rail and Rx Receiver Voltage rails are connected.





→ *Prediction profiler captures the impact of Input Design Factors to the Output.*

→ *Impactful Design factors are specified & optimized 1st .*

→ *The Surface plot shows the dependency of two significant design factors x_1 and x_2 on output jitter.*

x_1 → Tx Clock Tree Noise Tone at speed &

x_2 → Tx Clock Tree Noise Tone at ½ speed.

Outline

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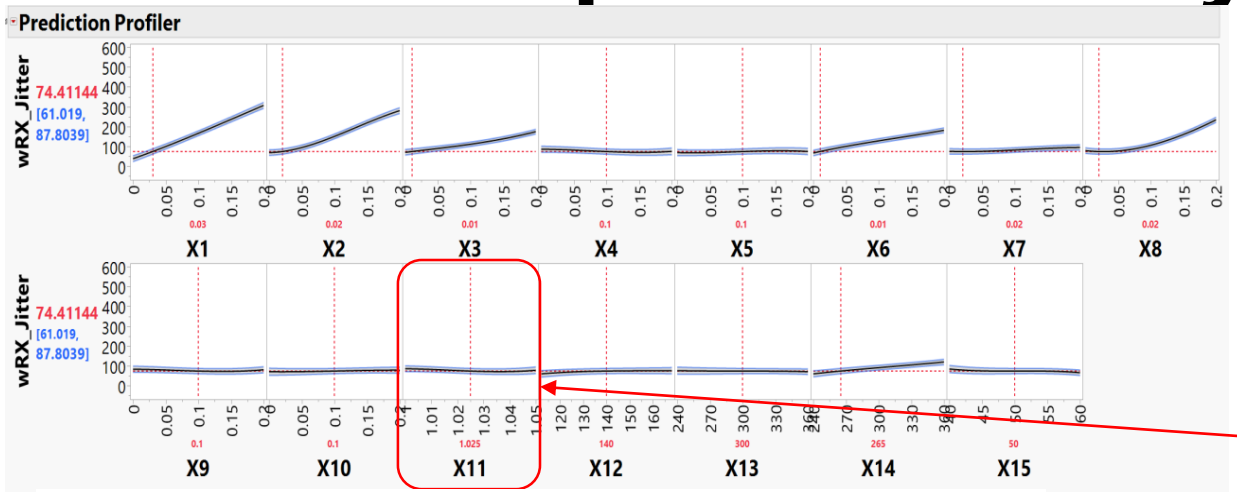
  - *How to determine these key design factors for development design & for specification?*
- *Design Factors (Specification Parameters) Sensitivity Analysis*
  - *Unified System Jitter Model for Gradient Descend Quantification.*
- *A Case Study: Performance Evaluation based on Input Design Factor Sensitivity Results*
- *Summary and Conclusions*

System Jitter Shmoo Comparison between Channel Implemented by Interposer and InFO



Input Design Factors	Descriptions
x_1	Power Noise Amplitude on Tx clock buffer at Noise Frequency 1
x_2	Power Noise Amplitude on Tx clock buffer at Noise Frequency 2
x_3	Power Noise Amplitude on Tx clock buffer at Noise Frequency 3
x_4	Power Noise Amplitude on Tx clock buffer at Noise Frequency 4
x_5	Power Noise Amplitude on Tx clock buffer at Noise Frequency 5
x_6	Power Noise Amplitude on Driver & RCV at Noise Frequency 1 *
x_7	Power Noise Amplitude on Driver & RCV at Noise Frequency 2 *
x_8	Power Noise Amplitude on Driver & RCV at Noise Frequency 3 *
x_9	Power Noise Amplitude on Driver & RCV at Noise Frequency 4 *
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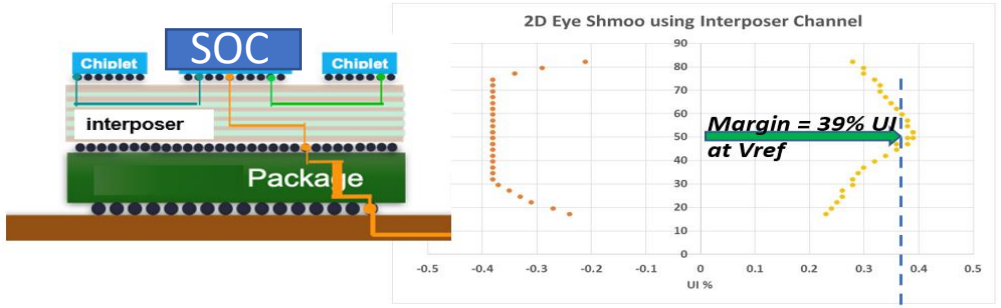
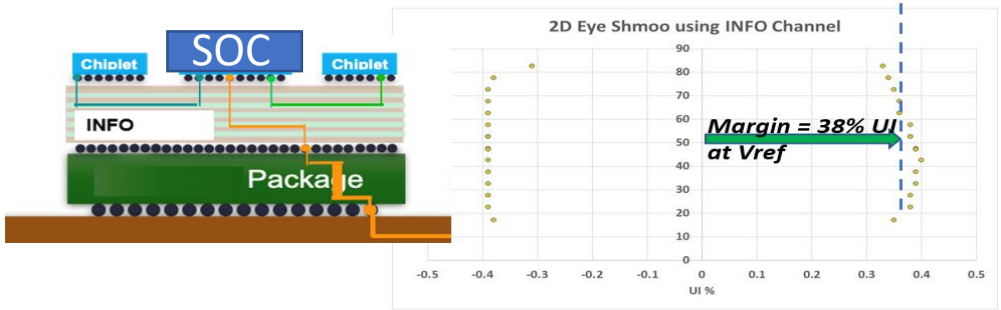
Assuming the Tx Driver Voltage Rail and Rx Receiver Voltage rails are connected.





→ ***Sensitivity Analysis Allows a Prediction of successful channel media trade.***

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Summary & Key Takeaways

- ***Monolithic Silicon System On Chip (SOC) Integration ROI Slow Down:-***
  Due to Silicon Technology scaling decelerated.
- ***Chiplet Implementation as a Solution:-***
  New Integration provides a new way to incorporate different features to system SOC.
  But….. Also create new challenges!
- ***New Challenges:-***
  Heterogenous integration requires identifying key design factors for specifications as well as for system optimizations.
- ***A Systematic & Holistic approach is presented based on a unified system jitter model.***
  Unified Jitter Model was developed to combine the input design factors effects.
  The model was correlated with empirical measurement.
  Unified Jitter Model was used to generate training examples and for sensitivity analysis.
- ***A Case Study Application***
  Demonstrated the application flow which quantified the impact of changing of chiplet interconnect media.

Identifying Key Design Factors for Specification Systematically is crucial for ECO System Enabling.

Thank You !!

Q & A

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