Road to Chiplets: Design Integration

May 10-12, 2022

MEPTEC
THE NEXT GENERATION

www.meptec.org

MEPTEC 2022

Heterogenous Integration: The role of design in putting pieces together

Sujit Sharan

Senior Director, Advanced Design & Technology Solutions

ATTD/Intel

Agenda

- Heterogenous Integration: Opportunity
- Complexities involved
- Why STCO is important?
- Enabling eco system and other vendors
- Next Steps

ADTS

Heterogeneous Integration: What & Why?

Key Elements

- Heterogeneous integration combines chips and chiplets using advanced packaging.
- Chips and chiplets include
  - diverse functionalities (e.g., memory, compute engine, I/O hub, graphics)
  - varying silicon nodes, different foundries
- Advanced packaging can be 2.5D or 3D with:
  - fine line/space, microbumps & fine pitches
  - die stacking/embedding/TSVs, redistribution layers

The Benefits

- Reuse strategies & scalable product portfolios
- Time-to-market
- Product optimization & customization
- Manufacturing yield and quality

2.5D Advanced Packaging

Std C4 Bump & Pitch (~110um)
Micro-Bump & Pitch (45um – 55um)
HBM
SOC
Surface
Surface -1
Surface -2
~75um
Vss Layer
Vcc Layer
Std Pkg vias & routing l/s (~20um / 20um)
Bridge routing l/s (~1-2um / 1-2um)

3D Advanced Packaging

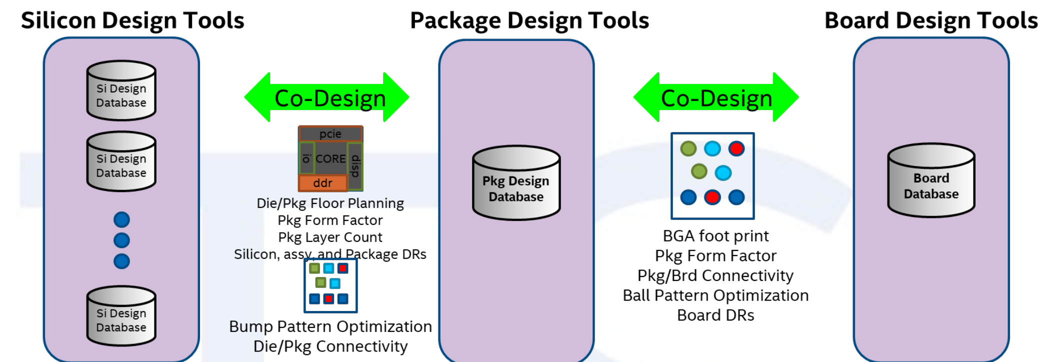
ubumps
Top Die 1
Top Die 2
Top Die 3
RDL (redistribution layer)
36 um
Base Die
Die-to-die routing
C4 bumps
TSV (thru-silicon via)
110 um
Package Substrate
BGAs
1 mm
Motherboard

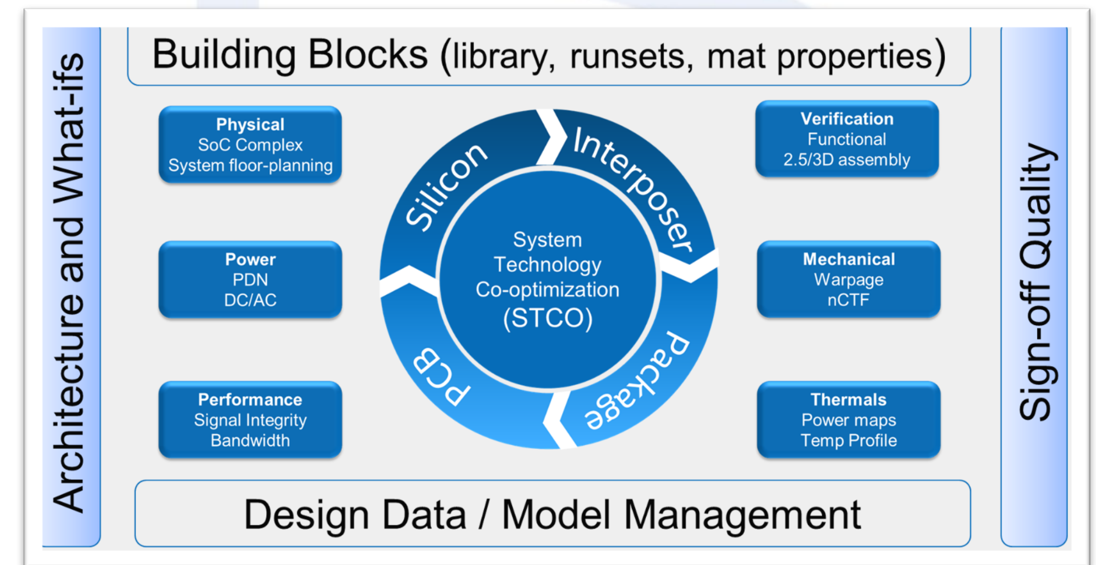
Design Complexities in Heterogenous Integration

- Connectivity across Stack
- TSV Planning
- Transistor / Routing Conflicts
- RDL Optimization
- Visualization
- Bi-Directional Design Data Flow
- Co-optimization across Stack
- Trade-offs
- Validation

EDA Tools & Heterogenous Integration

- Traditionally IC design is performed without consideration of package and board
- Tools enabled design, analysis, and verification of individual components
- With heterogenous integration, co-design tools, and methodologies are needed for:
  - multi-domain design planning (silicon, package, board)
  - multi-physics (thermal, mechanical, electrical) analysis
- To maximize benefits of technology, trade offs are critical and tools for optimum trade off are lacking in the EDA eco system.
- Design optimization includes architecture selection, overall form-fit (XYZ) estimation, routability, signal integrity and power delivery, thermals, and mechanical design analysis





Package Design complexity stresses EDA Tools

- Very Large databases
- High-aspect ratio of features (from silicon to package sizes)
- Integration of data formats (internal/external silicon, bridge die, multiple pkg substrates)
- Silicon / Pkg Co-Design (interactive, bidirectional)
- Compatibility / exportability to TME modeling & analysis tools
- **Revolutionary scaling of tools is needed!**

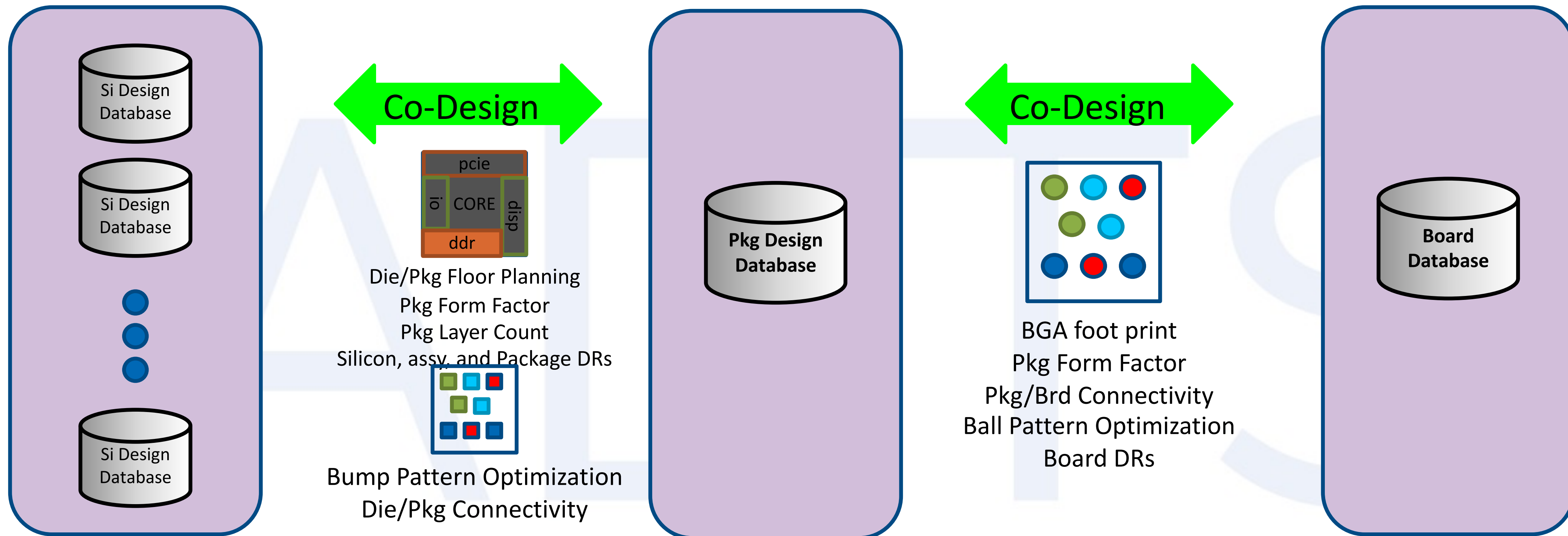
ADTS

Why is STCO (Co-Design) so important?

- STCO is optimization of the entire system driven by:
- Co- Optimized Design
  - Si Design Optimization (Top MLs, MIM , Bump, Advanced DRs)
  - Package Design Optimization (Bump Map, Layer Count (LC), Form Factor (FF), Power Delivery Network (PDN), Signal Integrity (SI), Advanced DRs, Ball Map, Yield)
  - Board Design Optimization (LC, FF, PDN, SI, Advanced DRs)

Need fully optimized design methodology: in SoC, Package, Board, System, Software to achieve the highest performance at the right cost structure

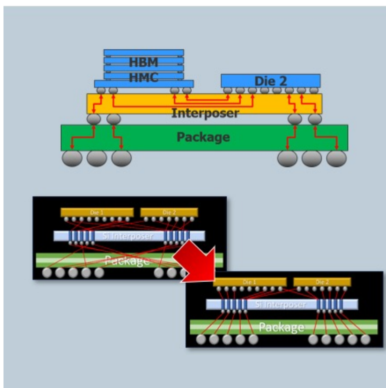
STCO Design Process



Thermal / Mechanical / Electrical trade-offs are very serial … Efforts to enable visualization across the stack and interactive, bi-directional data flow/Optimization are warrantied

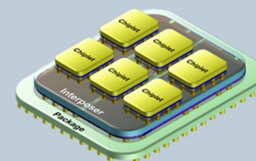
XSI, an industry first co-design tool

Xpedition Substrate Integrator
Accelerate heterogeneous planning and prototyping



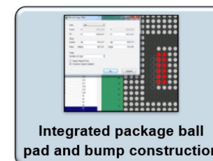
- ✓ Aggregates data from different sources and formats into cohesive system model for planning
- ✓ Define and optimize connectivity in context of full-system – die, interposer, package, & pcb
- ✓ Generate and manage the full system net list
- ✓ Drives rapid prototyping to evaluate electrical and thermal feasibility

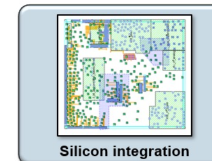
Heterogeneous planning and prototyping
Xpedition Substrate Integrator – value proposition

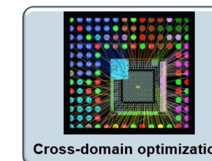


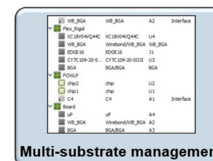
- ✓ Eliminates dependency on error-prone spreadsheets
- ✓ Reduces iterations while improving route resource utilization
- ✓ Drives better IO assignment with dynamic device interaction and connectivity visualization
- ✓ Delivers capacity, performance, and scalability necessary for 500K+ pin interposer designs

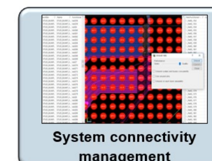
Xpedition Substrate Integrator
Functionality for heterogeneous planning and prototyping

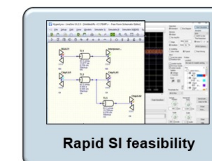

Integrated package ball pad and bump construction


Silicon integration


Cross-domain optimization


Multi-substrate management


System connectivity management


Rapid SI feasibility

EDA Eco-system Enabling Partnership

- EDA Eco system enabling is critical to deliver best-in-class EDA tools for Intel and industry overall
- Partnering with all 3 EDA vendors to drive our STCO perspective with rest of the industry
- Power delivery methodology for 3DIC delivered in partnership with Ansys, Siemens
- Cloud based design enabling definition in flight
- Significant effort from all 3 major EDA vendors on 3DIC STCO capabilities including package and PCB

Next Steps

- Silicon package co-design and analysis should be standardized and proliferated across the industry
- Opportunity to partition / budget specs optimally across all system ingredients and meet performance and cost targets systematically
- Need standards-based EDA eco-system to achieve co-optimization across the system, chiplet partners, and foundry ecosystem

COPYRIGHT NOTICE

This presentation in this publication was presented at the **Road to Chiplets: Design Integration** (March 10-12, 2022). The content reflects the opinion of the author(s) and their respective companies. The inclusion of presentations in this publication does not constitute an endorsement by MEPTEC or the sponsors.

There is no copyright protection claimed by this publication. However, each presentation is the work of the authors and their respective companies and may contain copyrighted material. As such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

www.meptec.org

MEPTEC
THE NEXT GENERATION