Road to Chiplets: Design Integration

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Silicon Photonics Chiplet Package - Design Integration

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Agenda

- Scope (Silicon Photonics Optical IO Chiplet)
- Design for X (mainly DfM principles and practices)
- Design enablement (including modeling and design tools)
- Test Vehicles (Pico-Killington DDP)
- Summary

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Scope

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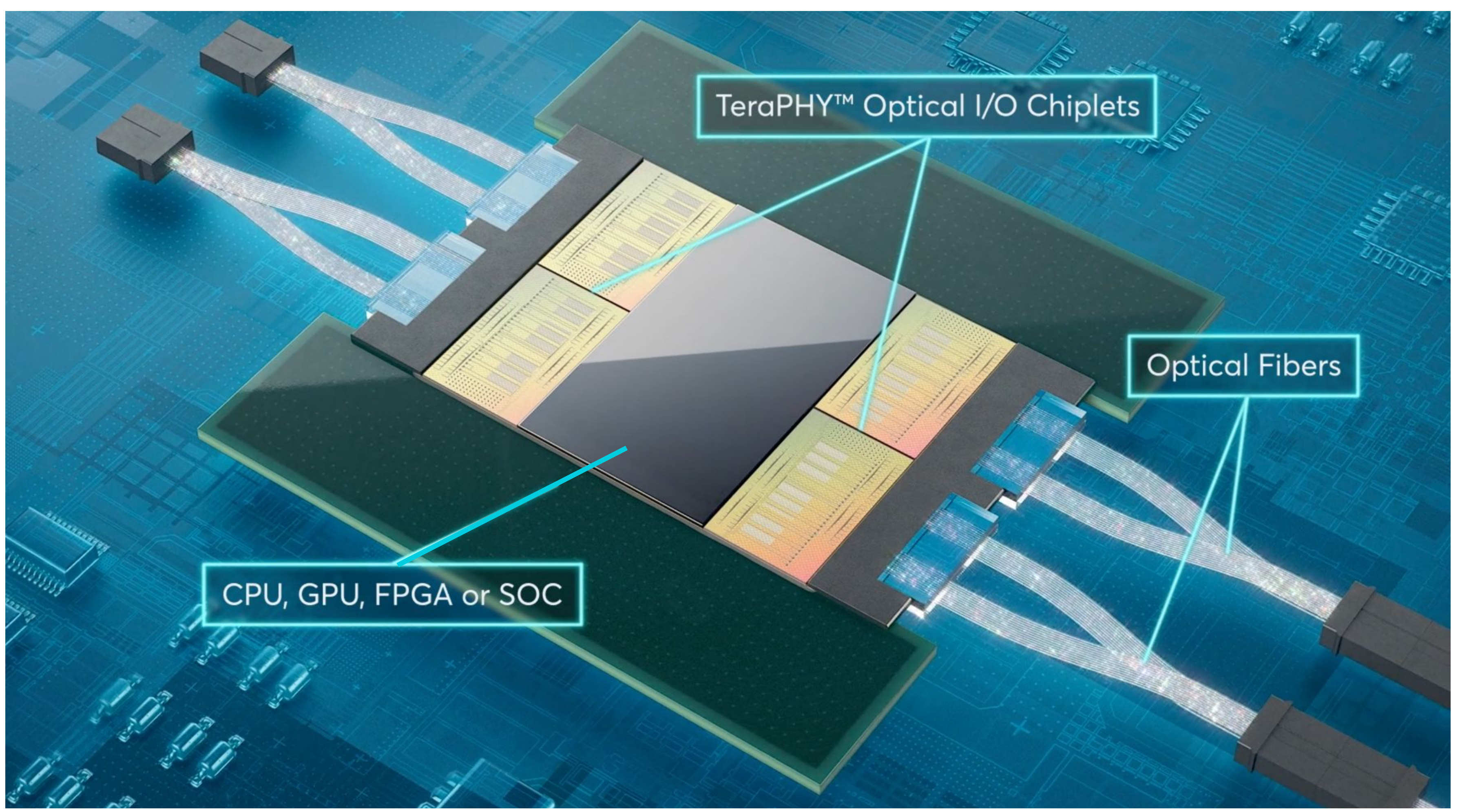
Ayar Labs - TeraPHY^{TM} Optical IO Chiplet



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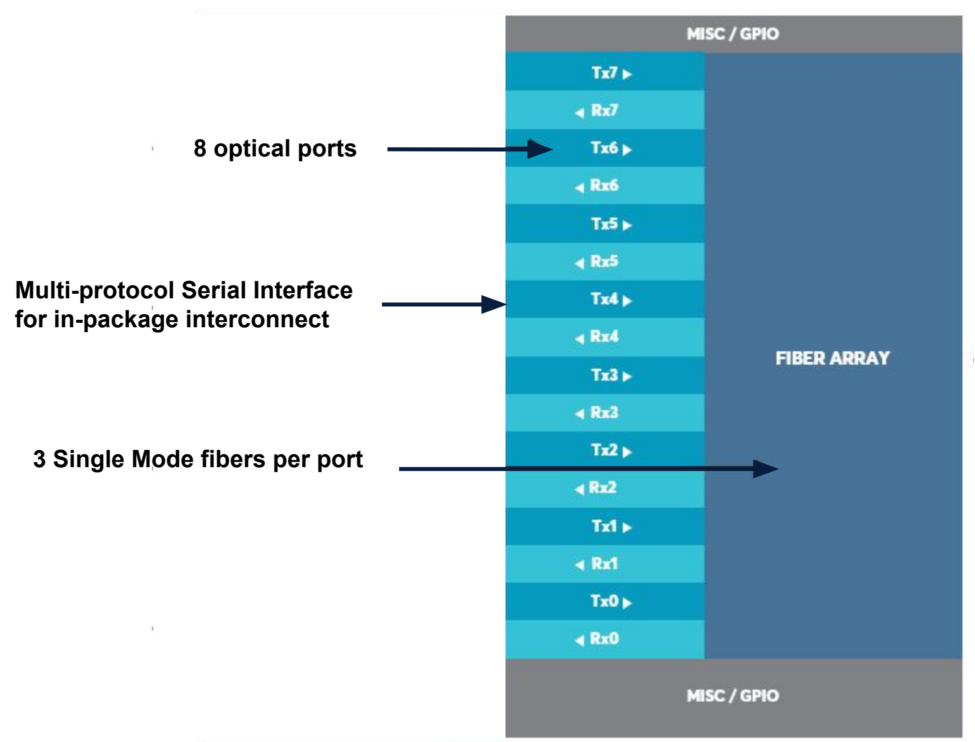
TeraPHY™ In-Package Optical I/O Chiplet



Features

- Supports PCIe/CXL, CEI 56G XSR, JESD serial electrical interfaces
- 8 full-duplex optical ports
- 8 WDM slices per optical port
- Configurable up to 464 Gb/s per port (3.7 Tb/s per chiplet, full duplex)
- NRZ modulation format on the optical port – no Forward Error Correction (FEC) required!
- Roadmap to 32+ Tb/s per TeraPHY™ chiplet
- Energy efficiency < 3 pJ/bit
- Latency < 1ns + TOF
- Distances up to 2km (better: socket-2-socket, board-2-board, rack-2-rack

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Design Enablement

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Design Enablement (Chiplet/Package Co-Design)

- Are thermal, electrical, mechanical modeling and design tools **interoperable** to do the relevant analysis?
  - It depends…
- Do simulation teams and modeling tools talk **same language and boundary conditions**?
  - Teams are interested in different scales of simulation. Multichip Packaging teams use **Reduced Order Models** and **Rules of Mixtures** to make simulation procedure more tractable.
- How are transient/dynamic issues in electrical and thermal domains handled? What are right stimulus and boundary conditions for DI simulation? Are characterization tools able to provide right inputs to design too for current and future designs?
  - Yes, **characterization tools** (i.e., materials, strength, and thermal analysis) are adequate, but a proper amount of forensics needs to be used to understand physics of failure & overtemp conditions.
- How to avoid custom scripts and other "hacks" in the design flow?
  - Use **intrinsic macro language** or **approved API** within software.

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Multichip Thermal Simulation

- Synchronization between package design and mechanical/thermal design is also a significant challenge to **first-time-right success**.
  - Heterogeneous multi-substrate packages exhibit multiple chip-package interactions.
  - One of the largest is thermal dissipation, especially of non-linearly or location-specific generated heat typical (i.e., hotspots) in such packages.
- A typical approach to thermal management uses a **heat sink**, **integrated heat spreader** (IHS), or **vapor chamber** for heat transfer and dissipation.
  - A heat spreader is only as good as its design.
  - For the heat spreader to be efficient and effective, it must be co-designed and co-simulated in with the package, not as an afterthought.
  - Designing the entire package in 3D ensures efficient heat-transfer realization without significant design compromises.

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Electro-Mechanical Simulations & Practices

- Synchronization of electrical and mechanical information is essential to ensuring that no physical violations occur when a package is placed within an enclosure or an entire system.
- 2.5D and 3D stacking can create a **variety of unintentional physical stresses**, such as substrate warpage during mounting and bump-induced stress.
  - Designers must be able to analyze a layout for **stresses caused by such chip-package interactions** and their impact on device performance or birefringent effects in optical fibers.
  - Many drivers are setting up **Keep-Out Zones** (KOZs).
  - KOZs are used for **stress reasons** (Through Silicon Vias), **underfill bleeding**, or **mechanical fitment**.
- The incremental exchange of data during design is fundamental to ensuring ECAD-MCAD compatibility and increased first-pass success.
- It also aids in the creation of more robust designs while increasing productivity and achieving faster time to market.

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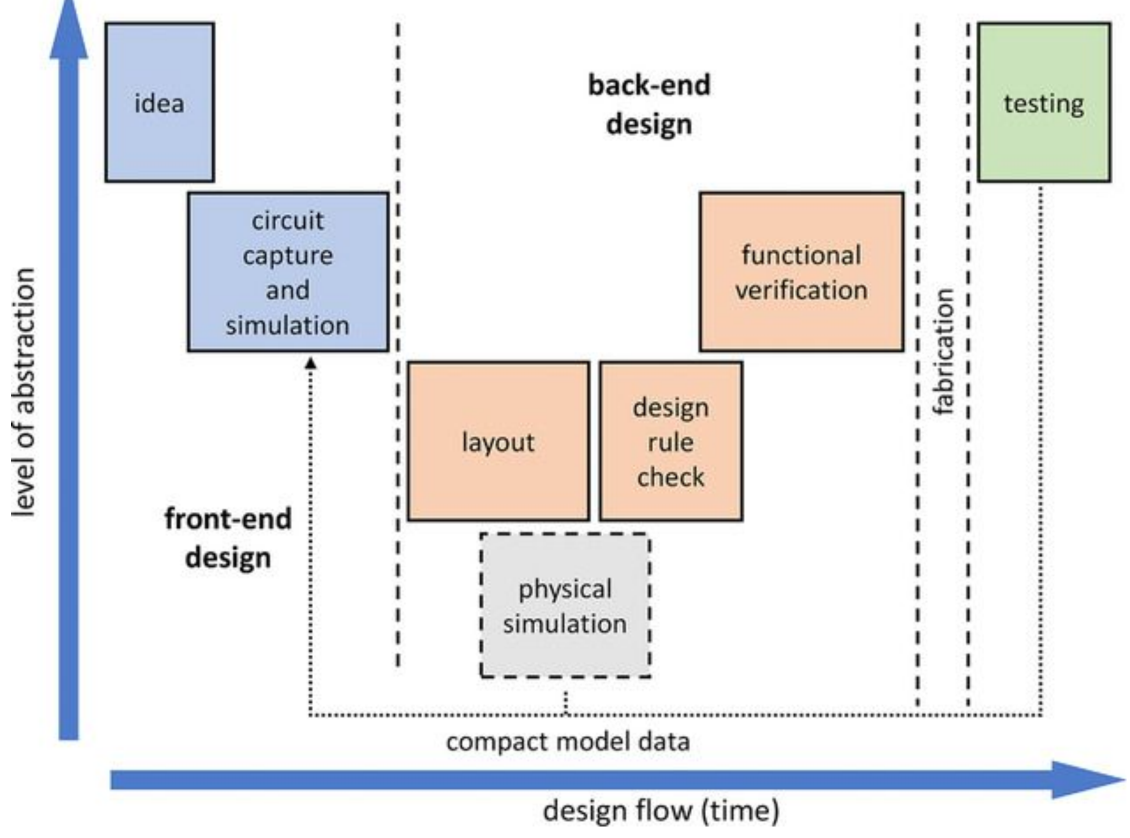
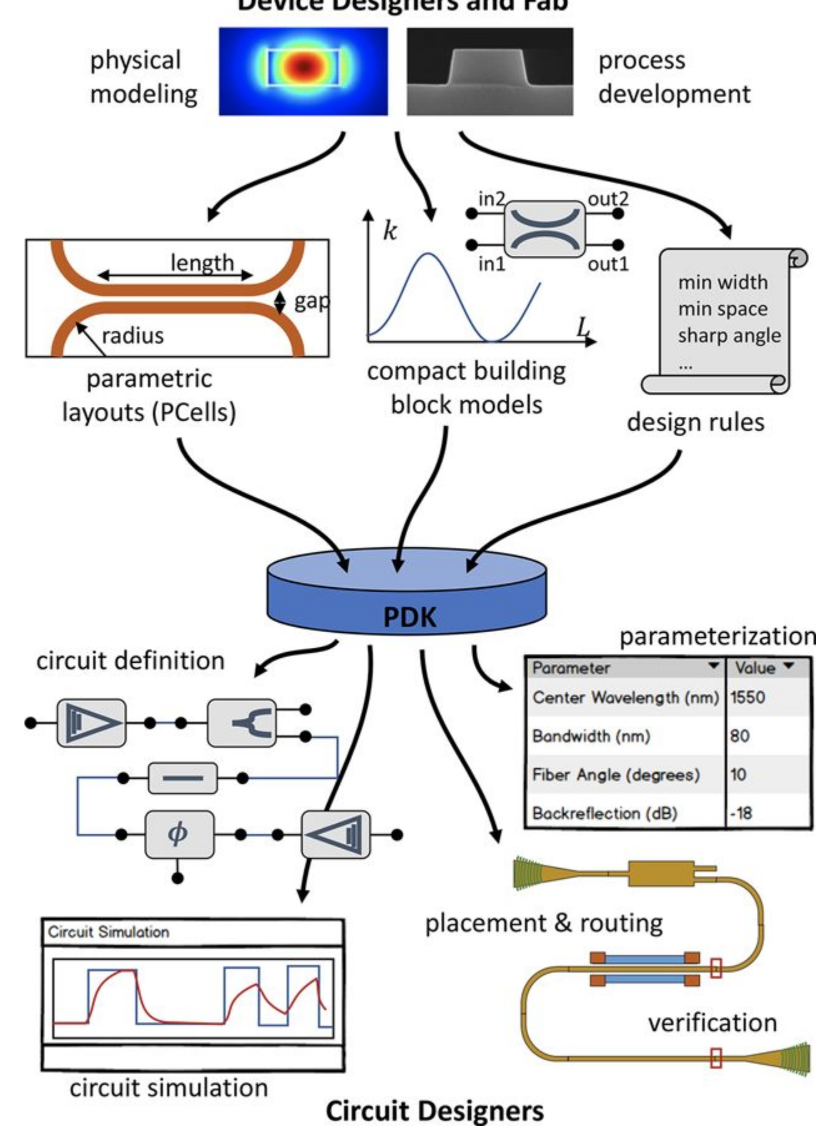
Silicon Photonics Design and Verification Flow

Different levels of abstraction in a optical IO circuit design flow





Ref: W. Bogaerts and L. Chrostowski, "Silicon Photonics Circuit Design: Methods, Tools and Challenges," Laser Photonics Rev. 2018, 1700237.
http://fotonica.intec.ugent.be/download/pub_4023.pdf

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Design Enablement (Pure Design Aspects)

- “Early delivery of accurate design kits is critical for design.”*
  - Early and accurate PDKs are conflicting qualities, unfortunately.
- If we had to choose, **early PDK is preferred** for design enablement over waiting too long for accurate.
  - You can always get some of your design, **if you had an early but inaccurate PDK**.
  - However, if there's no PDK, it doesn't matter how accurate it will be -- designs can't start, the foundry can't run designs to improve yield, model will not get more accurate
- **Standard cells** and **healthy IP ecosystem** are key.
  - Hard to piece together an SoC, if you had to develop it all yourself.

*Reference: M. E. Mason, "Design enablement: The challenge of being early, accurate, and complete," 2012 Symposium on VLSI Technology (VLSIT), 2012, pp. 145-146, doi: 10.1109/VLSIT.2012.6242503.

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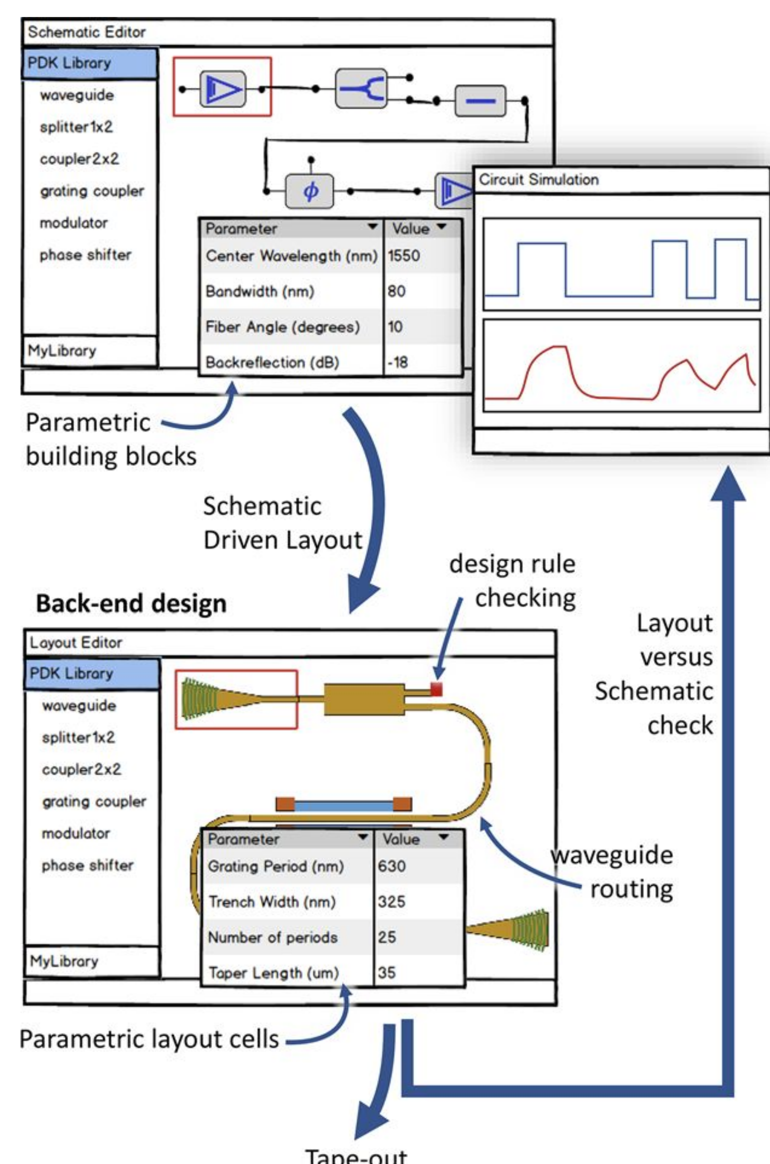
Photonic Design Flow

- Photonic design flow based on existing EDA flows.
- Flow is separated into a **front-end** (using a schematic editor) and a **back-end** (using a layout editor).
- Library-based approach helps to **keep schematic and layout aligned**, and allows for functional verification of layout before tape-out.
- Detailed geometry is abstracted into building blocks with a **compact numerical model**; **full electromagnetic waves are replaced with signals**.
- After fabrication, **design and simulations** can be compared to **actual measurements and test results**, which can be fed into design of subsequent circuits.



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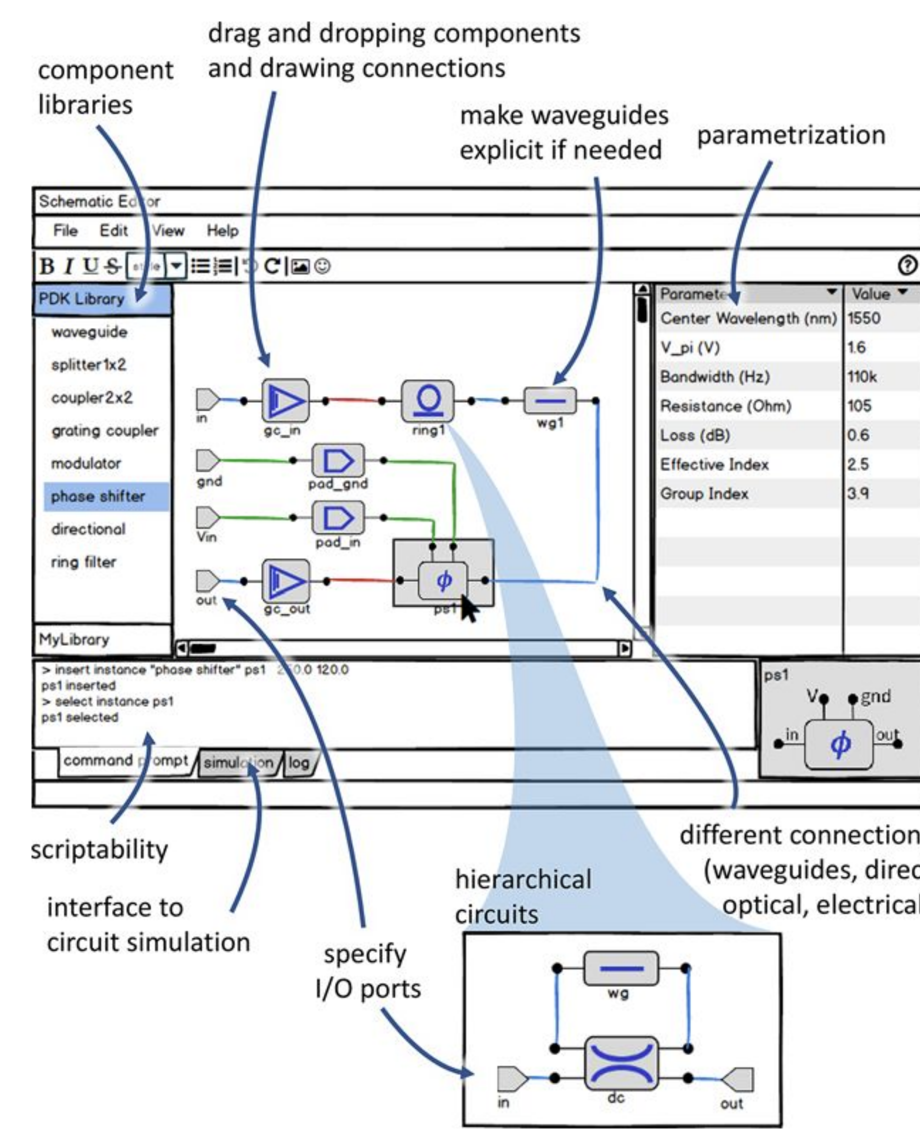
Schematic Capture (Electro-Optical)

Anatomy of a typical schematic editor used to define circuits:

- **Symbols** are placed and connected, both electrically and optically (either with explicit definition of waveguides or implicit).
- **Components** can be parameterized and hierarchically broken down in subcircuits.



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Photonic Circuit Design Tools & EDA Tools

Photonic Design Tools

- Design Suite v11 (VPIphotonics) https://www.vpiphotonics.com/Tools/DesignSuite/
- IPKISS Photonics Design Platform (Luceda Photonics) https://docs.lucedaphotonics.com/
- Lumerical (ANSYS) https://www.lumerical.com/products/
- Miscellaneous photonic design tools (Photo Design) https://www.photond.com/products.htm
- OptiSystem (Optiwave) https://optiwave.com/optisystem-overview/
- PhoeniX Software (Synopsys) https://www.synopsys.com/photonic-solutions.html
- RSoft (Synopsys) https://www.synopsys.com/photonic-solutions/rsoft-photonic-device-tools.html

Electronics Design Tools

- Virtuoso/Spectre/Allegro APD (Cadence Design Systems) https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/layout-design/virtuoso-layout-suite.html, https://www.cadence.com/en_US/home/tools/ic-package-design-and-analysis/cross-platform-co-design-and-analysis.html
- Mentor Calibre/Pyxis/Eldo/LightSuite/L-Edit Photonics (Siemens) https://eda.sw.siemens.com/en-US/ic/calibre-design/, https://eda.sw.siemens.com/en-US/ic/ic-custom/photonic/

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Design for X

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Product Management (Design for X)

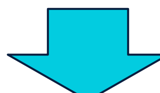
BRD targets solutions for a project including needs and expectations, purpose behind this solution, and any high-level constraints.

MRD targets people who need to understand opportunity you're pursuing at a high level.

PRD is targeted at leaders in product development.

ERD is target at engineers and defines product spec and technical requirements.

Business Requirement Document	Market Requirement Document	Product Requirement Document	Engineering Requirement Document



DESIGN	CODE/ASSEMBLE	TEST	RELEASE

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Example: Design for Testability (Electro-Optical)

Failure	Metrics
Low/High	Tx and Rx MRR tuning efficiency
High IL	L-to-Tx WG, Rx WG, and Fiber interface
High RL	internal component and Fiber interface
Responsivity	Tx Monitor and Tx PD
Dark current	Rx PD and Tx Monitor
Modulation	Efficiency and Bandwidth
PD bandwidth	PD Bandwidth
Heater IV	Out-of-family (Tx) and Out-of-family (Rx)
V-groove	Etch width and depth
Fiber polarization	Misalignment

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Design for Reliability (DfR)

- Design for Reliability (DfR) is a process that ensures a product, or system, performs a specified function within a given environment over the expected lifetime.
  - **DfR** often occurs at the **design stage** — before physical prototyping — and is often part of an overall design for excellence (DfX) strategy.
- The complexities of today's technologies make DfR more significant — and valuable — than ever before. Some of these reasons include:
  - **Product differentiation**: As electronic technologies reach maturity, there are fewer opportunities to set products apart from the competition through traditional metrics — like price and performance.
  - **Reliability assurance**: Advanced circuitry, sophisticated power requirements, new components, new material technologies and less robust parts make ensuring reliability increasingly difficult.
  - **Cost control**: 70% of a project's budget is allocated to design.
  - **Preserving profits**: Products get to market earlier, preventing erosion of sales and market share.

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Silicon Photonics Test Vehicle

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Package Design Speed-Up

- In the past, IC packaging engineers leveraged **standard EDA design tools** coupled with a **set of loosely defined rules** to lay out their packages, but this approach has many limitations when designing today's advanced multi-die packages.
- To provide a more holistic approach to the design and verification of SiP, OSAT and CAD companies have collaborated closely to develop an **Assembly Design Kit** (ADK), methodology, streamlined, and **automated reference flow** all tailored for OSAT's advanced IC package technologies.
- During package assembly, a few characterization techniques are implemented to ensure a higher quality with **Design for Manufacturability** and **Design for Reliability** can be delivered.

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Test Vehicle Drivers

- **How does Design Integration (DI) drive test vehicles?**
  - Today's IC and chiplets are quite complex with extreme low-k thin films, tight modular chip designs, and integrated optical elements.
  - Translating key attributes of the chiplet into a test vehicle ensures manufacturing success (good DfM).
  - Simulation of thermal thermomechanical, and mechanical effects are required to provide insight into product manufacturability, performance, and reliability.
- **Cost effective prototyping**
  - Yes, Ayar Labs' Pico-Killington TV chiplet has a subset of physical design features of TeraPHY™ chiplet, but for successful assembly & packaging DfM principles.

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What is Chip Package Interaction (CPI)?

- **Chip packaging interaction** (CPI) has drawn great attention to advanced silicon technology nodes due to introduction of Low-K and Ultra Low-K materials in back end of line (BEOL) and Cu pillar in chip package interconnects.
- CPI defines **manufacturability and reliability effects** as a result of interfacial cracks, delamination, crack propagation, temperature, etc.
- **Test structures** contained: Macro Heater, RTD-LB & -M2, Corner Stitches, Crack Detection, P-LINE, P-STITCH, Strain Gauge Split-A, -B, Daisy Chain
- Having a package test chip with key CPI test structures is important to **eliminate known failure mechanisms** that occur during Far BEOL (DfM), assembly processes (DfM), and accelerated testing (DfR).

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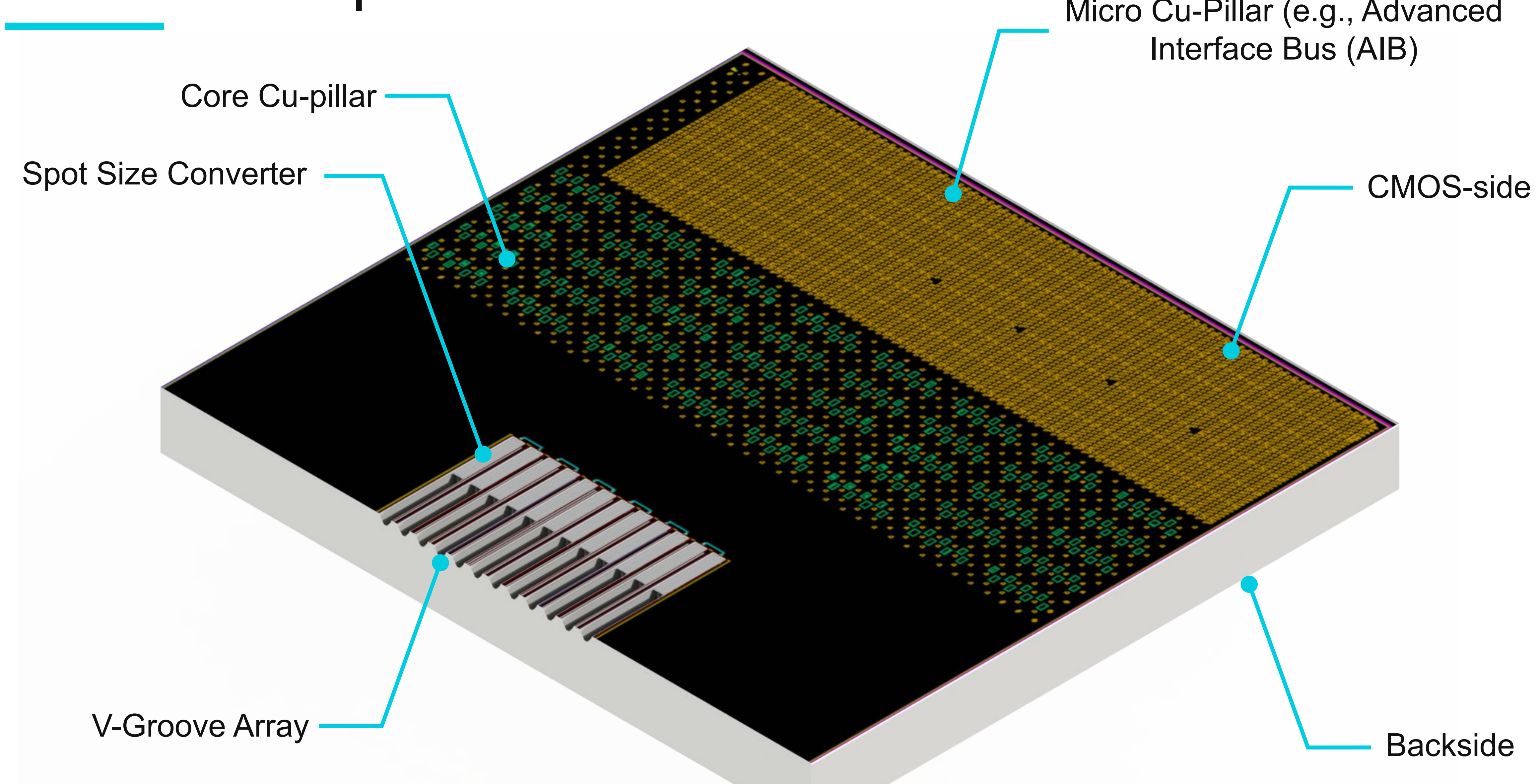
Pico TV Chiplet



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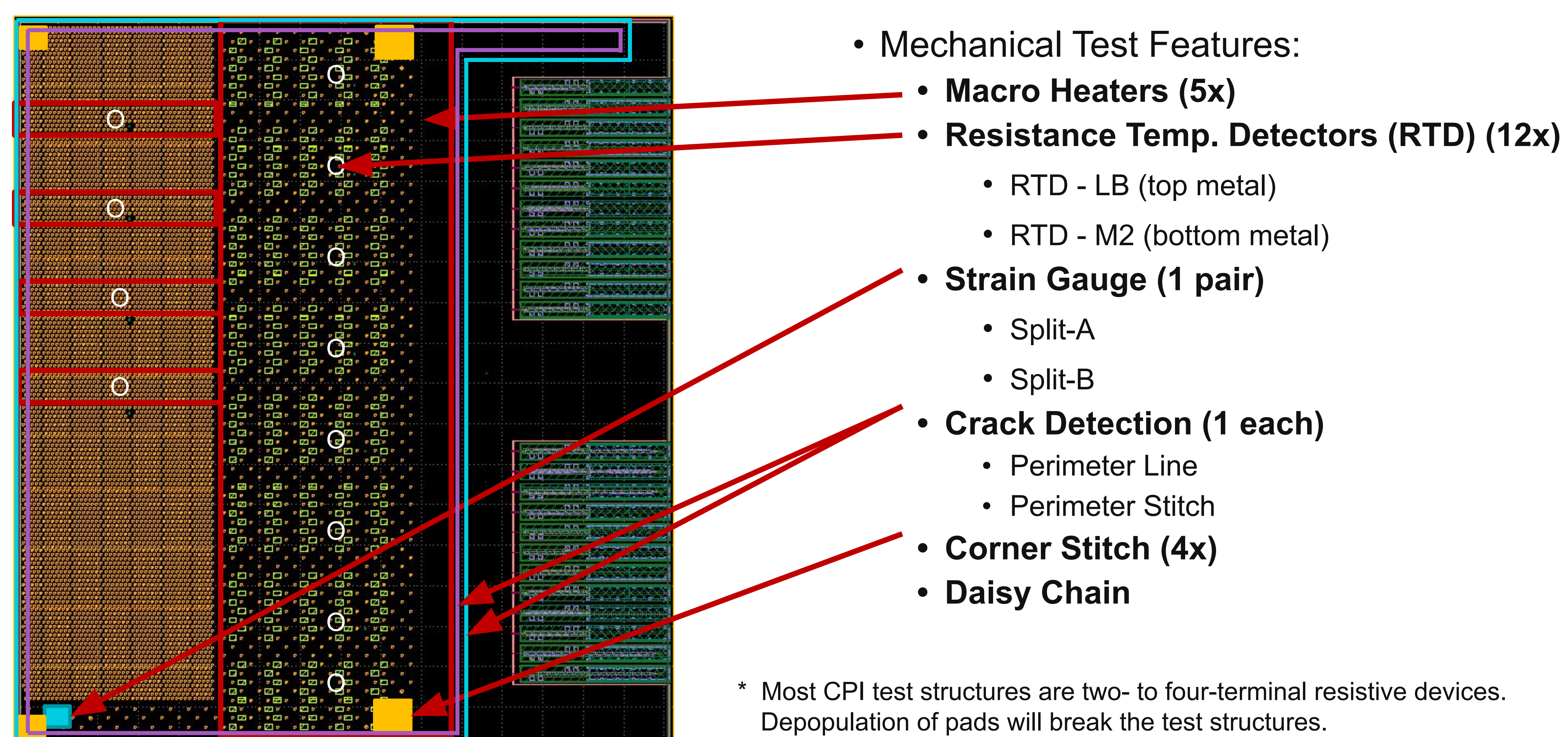
Pico Chip-Package-Interaction (CPI)



* Most CPI test structures are two- to four-terminal resistive devices. Depopulation of pads will break the test structures.

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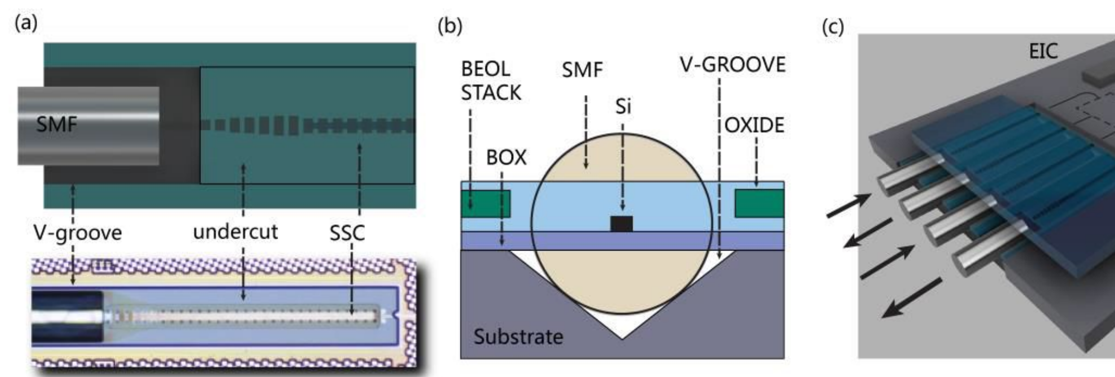
Test Vehicle Goals

- Enable an assembly process flow for silicon interposer-based Multi-Chip Packages (MCP) utilizing Cu-pillar, flip-chip, and IOSMF fiber attach called Pico/Killington platform.
- Accomplish above objective by demonstrating:
  - GlobalFoundries' 45CLO flip-chip with IOSMF (aka GF Fotonix), silicon interposer, and Cu-pillar technologies
  - Industry acceptable assembly yield and reliability metrics
  - Demonstrate viable supply chain, including:
    - Chip supplier, Interposer supplier, organic substrate supplier, fiber array unit (FAU), consumables (e.g., Capillary Underfill (CUF), epoxies, etc.)

Ref: B. Peng, et al., "A CMOS Compatible Monolithic Fiber Attach Solution with Reliable Performance and Self-alignment," in Optical Fiber Communication Conference (OFC) 2020, OSA Technical Digest (Optical Society of America, 2020).



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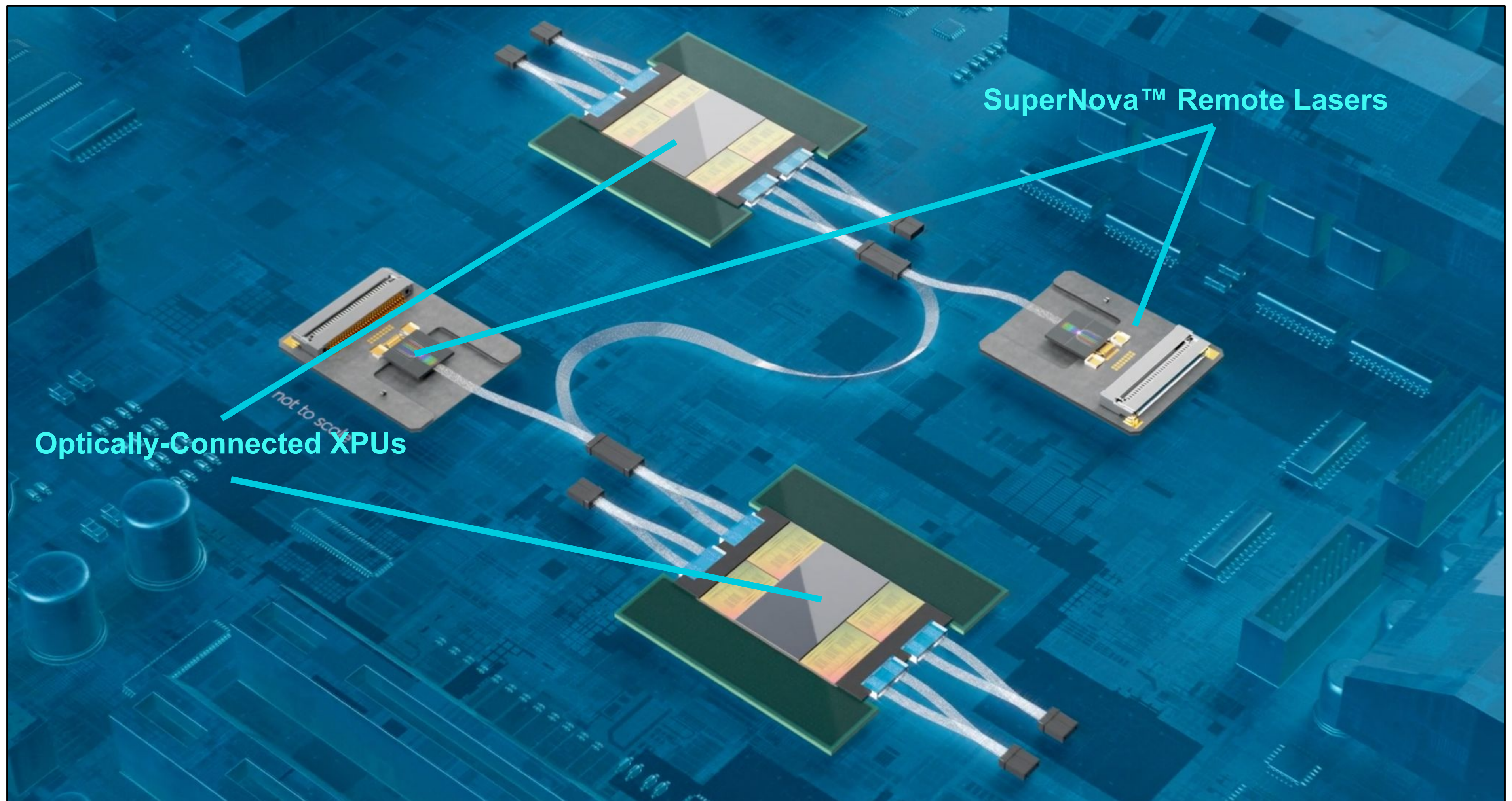
System w/ SuperNova™ Multi-Wavelength Laser



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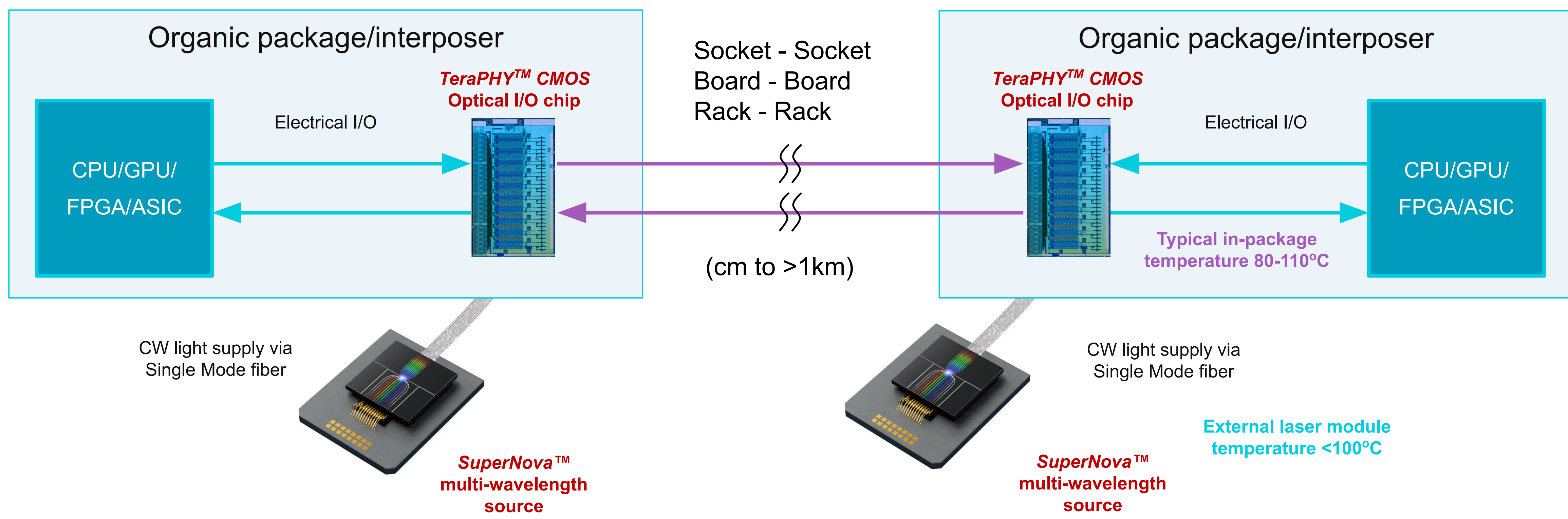
Ayar Labs Optical I/O Benefits



- Ayar Labs Optical I/O chiplet and integration technology enables bandwidth, power, and latency of short reach links to be used for long reach and fanout applications, greatly increasing overall system scalability and throughput

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Summary

- **Design for X**
  - Chiplet-Package Interactions (DfM) are very similar to leading edge CMOS devices with fragile low-k thin films, tight chiplet designs, etc.
  - When selecting electro-optical packaging materials, one must realize that they are deciding product reliability (DfR).
- **Design Enablement**
  - Chiplet and Package Co-Design is becoming more prevalent on the “Road to Chiplets”.
- **Chiplet Test Vehicles**
  - Test vehicles contain essential test structures that have proven detection of advanced silicon technology nodes with stress-sensitive thin film materials.

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