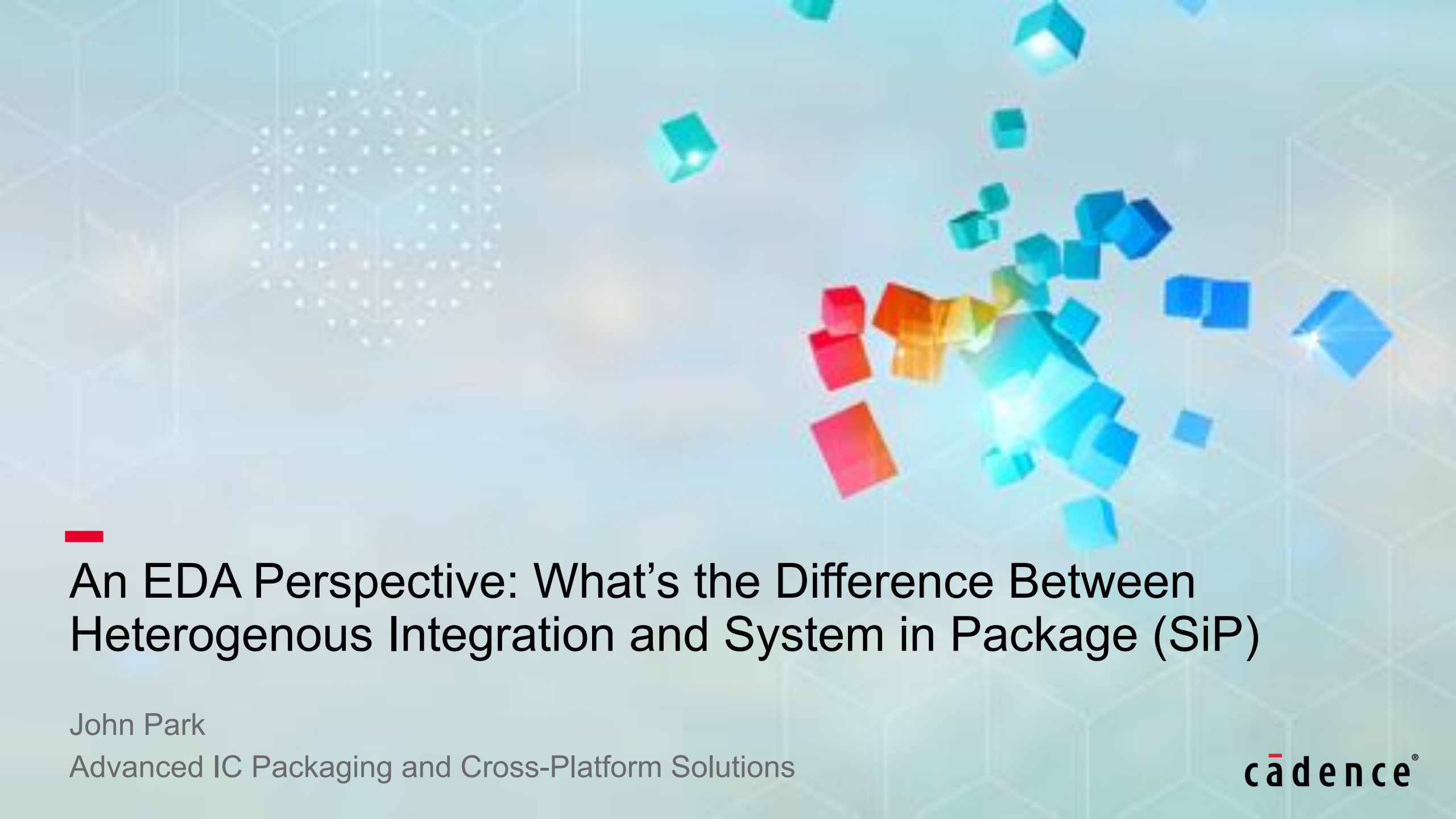# Semiconductor Industry Speaker Series

"An EDA Perspective:

What's the Difference Between Heterogenous Integration and System in Package (SiP)"

John Park

Cadence Design System

March 10, 2021

www.meptec.org   www.imaps.org

An EDA Perspective: What's the Difference Between Heterogenous Integration and System in Package (SiP)

John Park

Advanced IC Packaging and Cross-Platform Solutions
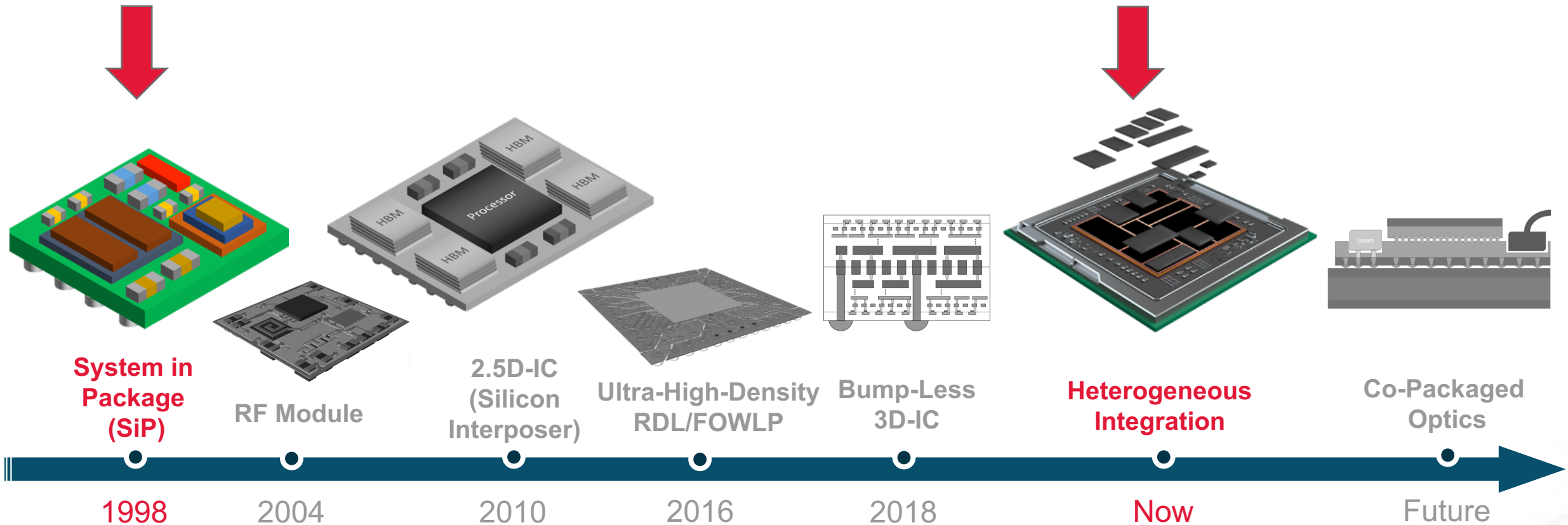
cādence®

Outline

Overview of SiP vs Heterogenous Integration

What's Driving Heterogenous Integration Trends
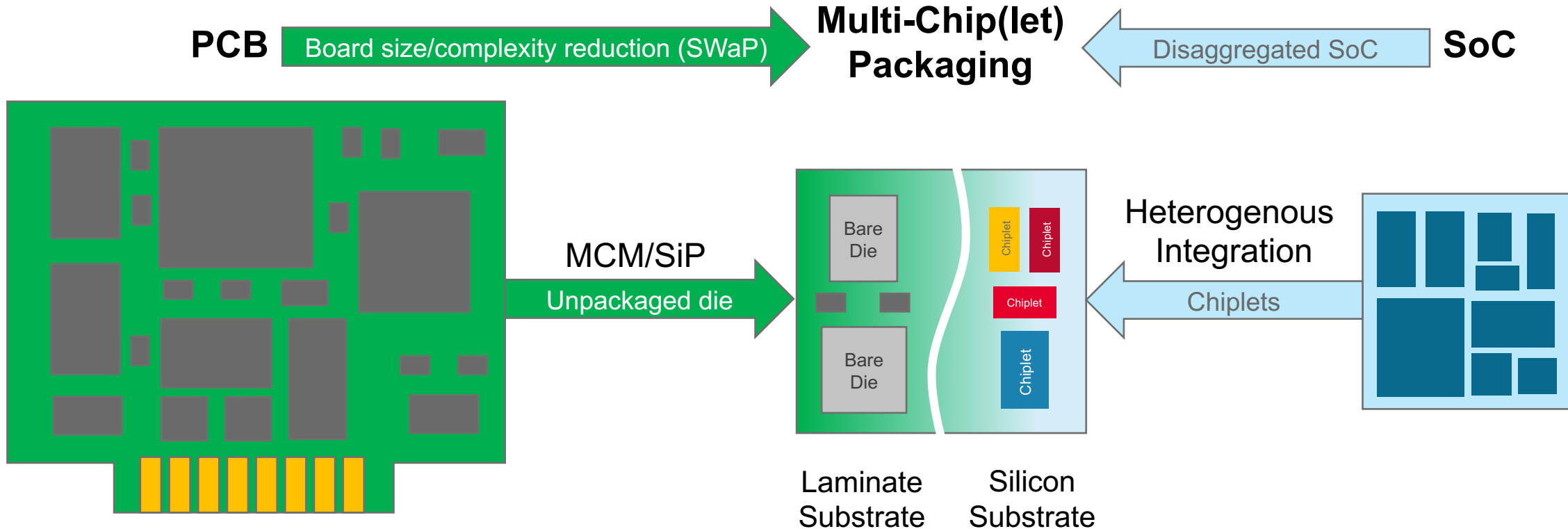
Design Challenges for Heterogenous Architectures

Design Flows for Next-Gen Packaging

cādence®

Evolution of Advanced Multi-Chip(let) Packaging Technologies

System in Package (SiP)

RF Module

2.5D-IC (Silicon Interposer)

Ultra-High-Density RDL/FOWLP

Bump-Less 3D-IC

Heterogeneous Integration

Co-Packaged Optics

| 1998 | 2004 | 2010 | 2016 | 2018 | Now | Future |

cādence®

SiP/MCM vs. Chiplet-Based (Heterogeneous Integration) Architectures
## New: The transition from system on a chip (SoC) to system in a package (SiP)

PCB → Board size/complexity reduction (SWaP) → **Multi-Chip(let) Packaging** ← Disaggregated SoC — SoC

MCM/SiP — Unpackaged die

Heterogenous Integration — Chiplets

Bare Die

Bare Die

Chiplet Chiplet

Chiplet

Chiplet

Laminate Substrate   Silicon Substrate

PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible architectures

cādence®

Heterogenous Integration is Just a Different Way of Logically Partitioning an SoC and is Independent of Packaging Technology

- Leveraging SiP design-style approach becoming a viable alternative to monolithic SoC
  - Modular approach vs monolithic approach
    - Not every logic function (IP) needs to be designed in the same process node (heterogeneous integration)
  - Leveraging IP in the form of chiplets
    - IP that is physically realized working on a standard communication interface
    - Similar to board-level design
  - Multiple options are available for "packaging" chiplets
    - Includes latest IC packaging 2.5D/3D-IC, FOWLP and embedded bridges

Integration Fabric

Memory

Processor

Accelerator

Ser Des

Analog
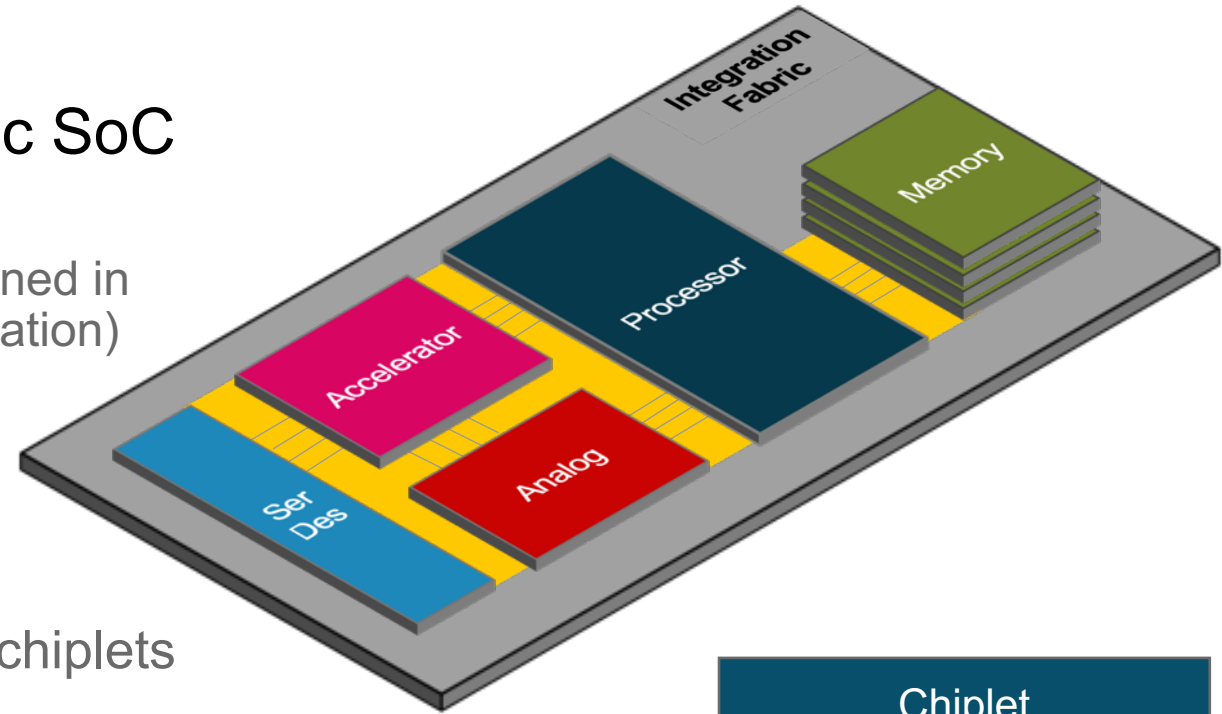
Hard IP

GDSII layout
Tied to specific technology/node

Soft IP

Synthesizable RTL
Gate-level netlist
Can be targeted to specific technology/node

Chiplet

Physically realized and tested (hardened) IP wrapped with micro-buffers driving standard communication interface, level-shifting, etc

cādence®

SiP vs. Heterogenous Integration

System in a Package (SiP)		
Simplify/shrink PCB	Higher performance, smaller form-factor	Much lower cost than transition to SoC
Schematic-driven PCB-like design flow	Little/no STA	Min/max/matched routing lengths
Moves devices closer together (unpackaged chips)	Shorter signal paths, less power	Bigger thermal challenge
	Flip-chip attach	100um-180um
	Bond-wire attach	Can be stacked
Integration fabric	Laminate/organic substrates	Ceramic (LTCC)

Heterogenous Integration		
Modularized/Disaggregate SoC	Reduced cost (relative to advanced node SoC)	Design/architecture flexibility and reduced time to market
Text/language driven IC-like design flow	Still requires formal IC-like sign-off process	Min/max/match interconnect to meet timing
Devices father apart (multiple chiplets)	Longer signal paths, more IO, larger form-factor	Bigger thermal challenge when 3D stacking
	Every chiplet is flip-chip-like attach	55um and smaller pitch
Targeted integration fabric	Silicon	Also, glass, embedded bridges & FOWLP

Why would we want to do this?
What happened to PPA?

cādence®

Outline

- Overview of SiP vs Heterogenous Integration
- **What's Driving Heterogenous Integration Trends**
- Design Challenges for Heterogenous Architectures
- Design Flows for Next-Gen Packaging

cādence®

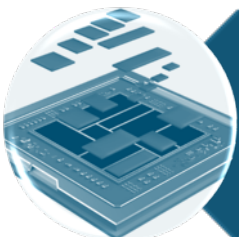# The End of Moore's Law & The Beginning of "More-Than-Moore"

For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore's Law. But things are changing…The economics of semiconductor logic scaling are gone…

Gordon Moore knew this day would come. He also predicted that *"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."*
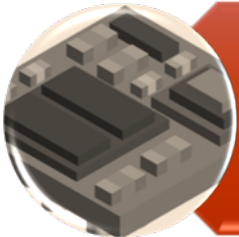
Providing a possible alternative to advanced monolithic SoCs, multi-chiplet SiPs have become a very attractive option for cost-sensitive complex designs

The generation of "More Than Moore" is here…

cādence®

The End of Moore's Law…Really?

- It's more than the limitations of physics…
- Cost per transistor has steadily increased since 2012/3 (28nm)
- Designing IC's at the latest nodes is hard and expensive
  - Low-volume businesses can't justify the NRE costs of designing an SoC at the latest node
  - Requires huge teams of engineering specialists that aren't always easy to find
  - Systems and software companies now designing chips and challenging the status-quo of SoC approach
- Today's SoCs are reaching reticle limits…but big chips typically don't yield anyways*
- More analog/RF content in today's designs
  - Analog/RF never have benefited from transistor scaling
  - Cost of Analog IP recertification at every node probably doesn't make sense in many cases

28nm

The End of Moore's Law?

2006 — 2008 — 2010 — 2012 — 2014 — 2016 →

Number of transistors per $

System on a Chip Design Costs ($M)

cādence®

Why Large Die Don't Yield?

Big Chips

Small Chips
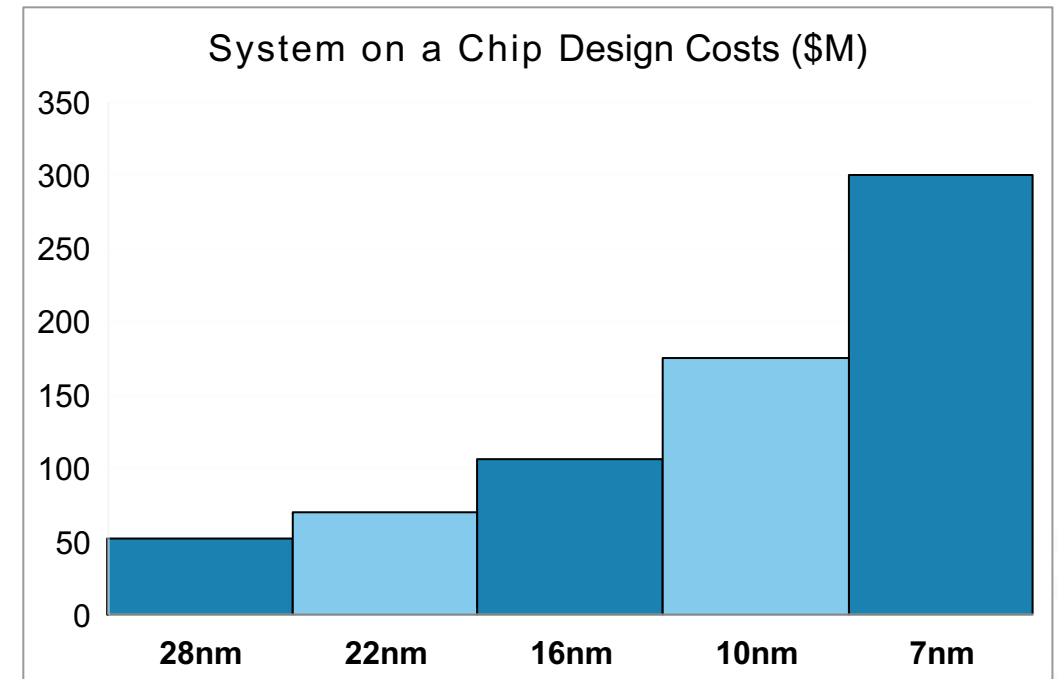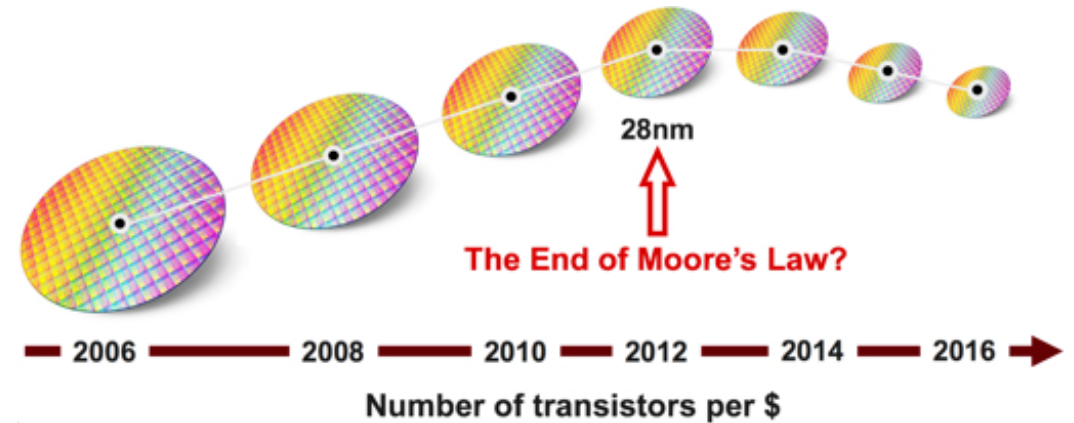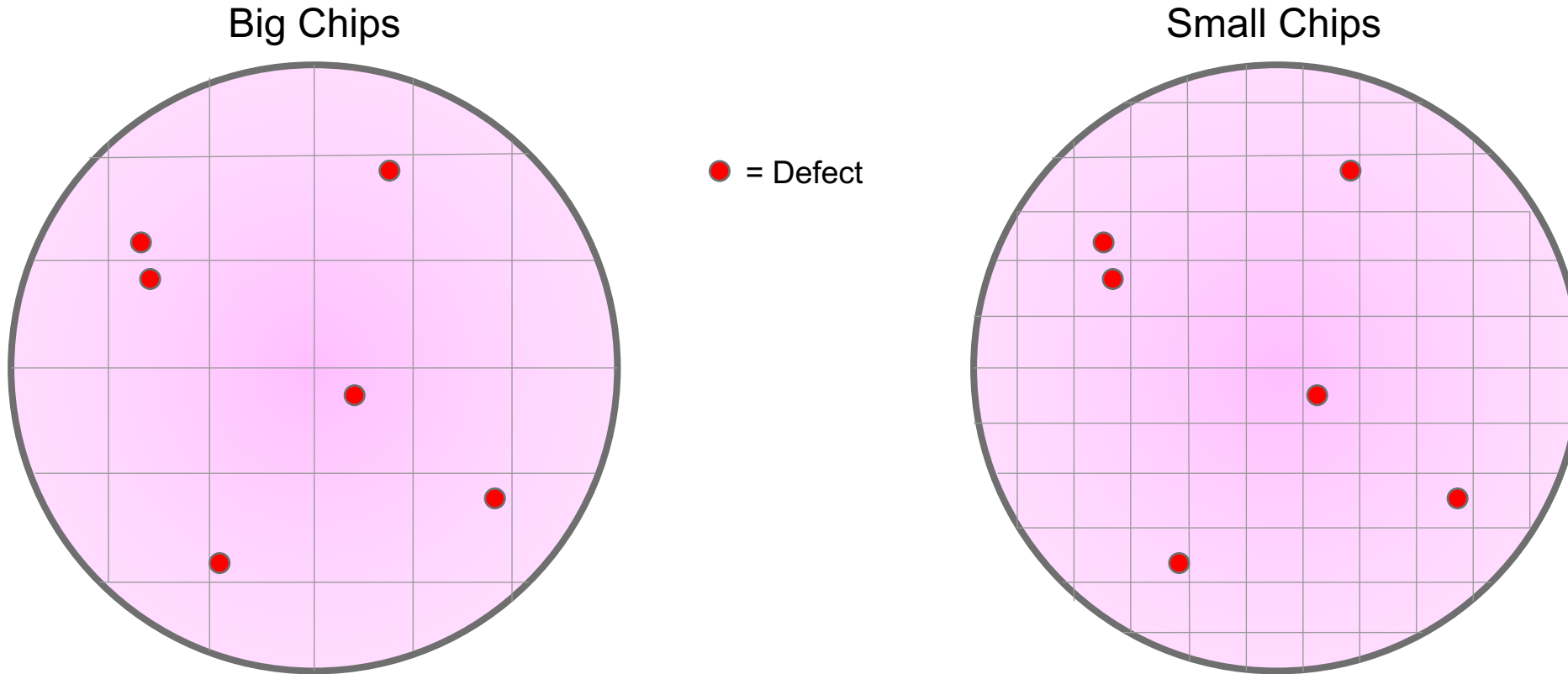
● = Defect

- Same size wafer, same number of defects:
  - The wafer on the left produces 10 working chips - (62% yield)
  - The wafer on the right produces 72 working chip(let)s - (92% yield)

cādence®

# Getting Your Chip Built, The Options Are Diminishing

130nm 2002 — 26
- ADI
- AMD
- Atmel
- Cypress
- Freescale
- Fujitsu
- Hitachi
- HLMC
- IBM
- Infineon
- Intel
- Mitsubishi
- ON
- Panasonic
- Renesas
- Rohm
- Samsung
- Sanyo
- Sharpe
- SMIC
- Sony
- STM
- TI
- Toshiba
- TSMC
- UMC

90nm 2005 — 18
- AMD
- Cypress
- Freescale
- Fujitsu
- IBM
- Infineon
- Intel
- Panasonic
- Renesas
- Samsung
- Sharpe
- SMIC
- Sony
- STM
- TI
- Toshiba
- TSMC
- UMC

65nm 2007 — 14
- Fujitsu
- GF
- HLMC
- IBM
- Intel
- Panasonic
- Renesas
- Samsung
- SMIC
- STM
- TI
- Toshiba
- TSMC
- UMC

45nm 2010 — 14
- Fujitsu
- GF
- HLMC
- IBM
- Intel
- Panasonic
- Renesas
- Samsung
- SMIC
- STM
- TI
- Toshiba
- TSMC
- UMC

32/28nm 2012 — 10
- GF
- HLMC
- IBM
- Intel
- Panasonic
- Samsung
- SMIC
- STM
- TSMC
- UMC

22/20nm 2014 — 7
- GF
- HLMC
- IBM
- Intel
- Samsung
- SMIC
- TSMC

16/14nm 2016 — 6
- GF
- Intel
- Samsung
- SMIC
- TSMC
- UMC

10nm 2018 — 3
- Intel
- Samsung
- TSMC

7nm 2020 — 3
- Intel
- Samsung
- TSMC

5/3nm 2022 — 2
- Samsung
- TSMC

cādence®

The World of IC Design Turns To Packaging…

3D Stacking is Old News
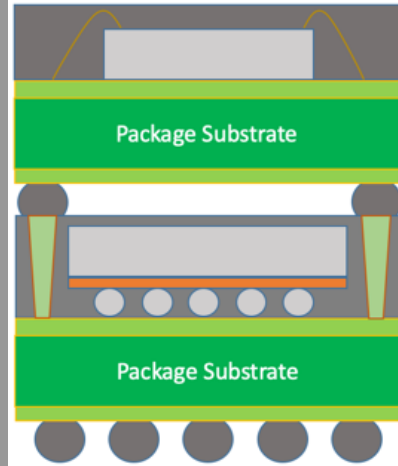
Package on Package (PoP)

Wire-bonded

Multi-Die Packaging is Decades Old
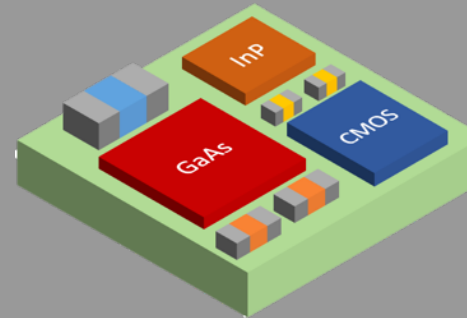
Multi-Chip-Module
MCM
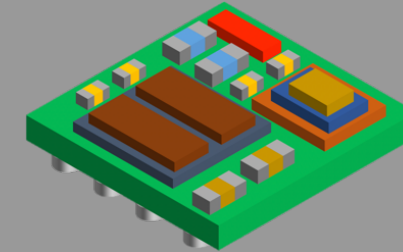
System-in-a-package
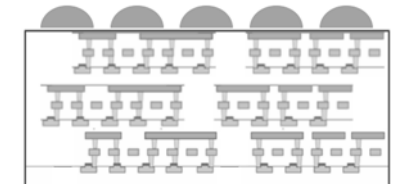SiP
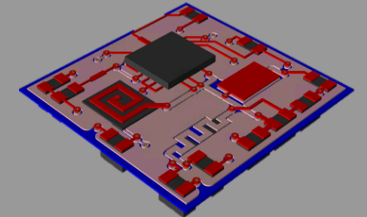
RF Module
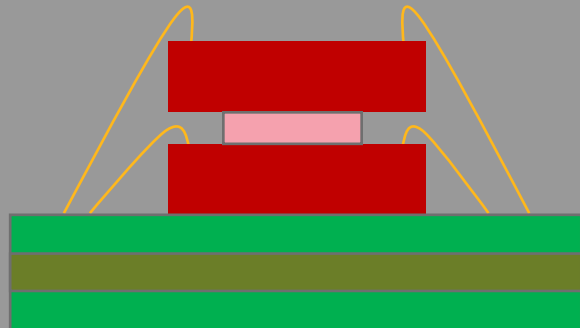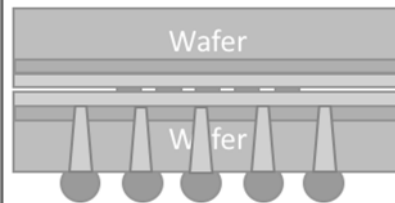
Wafer on wafer
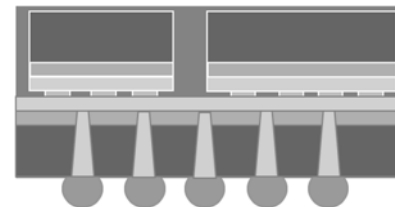
Chip(s) on wafer
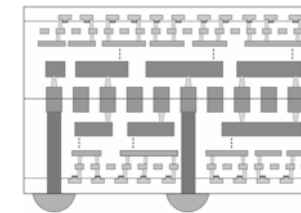
Bump-less

Monolithic 3D-IC
Transistor stacking

1998   2002   2015   2018   2020   Future

cādence®

Final Hurdles for Chiplets to Move into Mainstream
Commercialization/standardization of chiplets

- Today most chiplet-based designs are single vendor
  - Closed ecosystem

- The next step forward will likely require commercialization of chiplets
  - Standards and business model needed before IP companies proceed

- Ongoing work to define standards for chiplet-to-chiplet communication interface and data-exchange formats
  - Must be low power, low BER and low latency… No single PHY can do it all
  - Open Compute Project (OCP) and USG programs
    - BoW, OpenHBI, XSR, AIB, …
  - What about Analog/RF?
  - What about test/KGD? Who "owns" design yield?
  - Who manages chiplet inventory. Board part providers?

- Will compromised PPA be acceptable for all applications?

Interface Considerations Serial, Parallel or Proprietary
Package type
Reach
Power (pJ/bit)
Latency
Speed
Bandwidth
Routing complexity
Test, ESD, ???

	Monolithic SoC	Chiplet-Based
Cost	High	
Effort	High	
Risk	High	
Power		Acceptable?
Performance		Acceptable?
Area		Acceptable?

cādence®

Outline

- Overview of SiP vs Heterogenous Integration
- What's Driving Heterogenous Integration Trends
- **Design Challenges for Heterogenous Architectures**
- Design Flows for Next-Gen Packaging

cādence®

# Bottom Line…Design and Verification is Only Getting Harder

Transistor-level	Gate-level	ASIC	SoC	Heterogeneous Integration
1980	1990	2000	2010	Now
Functional	Functional	Functional	Functional	Functional
	Timing	Timing	Timing	Timing
		Power	Power	Power
			Reliability	Reliability
				System-Level
				Thermal
				Mechanical
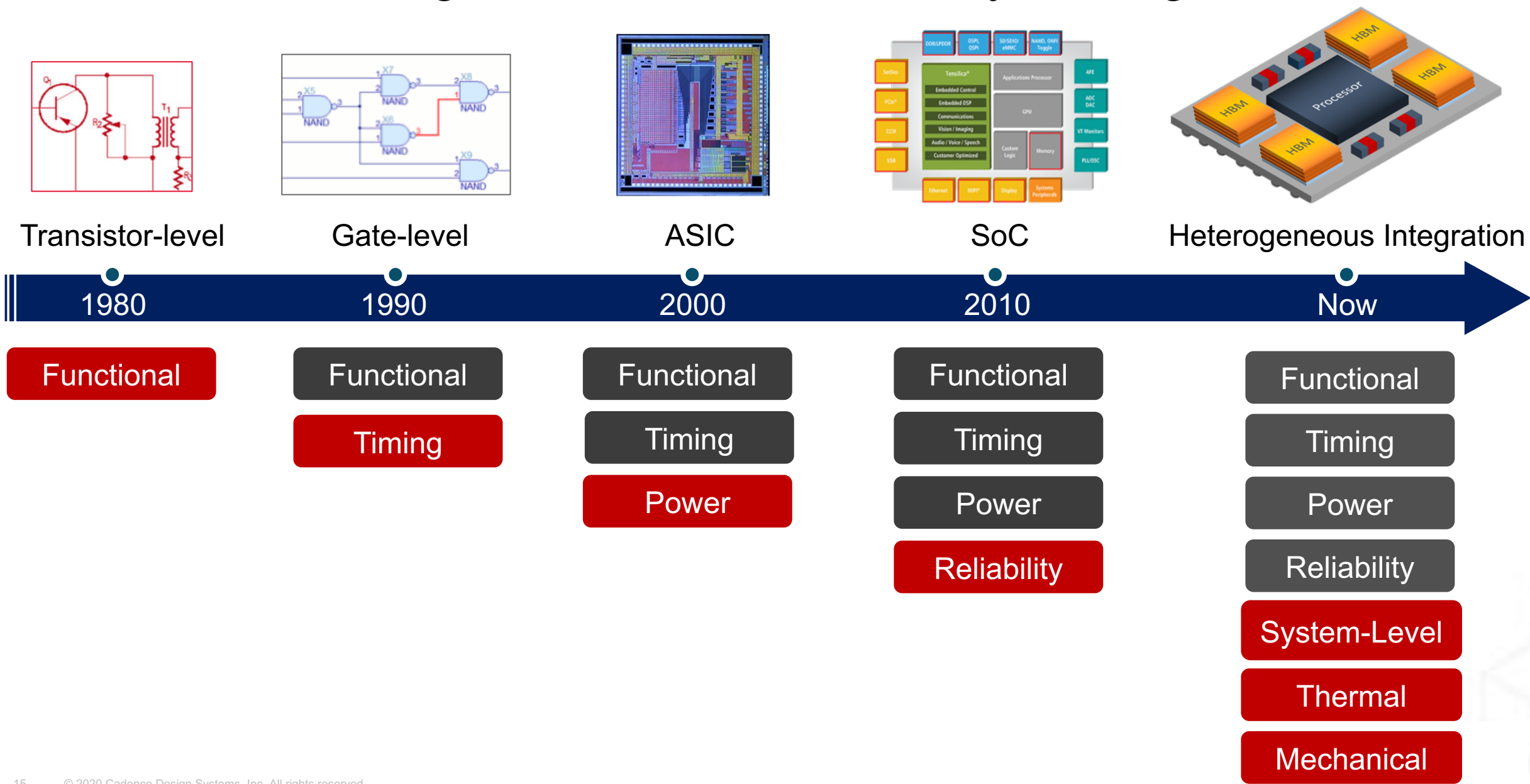
Design Tool/Flow Challenges for The Entire <u>Layout</u> Chain

- Requires design tools and flows that support cross-functional collaboration (co-design) for all design teams
  - Complete system-level visualization in a single tool
    - With the ability to optimize the system-level design and cross-domain interconnect
    - Pin-out and floorplan (including stack) optimization
    - Signal name aliasing across domains
    - Direct read/write into multiple layout domains and tools
  - Editing environment with user-specific design orientation
  - Cross-domain ECO loop
    - Domain-specific editing controls
    - Accept/Reject changes

System-Level View

Chip(let)-Level View

cādence®
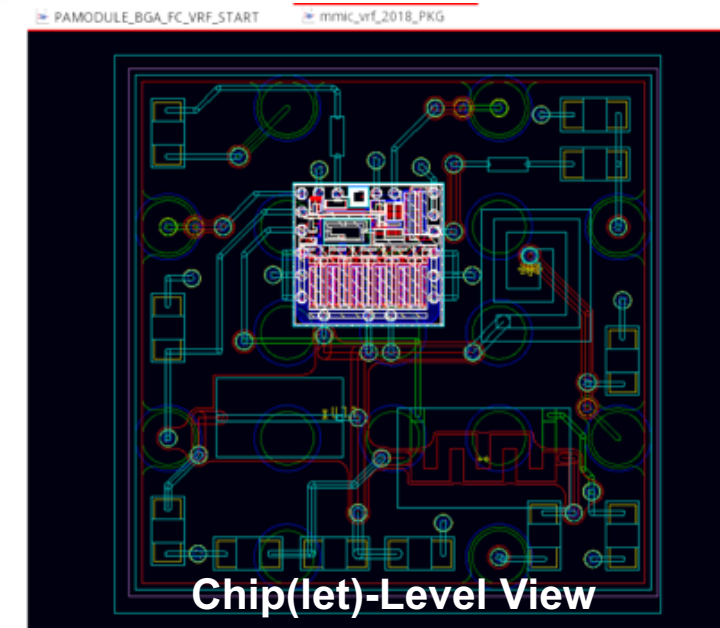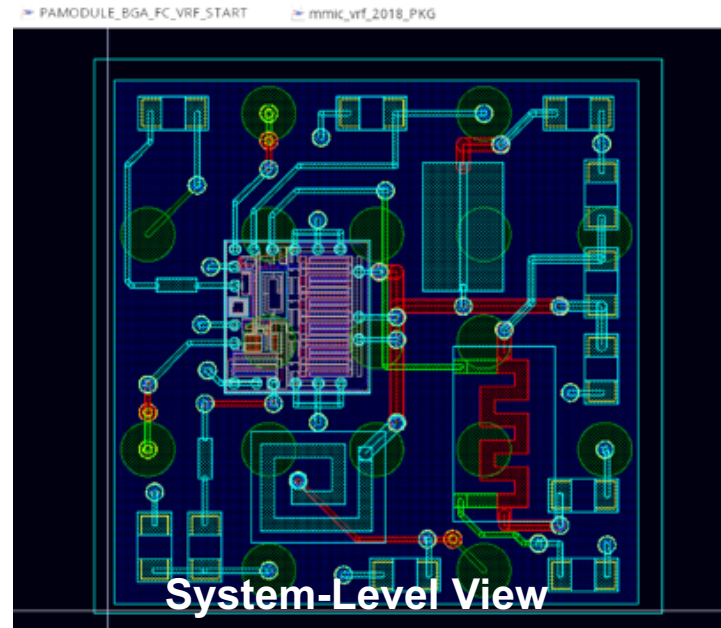
Design Tool/Flow Challenges for the Ecosystem

- Assembly Design Kits (ADK) Looking Beyond Design-Rule Manuals and Reference Designs…

TechFiles	Design Libraries	Assembly Rules	Compliance Kits	Manufacturing Rules	Rule Decks
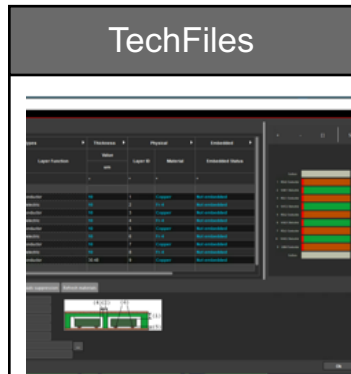
TechFiles

Layer stack-up
- Material
- Properties
- Thickness

Physical/Electrical layout constraints
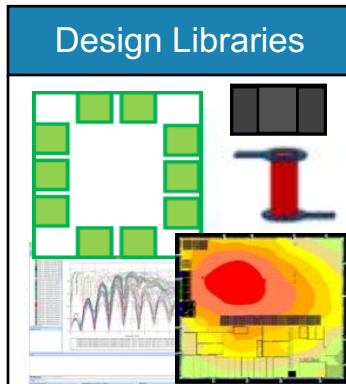
Design Libraries

Footprints
- Discrete
- BGA/LGA
- 3D Mechanical

Bond-Wire profiles

IO models

Thermal models

Power models
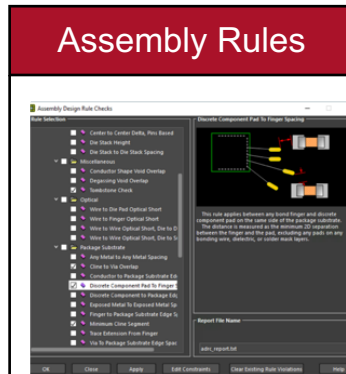
Assembly Rules

Device placement constraints based on assembly pick & place equipment
- Die to die spacing
- Device to device
- Device to obstacle

Compliance Kits

Electrical spec validation of chip(let)-to-chip(let) interfaces*
- Jitter tolerance
- Insertion loss
- Return loss
- Eye mask
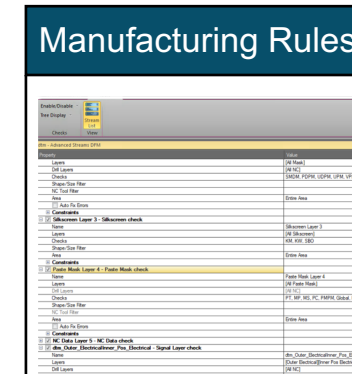
Manufacturing Rules

Board/substrate manufacturing process
- Substrate checks
- Soldermask checks
- Soldering issues
- Silkscreen checks

Rule Decks

Foundry/semiconductor manufacturing process
- DRC
- LVS
- Metal fill

cādence®

Design Tool/Flow Challenges for the Package Design Team

- Advanced multi-chip(let) silicon-based packages require specialized layout features and formal physical/logical verification capabilities

- Layout features specific to silicon substrate designs
  - Advanced filleting and trace widening
  - Progressive shape and pad degassing algorithms
  - High-capacity design support

- Mask-level accurate output data (GDSII) from substrate layout tool
  - Advanced arc vectorization

- Seamless integration with IC physical verification tool with feedback loop to layout
  1. Mask-level DRC
  2. Connectivity verification (LVS) of multi-chip(let) designs
  3. Region specific advanced metal fill (balancing)

cādence®
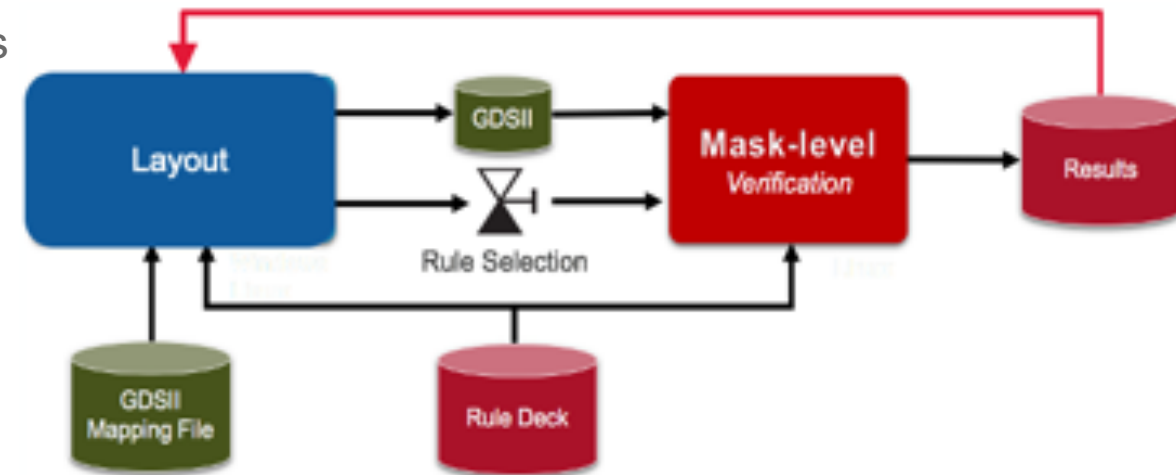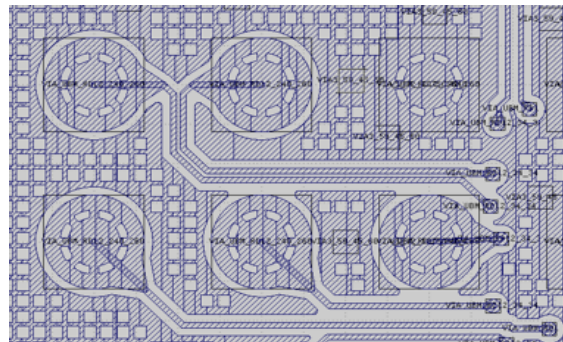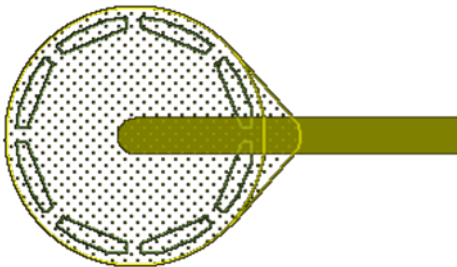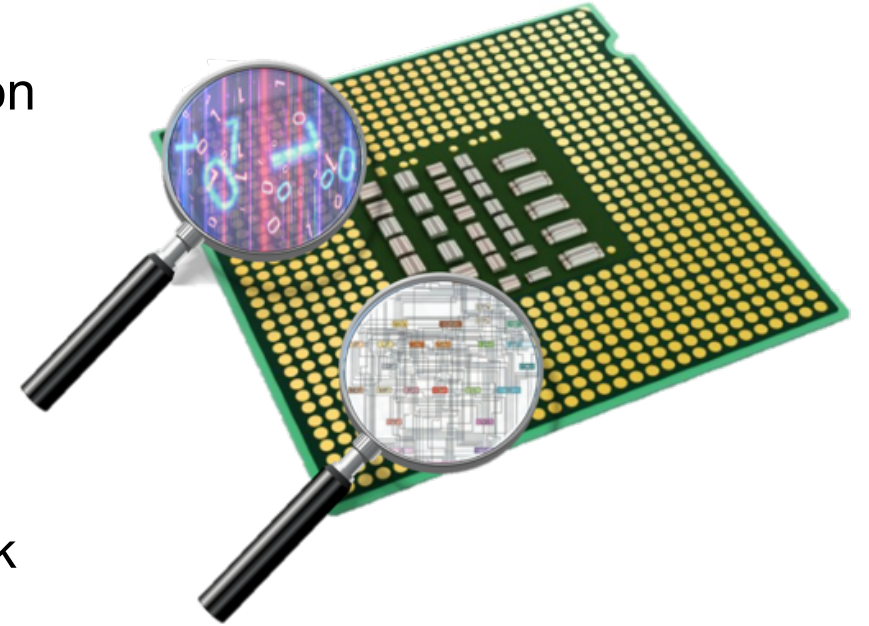
Design Tool/Flow Challenges for the IC Design Architect

- **Top-level design aggregation, management and system-level optimization**
  - Integrated with sign-off tools for stack alignment and layout vs schematic (LVS) checking
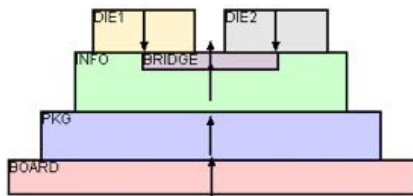
Stack Management
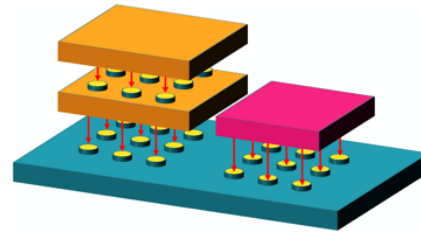
Interface Alignment Validation
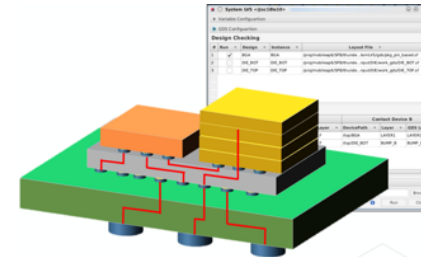
System-Level Connectivity Verification
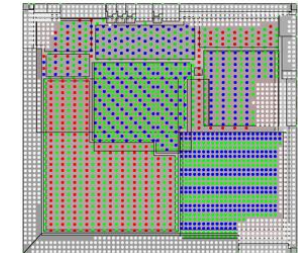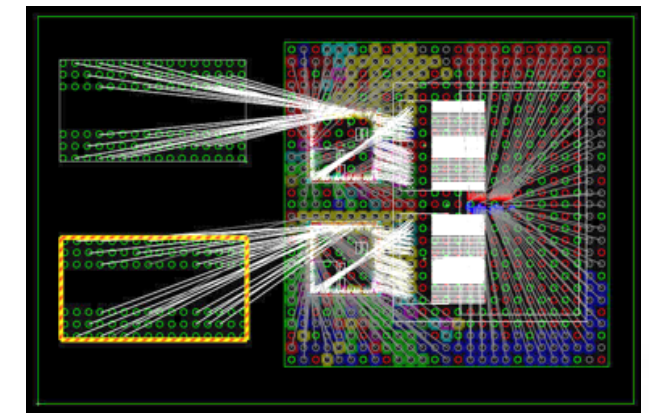

Advanced Bump/TSV Planning

Hierarchical Design Management
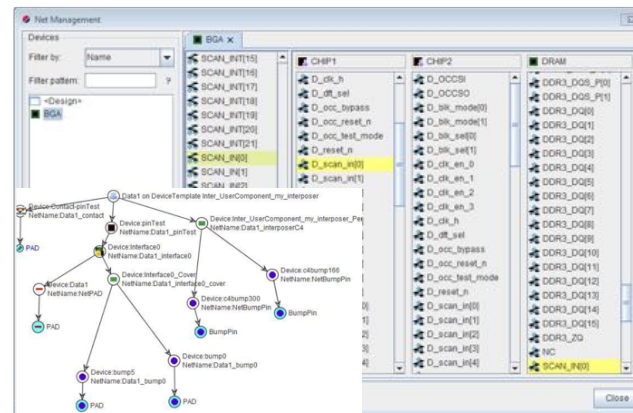

Hierarchical Signal Mapping

System-Level Connectivity Optimization

cādence®

Design Tool/Flow Challenges for Electrical/Thermal Analysis

- Analysis at the system level requires multiple simulation solutions
  - On-chip and off-chip EM modeling and analysis
    - Device, interconnect and antenna
    - Layout conditioning
  - Chip/package/board cross-domain coupling
  - Back-annotation to top-level design
  - In-design analysis and electrical sign-off verification
  - Thermal coupled with power analysis
  - Thermal self-heating coupled with CFD
  - Seamless integration with layout tools
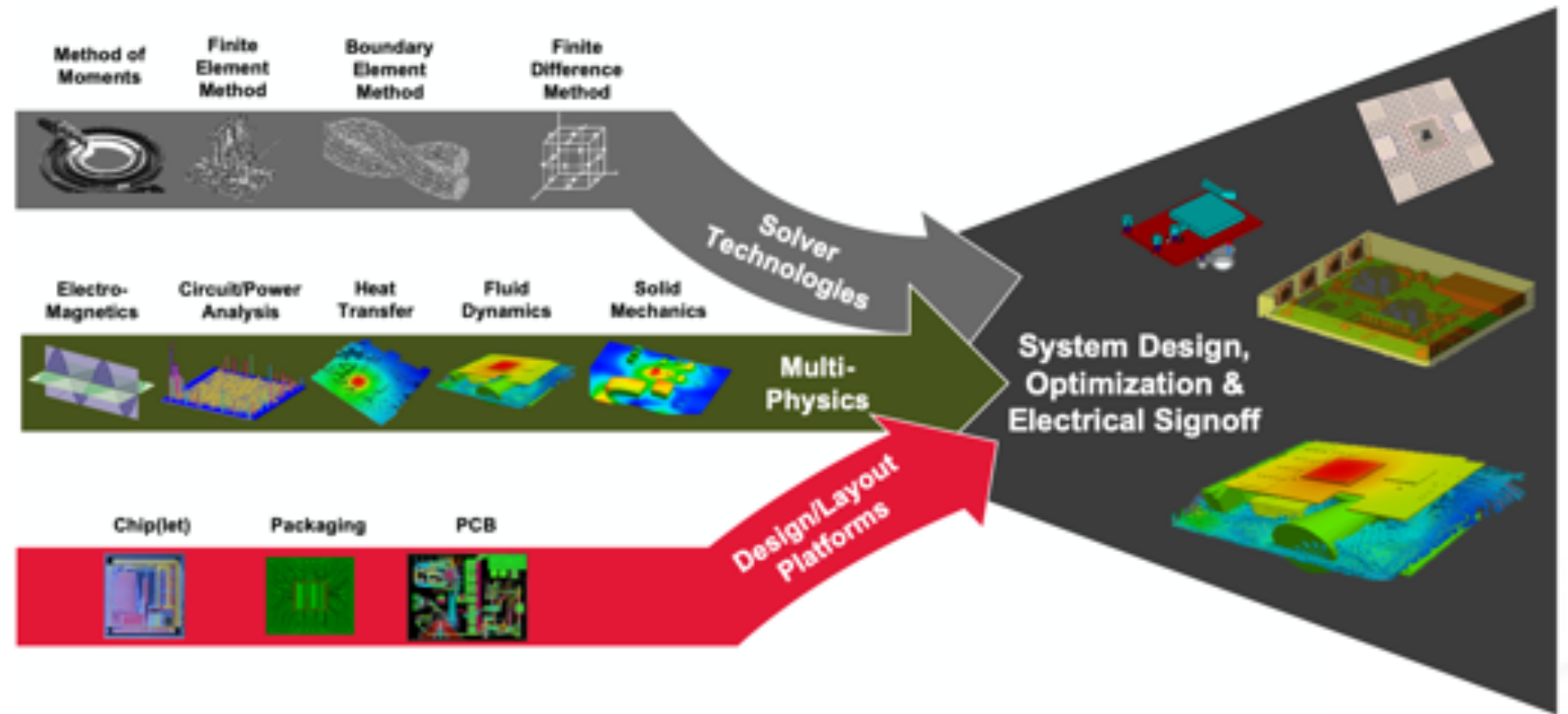
cādence®

Outline

- Overview of SiP vs Heterogenous Integration
- What's Driving Heterogenous Integration Trends
- Design Challenges for Heterogenous Architectures
- **Design Flows for Next-Gen Packaging**

cādence®
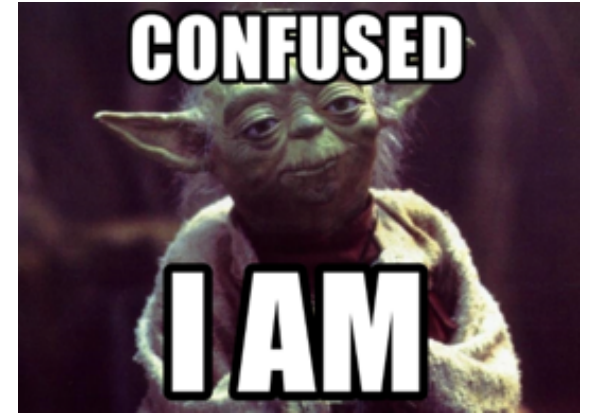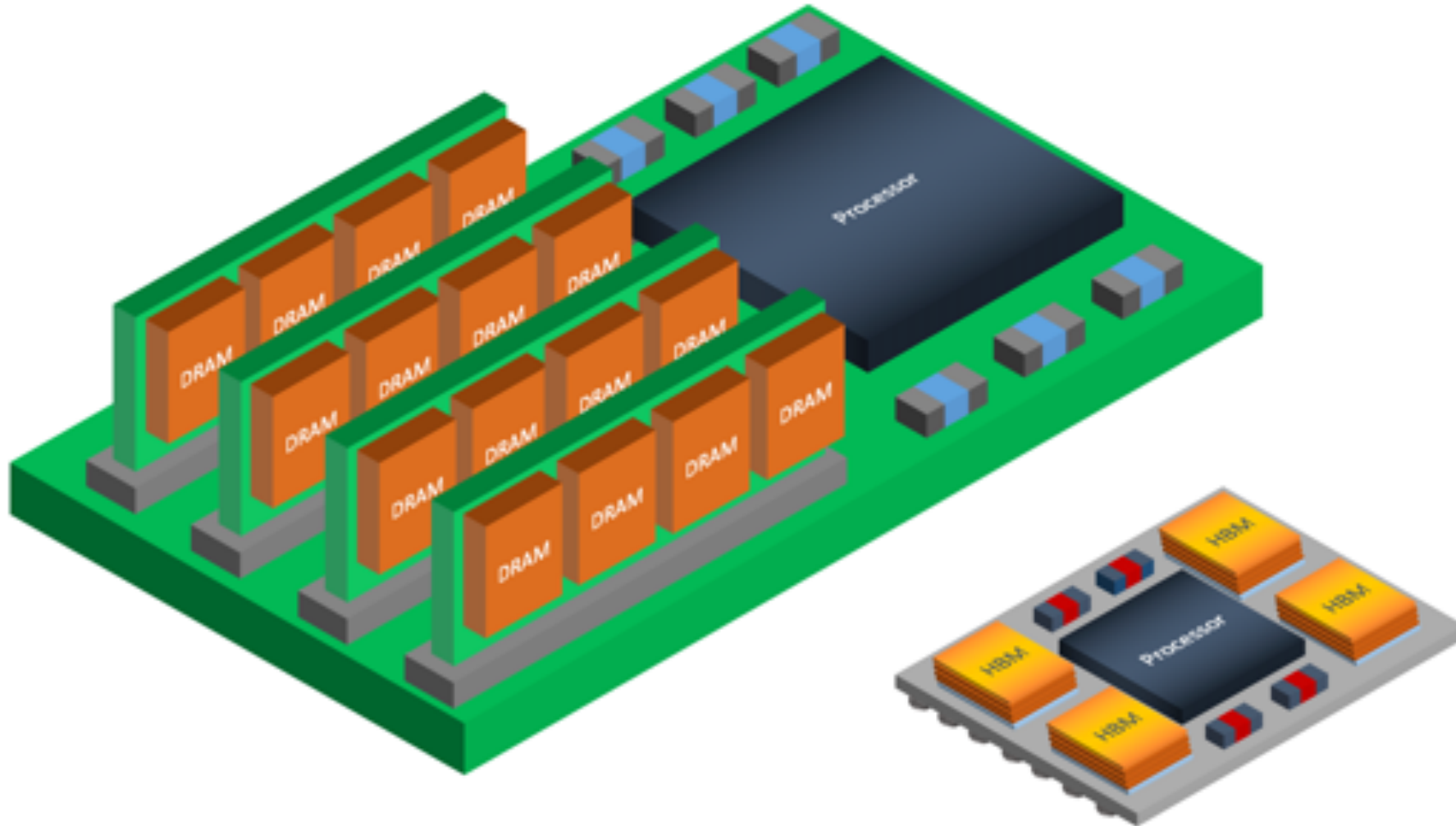
Transitioning to System-Level Design/Analysis Tools/Flows

Multi-Chip(let) Design Planning, Optimization and Management

Design Implementation

Multi-Chip(let) Electrical/Thermal Analysis and Sign-Off

Digital IC — Analog/RFIC/MMIC — Interposer — Fanout RDL — BGA/LGA — Stack

System-Level Design Planning and Aggregation

Top-Level Netlist

Die stack XML

Digital/SoC Design — *Analog/RFIC/MMIC Design* — *Multi-Chip(let) Package Design* — *Printed Circuit Board Design*

On/Off-Chip(let) Extraction — *Thermal Analysis* — *Signal/Power Integrity* — *Chip-Stack EM/IR* — *EMI Analysis*

cādence®

Example of System-Level Co-Design/Analysis Flow for HI

Automatic Parasitic Model Stitching

System-Level Unified Library

Hierarchical Top-Level Schematic Representing Complete System-Level Design

Multi-Chip(let) Layout

Thermal

Interconnect Parasitics

Device Models

Comp Def

Single Source Schematic Automates LVS

IC – Package Co-Design Flow

Multi-PDK Support

Simulation

PCB Layout

Mask-Level Physical Verification (DRC/LVS)

Tape-Out

Digital Chiplet

MWave Chiplet

Analog Chiplet

cādence

Question: What Is This?
It's Certainly "More Than Moore". But is it Heterogenous Integration?

cādence®

Conclusion

✓ We have entered the More-than-More era and electronic design will get harder

✓ SiP technologies being leveraged by IC designers to create heterogeneously integrated architectures

✓ New challenges face package designers and IC designers

✓ New design tools and flows will be required

cādence®

Packaging Technologies Being Targeted for Heterogenous Integration

Silicon Interposers (2.5D-IC)

Laminate BGA/LGA

Embedded Bridges

High-Density RDL (FOWLP)

Chip-on-Wafer Stacking (3D-IC)

cādence®

COPYRIGHT NOTICE

MEPTEC
THE NEXT GENERATION

www.meptec.org