Road to Chiplets: Architecture

July 13 & 14, 2021

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Road to Chiplets

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MEPTEC, Microelectronics Packaging & Test Engineering Council
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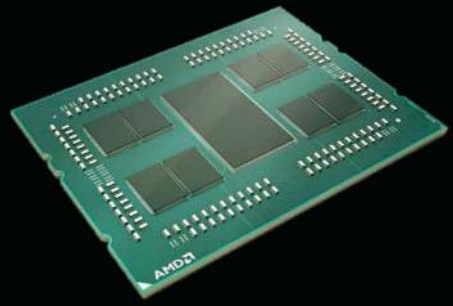
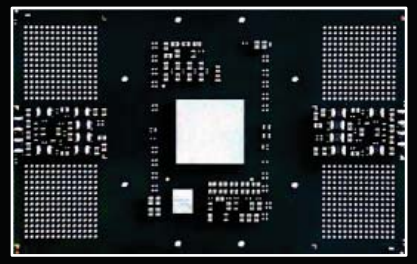
Why not only monolithic?

- Different functions don’t always want to be on the same chip:
  - IO function, RF, analog and memory
- Due to:
  - Technology fit
  - Schedule
  - Modularity
  - Cost
- Reticle starting to get “too small”

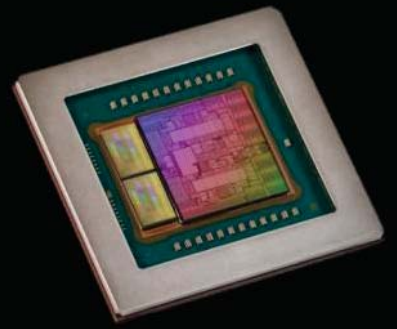
AMD Epyc™ 2 (Rome) processors



Data converters



HBM memory



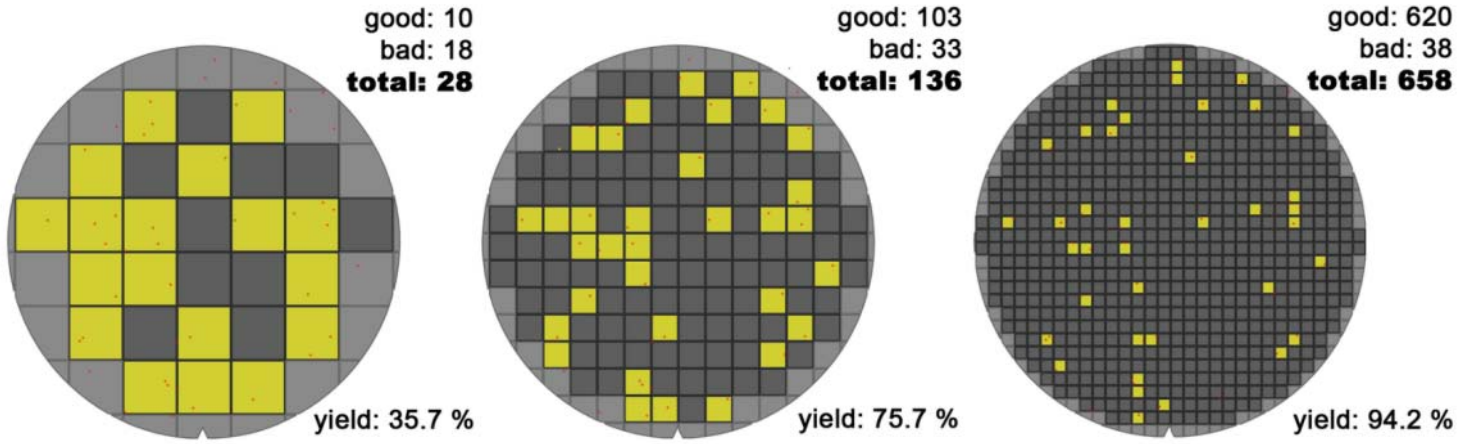
Modularity

Distributing functions between multiple dies

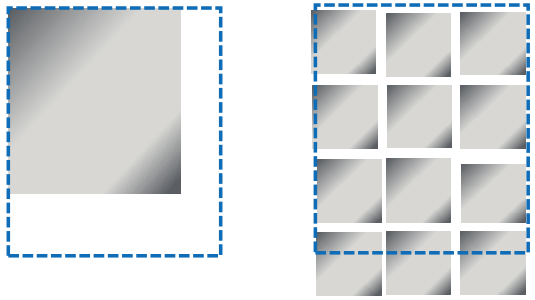
Breaking the problem to smaller pieces

Addressing the full reticle limitation

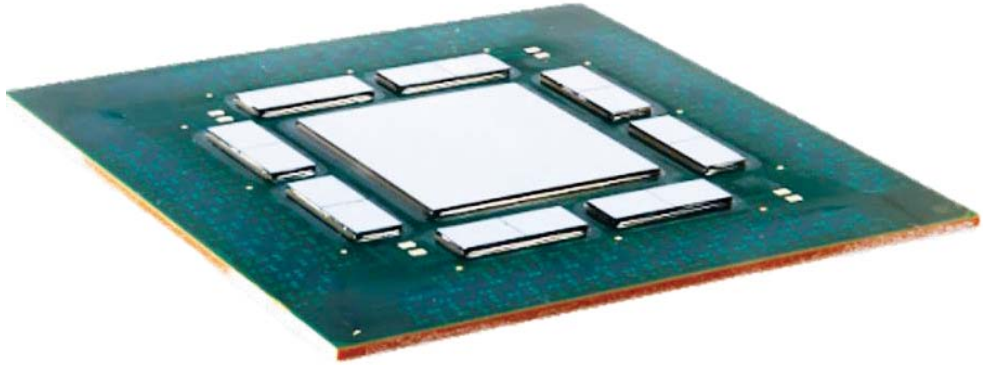
Overall yield improvement

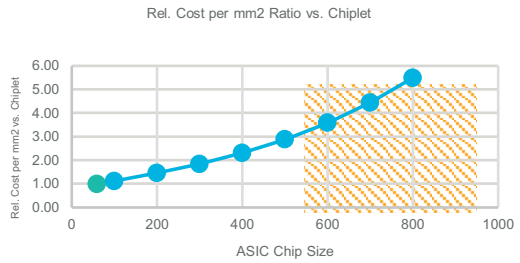


Marvell Switch



More silicon
than what
fits in a reticle



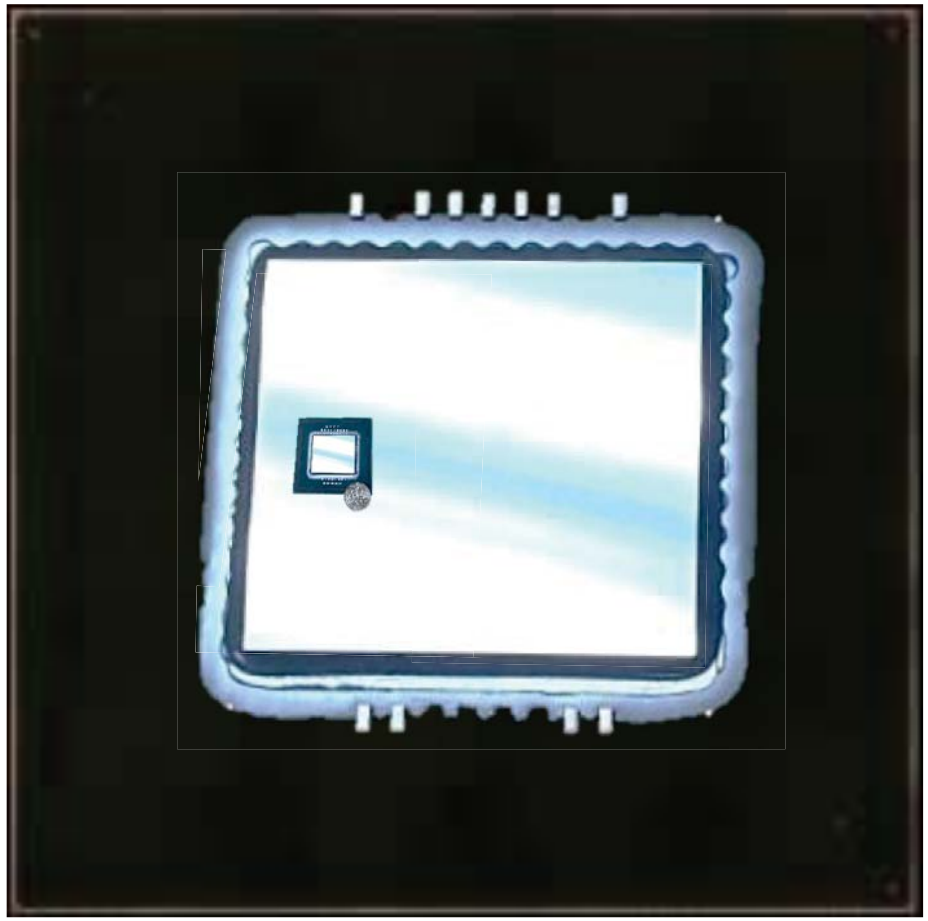


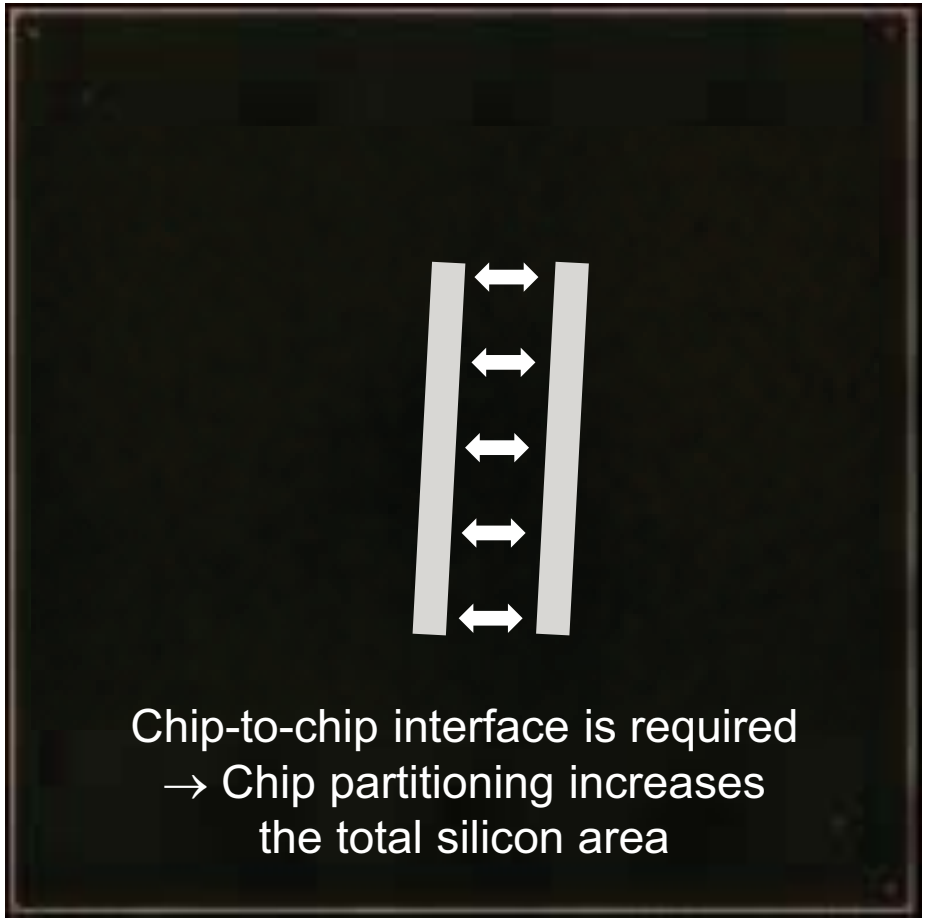
Smaller chips

Better yield

Lower cost

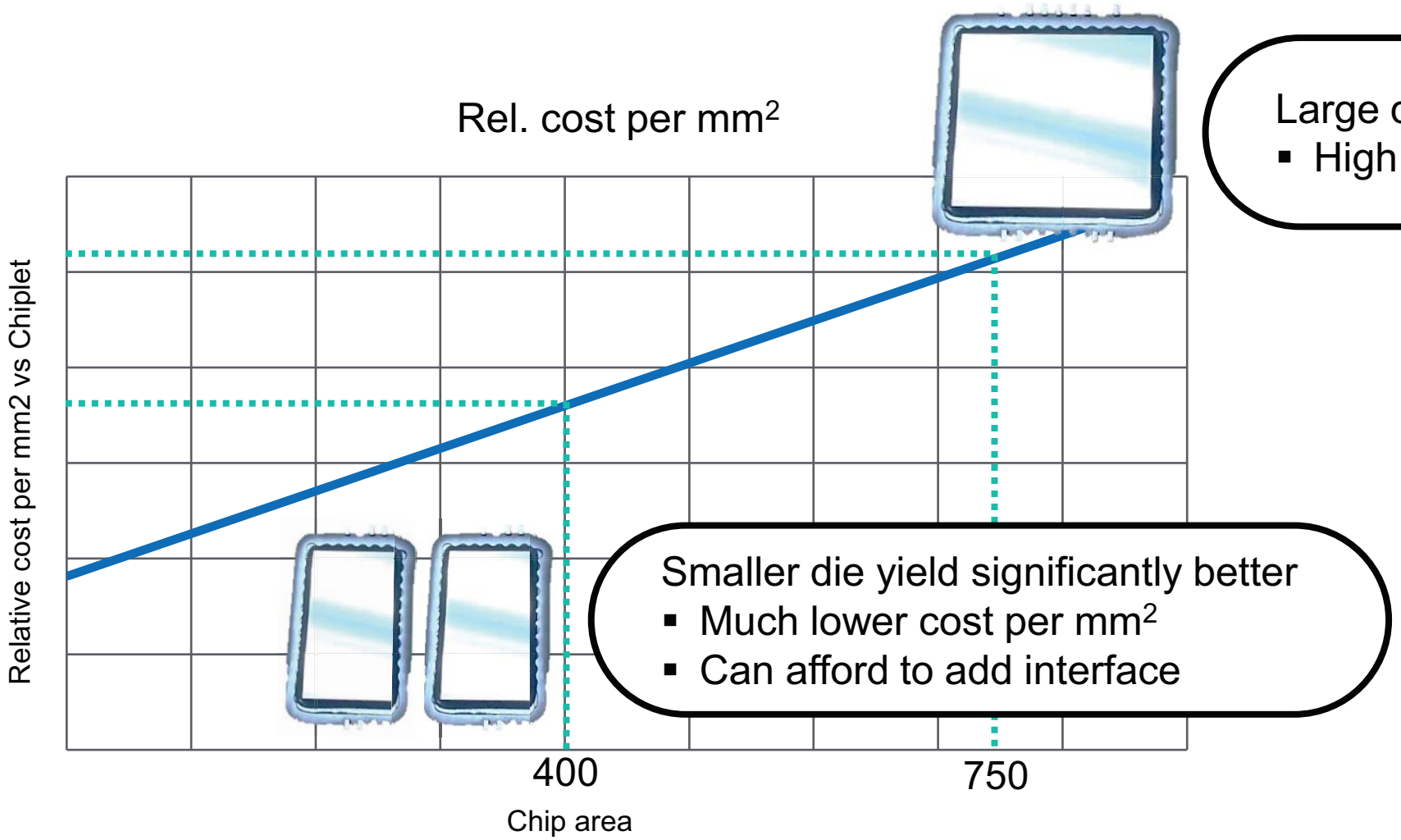
Partitioning and interfaces





Chip-to-chip interface is required
→ Chip partitioning increases
the total silicon area

Chiplets – Area vs. cost consideration

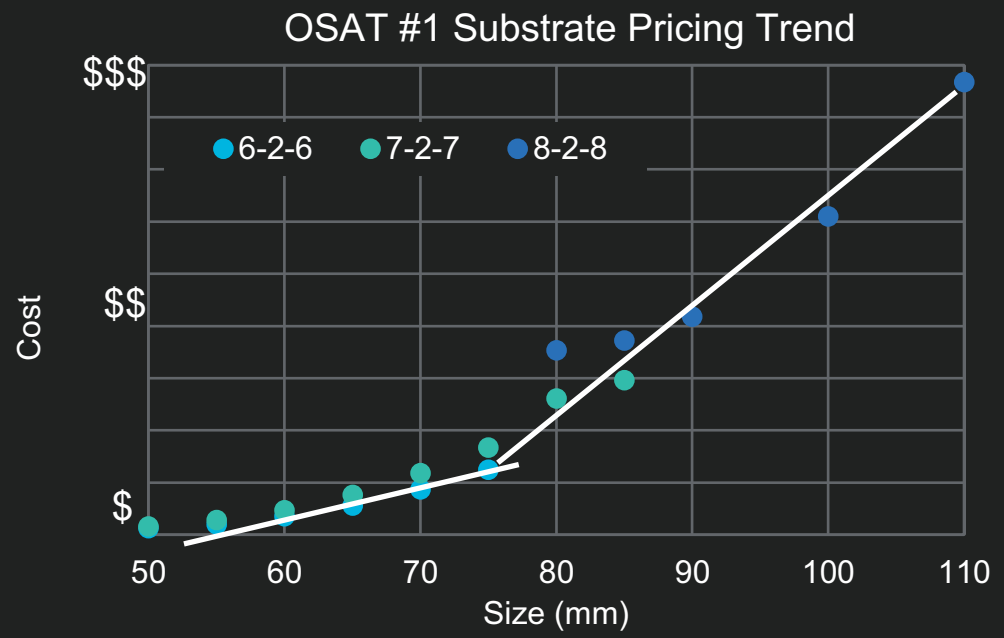


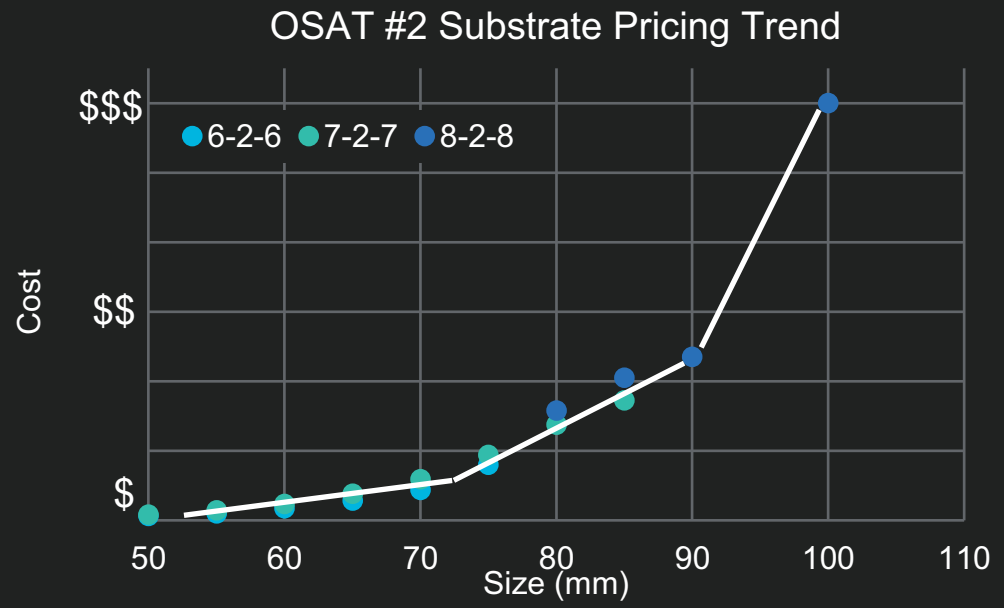
Large die yield poorly
- High cost per mm^2

Smaller die yield significantly better
- Much lower cost per mm^2
- Can afford to add interface

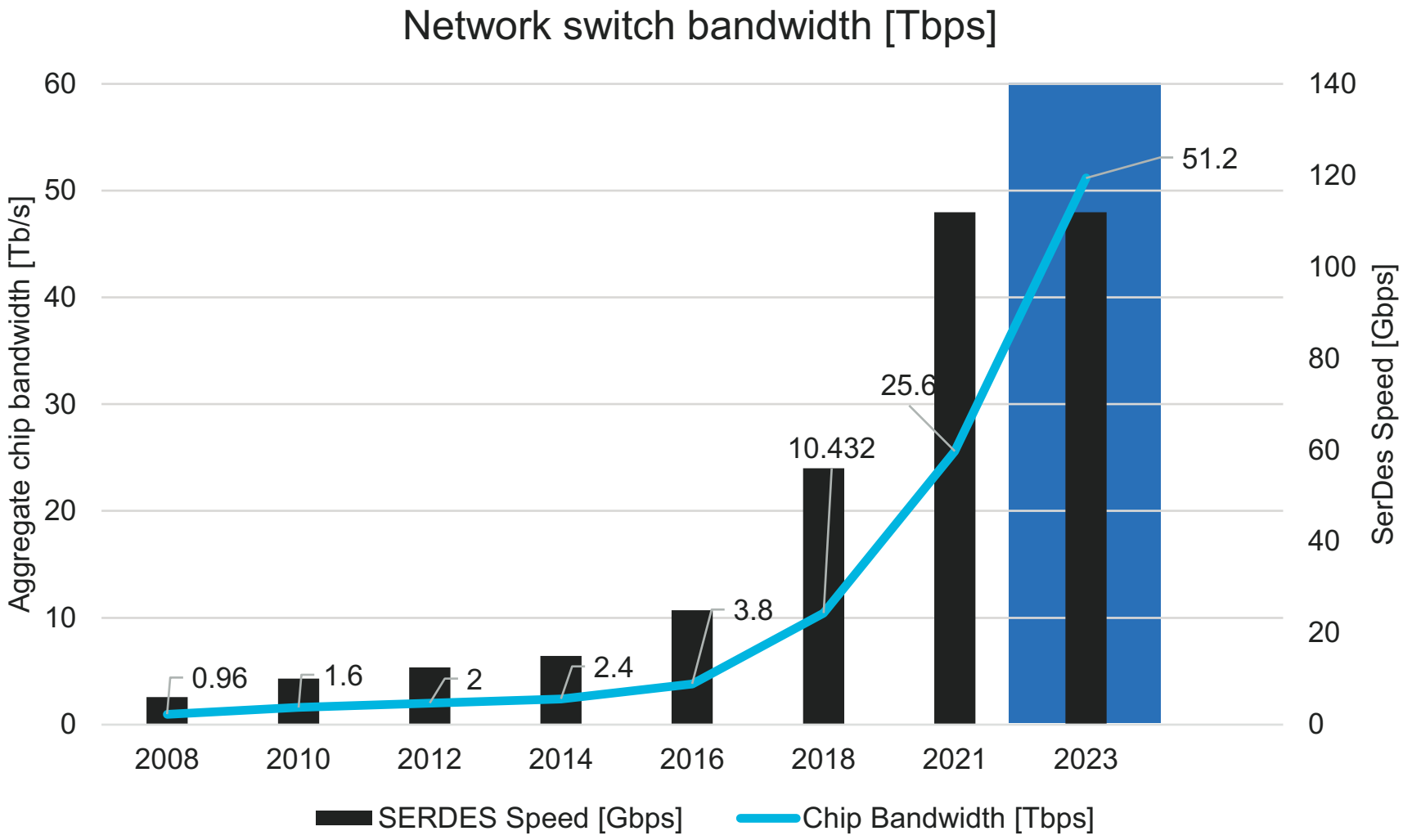
Package cost considerations

- Increasing % of overall product cost
- 2 key variables for substrate cost:
  - Size
    - Typically determined by # of I/Os & power needed
  - Build-up layers
    - Adding a layer increases substrate cost by 25-30%
    - Additional 2 layers (5-2-5 → 7-2-7) increases substrate cost by 55-70%
- Very large substrates are becoming increasingly expensive



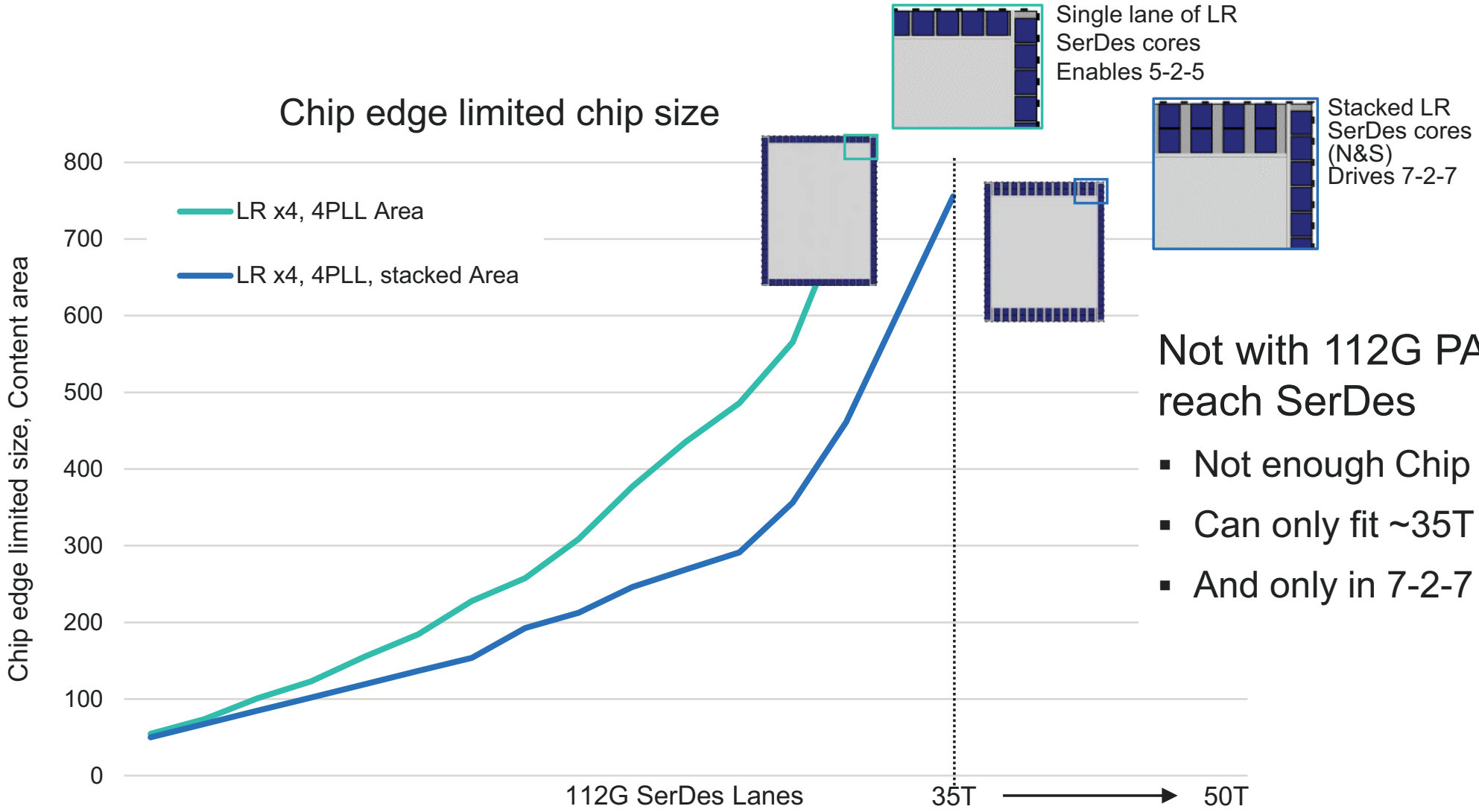


Next generation network switch – “50T”



- 50T network switch is around the corner
- Drives > 90mm package size
  - Unless we find other ways to get the data off the module

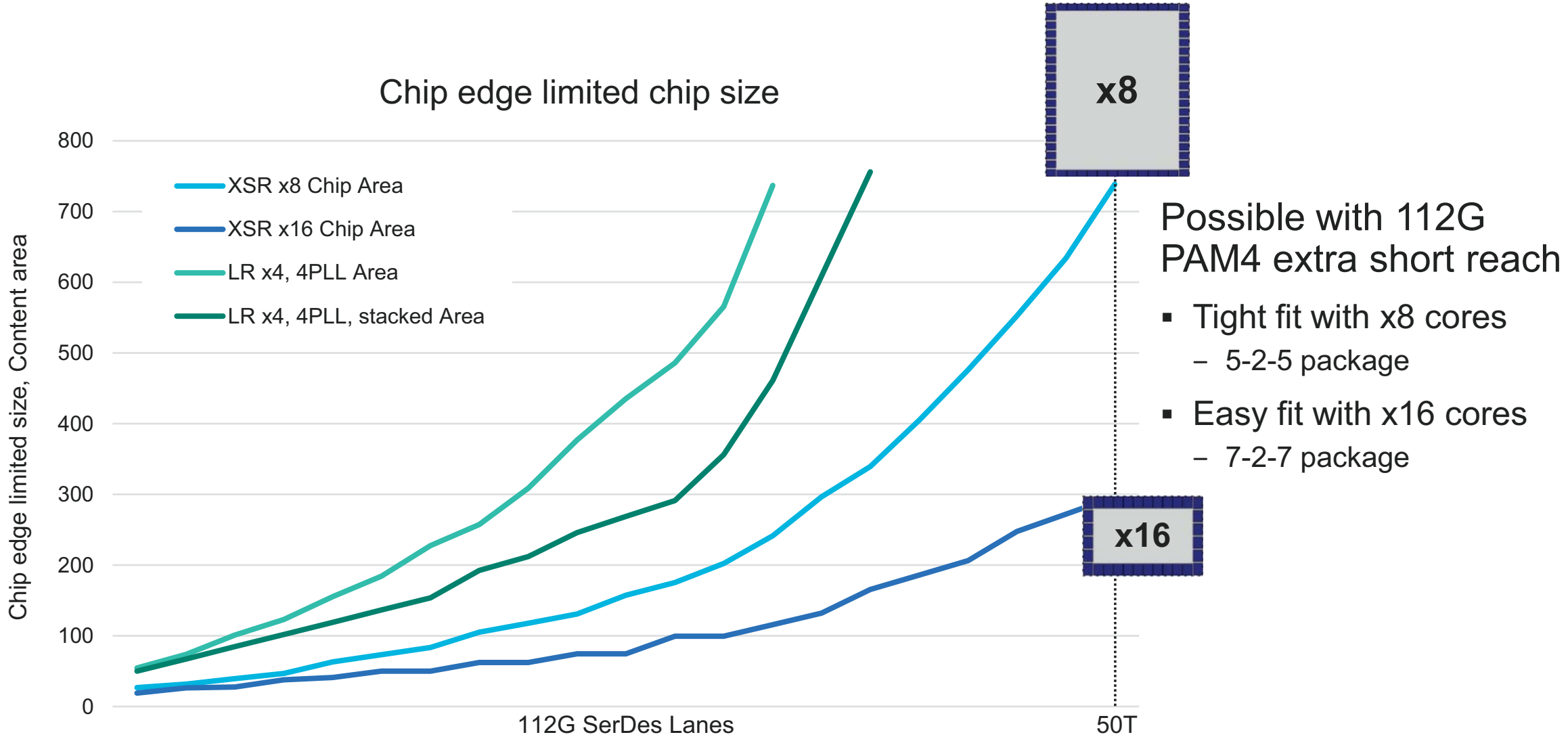
50T on one chip?



Not with 112G PAM4 long reach SerDes

- Not enough Chip edge available
- Can only fit ~35T
- And only in 7-2-7 package

50T on one chip!

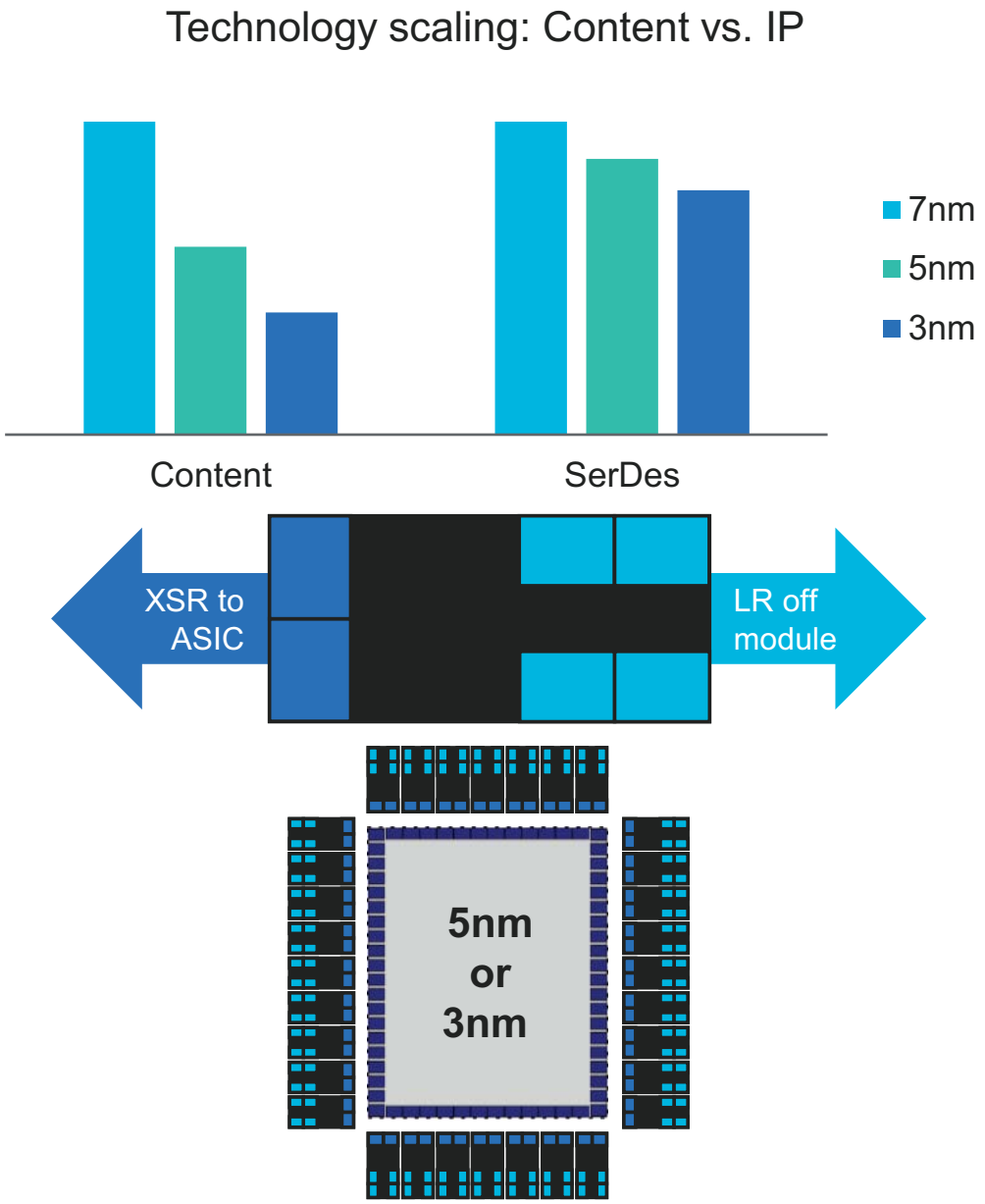


Possible with 112G PAM4 extra short reach

- Tight fit with x8 cores
  - 5-2-5 package
- Easy fit with x16 cores
  - 7-2-7 package

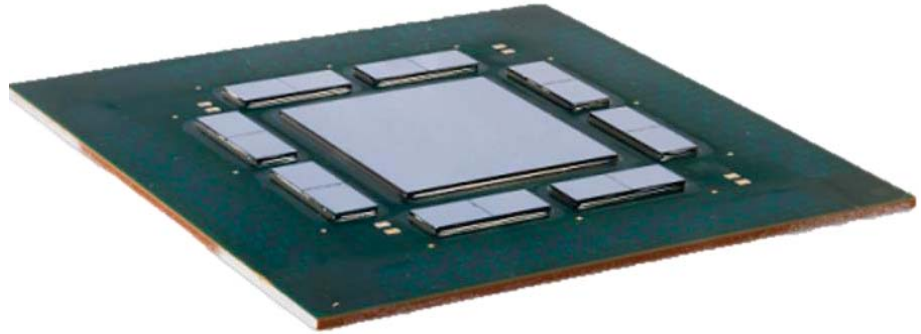
Chiplet time to market advantage

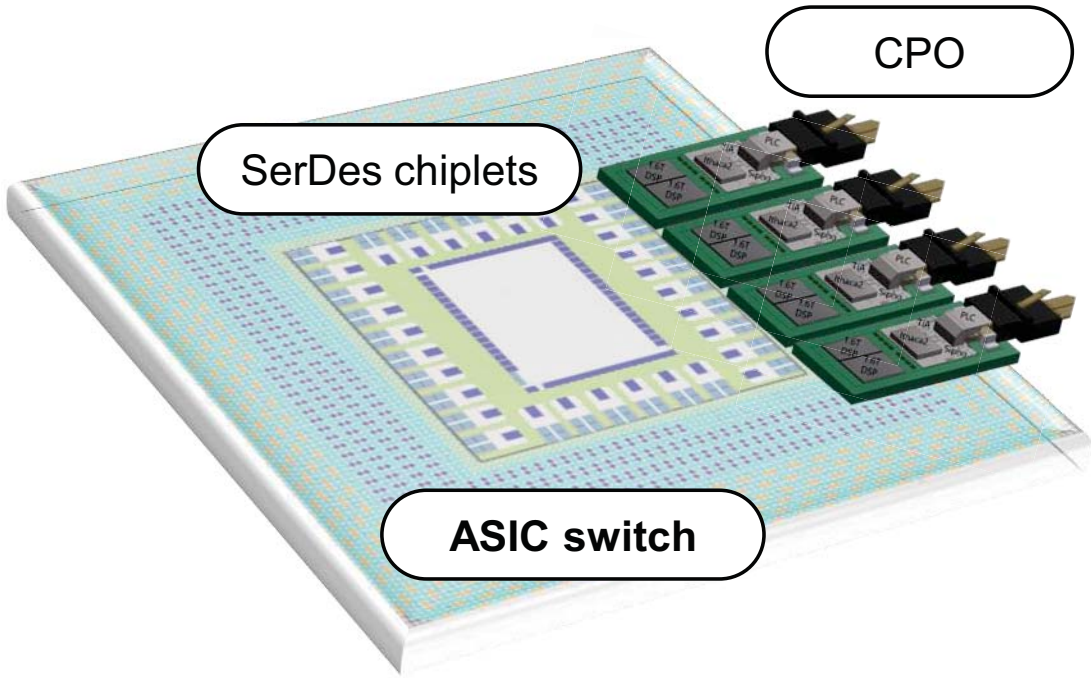
- Technology scaling
  - SerDes scaling benefits are relatively minimal in very advanced nodes
  - 3nm silicon cost, yield and IP availability will be challenging
- N-1 node
  - Interface IP available
  - Create (N-1)nm interface chiplets
- N node
  - Use XSR for ASIC-to-chiplet communication
  - Leverage (N-1)nm interface chiplets



Solutions for integrated optics

- Future of scalable systems
  - High bandwidth die-to-die interconnect
  - Chiplet based switching
  - SerDes technology
    - Low power / High bandwidth density
- Next generation optical interconnect
  - Proven Optical and DSP technology
  - Compact form-factor co-packaged optics (CPO)
    - Enabling scalable, future proof electrical to optical systems
    - Reduce power by moving the optics onto the package with the switch



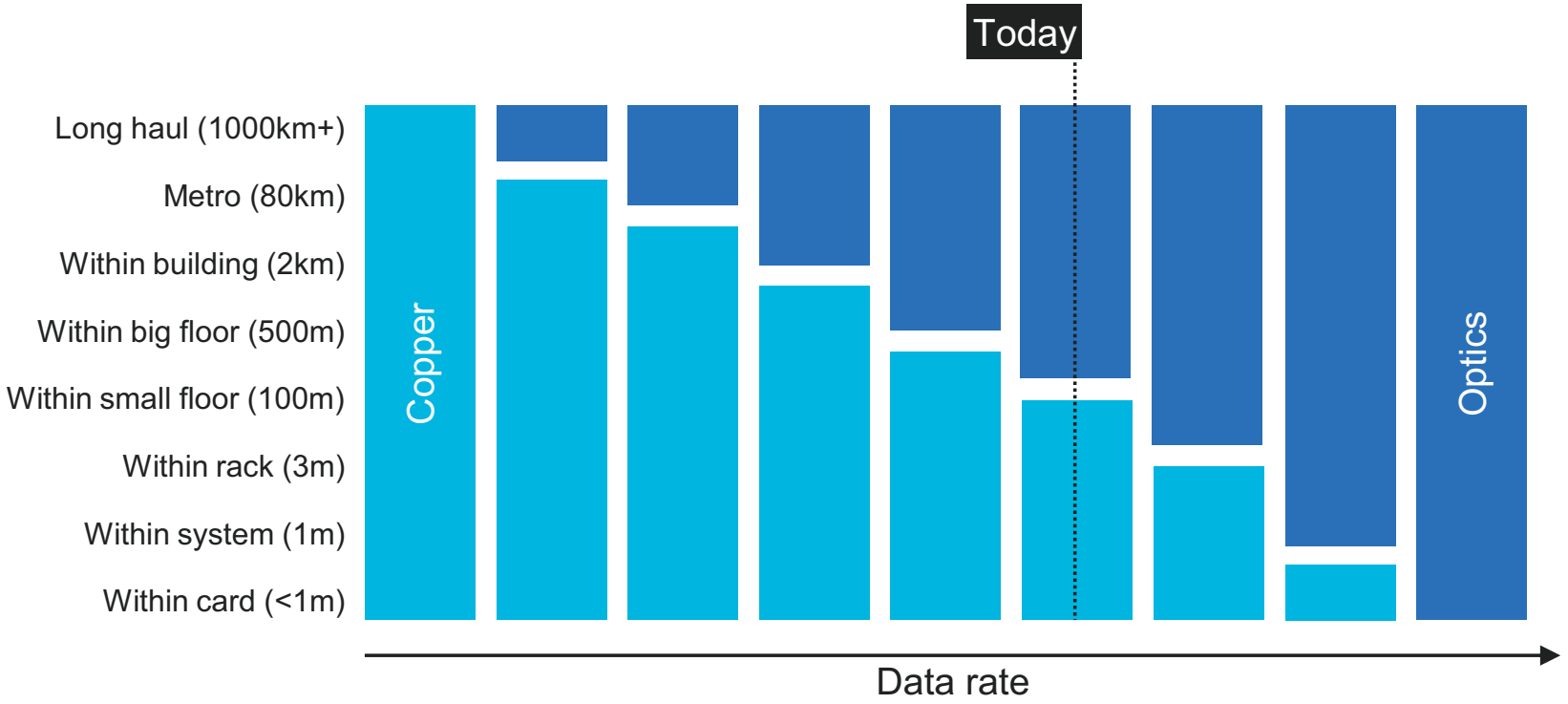


Global communication trends from copper to optics

Higher data rates and distance drive the move from copper to optics

Future innovations will only be possible with silicon and optical integration

Si Silicon + Op Optics

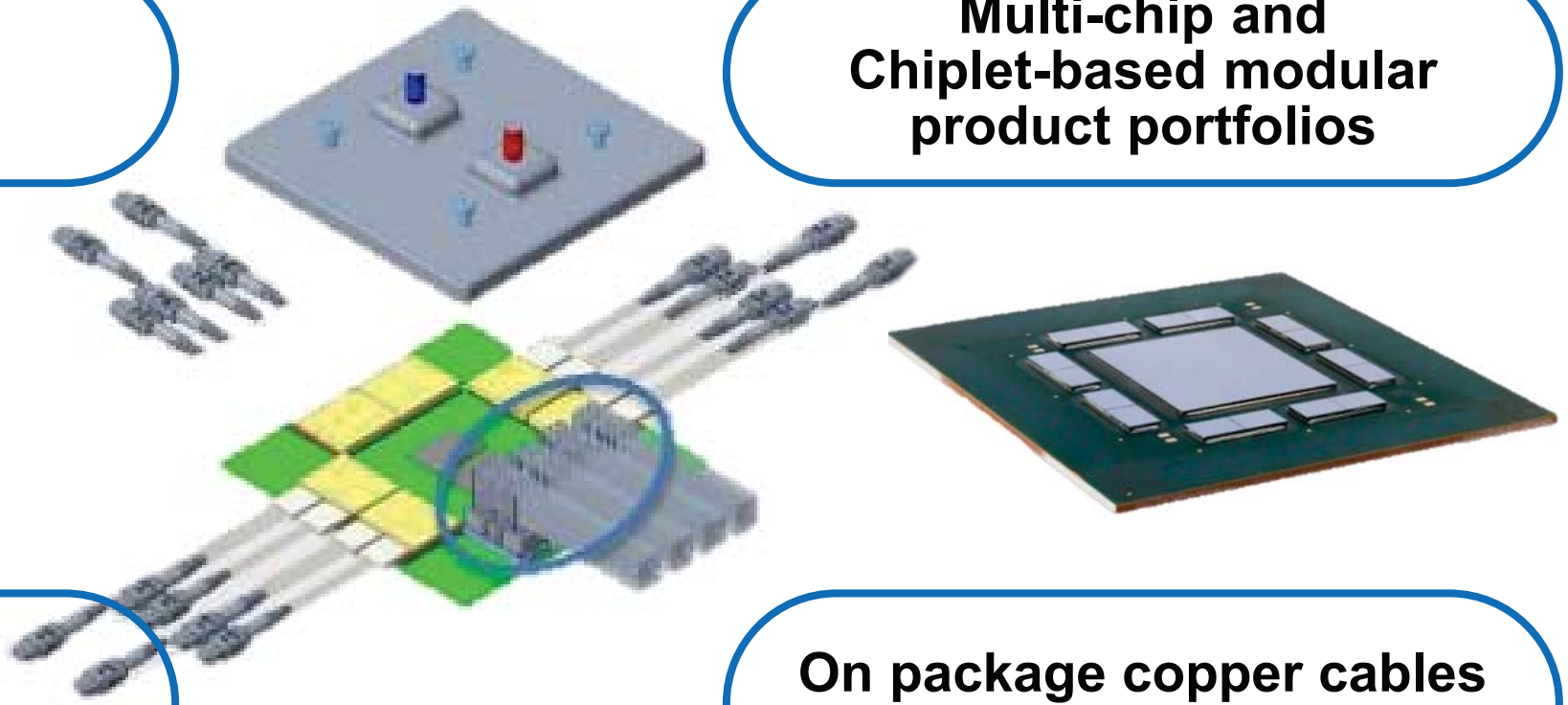


Source: https://blogs.cisco.com/sp/co-packaged-optics-and-an-open-ecosystem

Future Carrier and Data Center switching

Liquid cooling

Multi-chip and Chiplet-based modular product portfolios



Integrated co-packaged optics

On package copper cables Passive and active

Summary

- Chiplets and modular designs – for multiple reasons
  - Integrate content that doesn’t want to be on the same chip
  - Cost and yield
  - Schedule and IP availability
- Chip-to-chip Interface determines what package technology is needed
- Package complexity must be optimized to reduce total product cost
  - Co-optimization between architecture and package is critical
- Chiplets and advanced packaging provide path to co-packaged optics

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