Road to Chiplets: Architecture

July 13 & 14, 2021

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Chiplet Architectural Considerations for Adoption and Scaling

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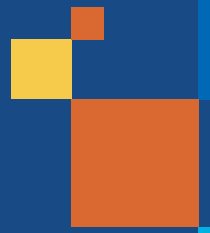
With numerous contributions from Intel's Chiplet Work Group (special thanks to Dave Kehlet, Tanay Karnik, Ramune Nagisetty, Peter Onufryk, and others)

July 14, 2021



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Moore's Predicted "Day of Reckoning"

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

-Gordon E. Moore

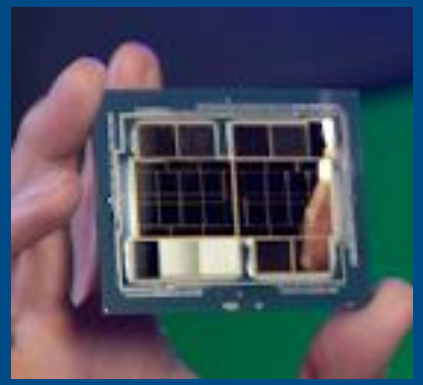
Image: Intel

[1]: "**Cramming more components onto integrated circuits**", Electronics, Volume 38, Number 8, April 19, 1965

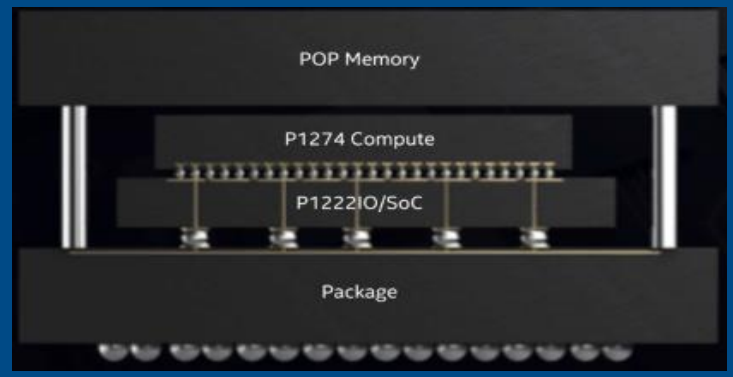
Some Intel Products Using Chiplets

- FPGAs

- Ponte Vecchio GPU



- Lakefield Client CPU



Growing Usage Across Multiple Product Families

Chiplet Approach Value Proposition

- Lower portfolio costs
  - Product cost (bigger chips with higher yields, less wasted silicon, better align delivered IP to optimal manufacturing process and related heterogeneous integration benefits, etc.)
  - Project costs (more configurations with fewer die developments, internal and external reuse with easier customization, reduced IP porting expenses, etc.)
- Scale innovation and delivery capabilities
  - Granular leverage of die and process-locked IP from internal and external sources
  - Granular leverage of manufacturing capabilities and capacity
  - Access 3D stacking benefits (XY area reduction, placing memory closer to logic)
- Reduce time to solution
  - Reuse, reduce process availability/maturity and IP porting schedule and ramp risks

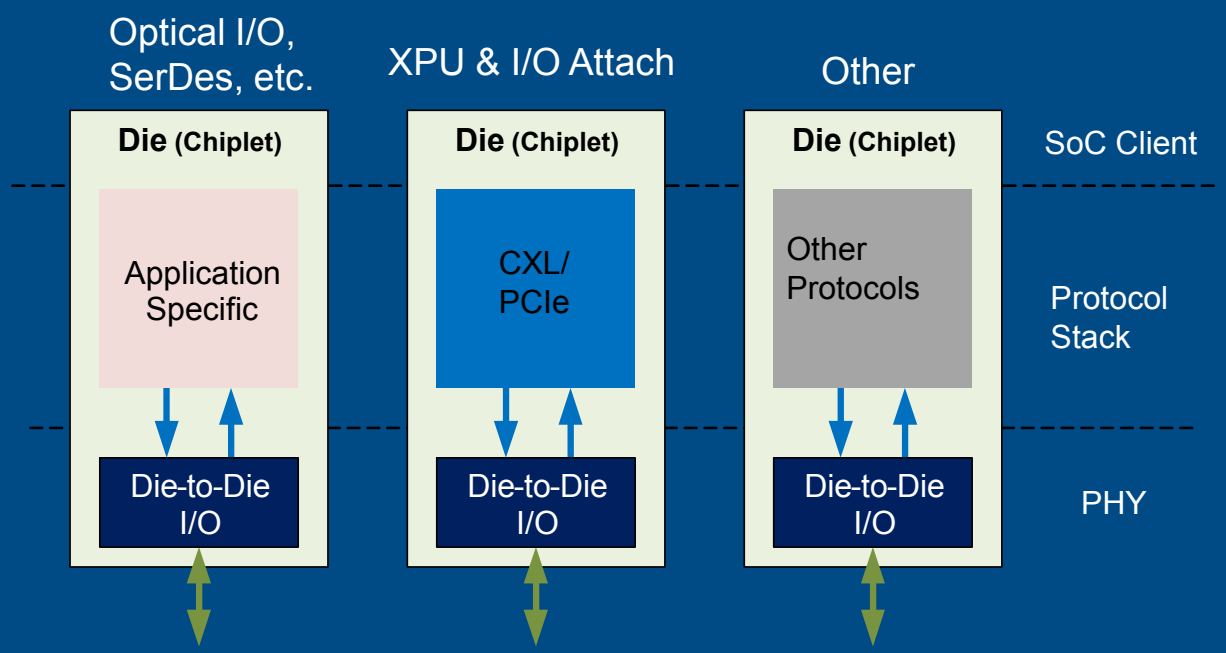
Chiplet Approach Known Trade-Offs

- Tiling overheads
  - Incremental area/power/performance overhead for die-to-die interface
  - Incremental package, assembly, and test costs/duration and tolerance requirements, impacting throughput/time, inventory management, etc.
- Impractical to co-package multiple “hot” die or die that each need a large amount of external PCB connectivity
- Margin stacking and inventory carrying costs when using external die
- Not optimal in cases where a single “sweet spot” configuration monolithic alternative is feasible and attractive
- Die built for a 3D stack difficult to reuse and may have additional thermal challenges

Adoption and Scaling Prerequisites

- Chiplet Based Product Volume Attach Points
- Fully Specified Interface Standards for Interoperability
- Chiplet-based Product Development and Integration Enabling IP, Software, and Tools/Flows/Methods
- Broad Market Manufacturing, Packaging, Assembly, and Test Capabilities

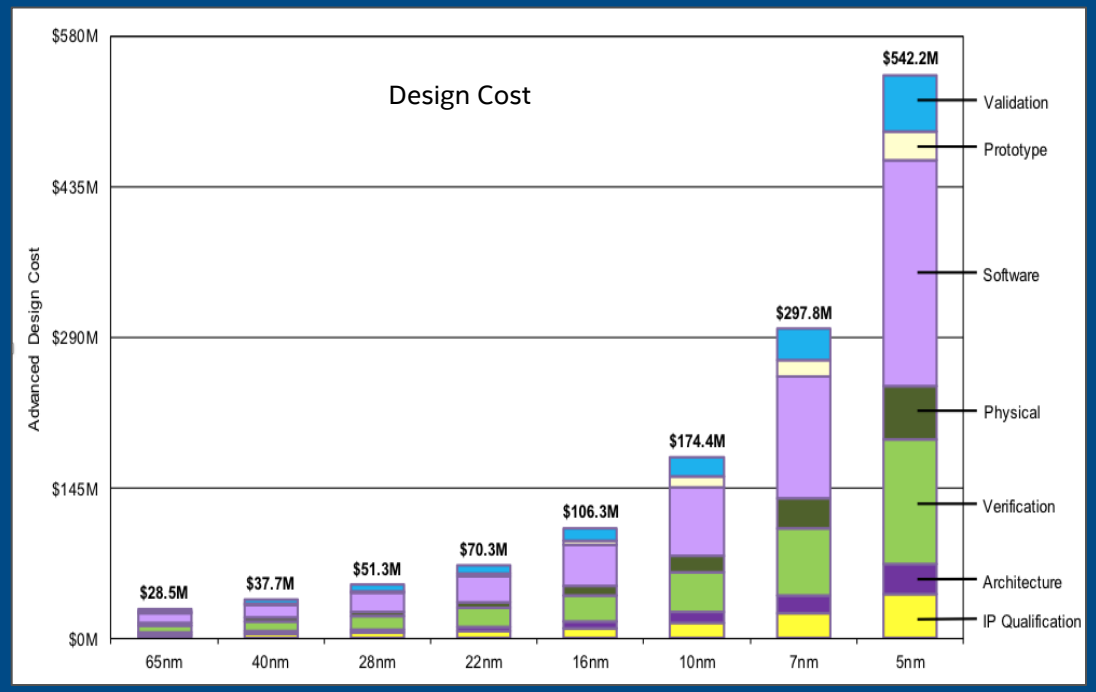
Die-to-Die Protocols and Use Cases



Volume Opportunity: XPU & I/O Attach

- Layer 1-Only Usage
  - Ideal for SerDes, Optical I/O, etc. PHY attach
- CXL/PCIe for XPU and I/O Attach
  - Addresses SoC construction and interfacing issues by leveraging proven CXL/PCIe model
  - CXL addresses common use cases
    - PCIe use cases are supported with CXL.io
    - Memory use cases are supported with CXL.mem
    - Accelerator use cases are supported with CXL.cache
- Other
  - Other protocols (e.g. AXI et. al.) and usages

Reuse is Key to Portfolio Cost Economics

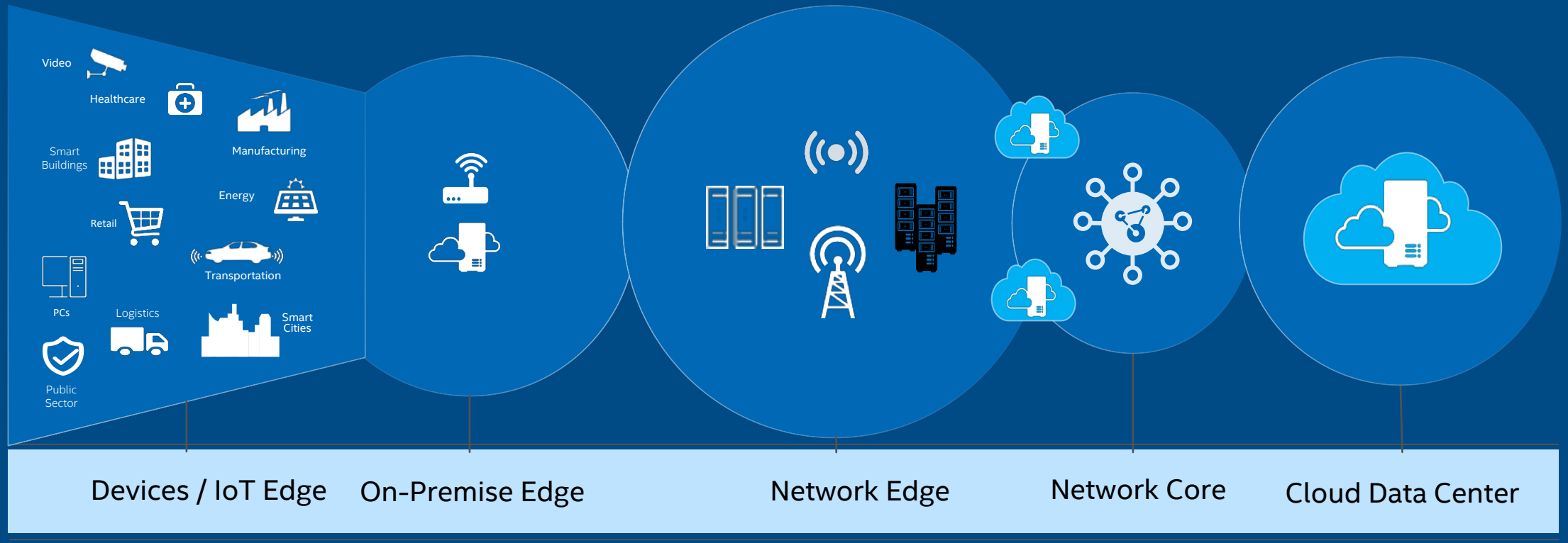


Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

Fewer chip design-in opportunities will individually be large enough to amortize rapidly rising leading edge chip costs

Must reuse IP/die within and between chips to manage cost mismatch

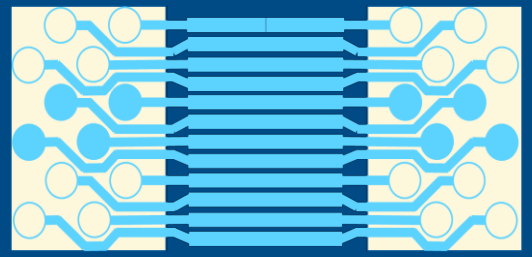
Reuse Key to Uniform Edge to Cloud Experience



- Compute, acceleration, and I/O capabilities rightsized for deployment environment
- Common software model largely agnostic to deployment details

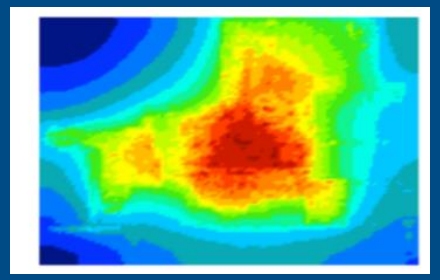
Need Architected, Fully Specified Interfaces

Mechanical



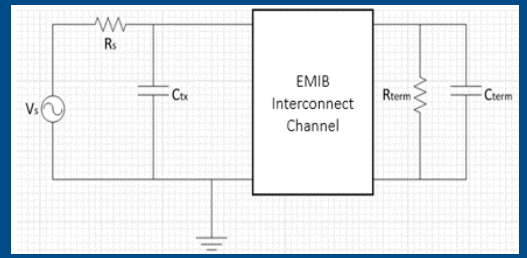
- Bump and wire sizes
- Bonding footprint
- xyz constraints

Thermal



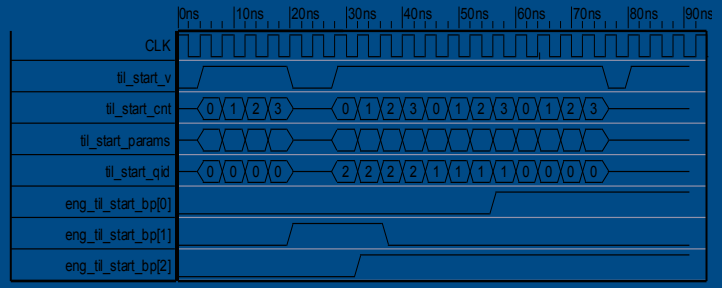
Thermal/temperature characteristics and constraints

Electrical



- Power delivery
- Noise margin
- Capacitance

Functional



- Data/transaction specifications
- Mgmt: power, security, debug, etc.
- Configuration & statistics
- Manufacturing test access

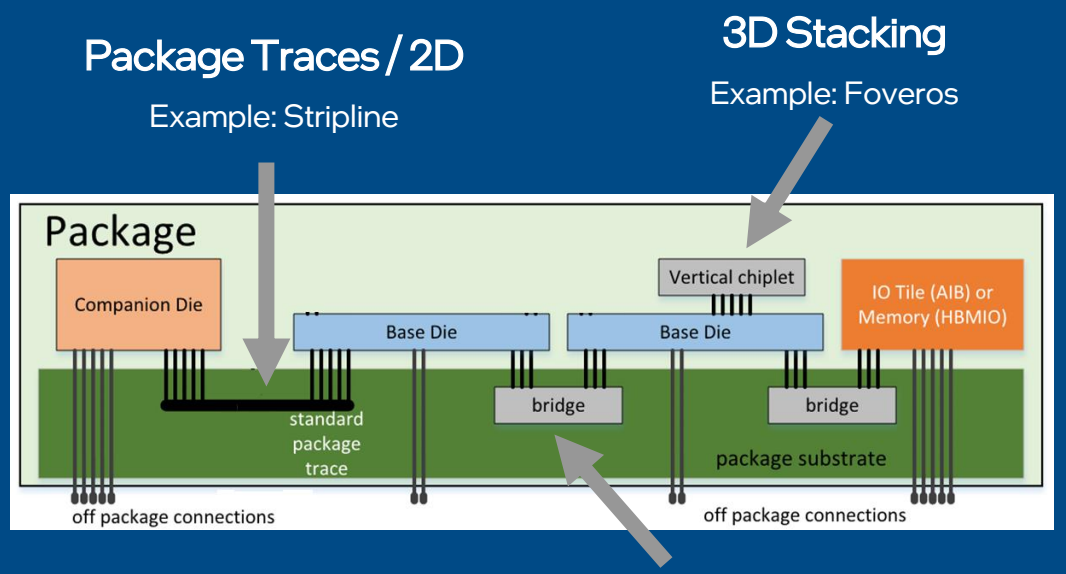
Which support
Generational Compatibility

All enabled by off-the-shelf
Tools/Flows/Methods and
HW/SW Building Blocks

… to support industry scale systematic reuse

Physical Connectivity Building Blocks

Packaging Technology

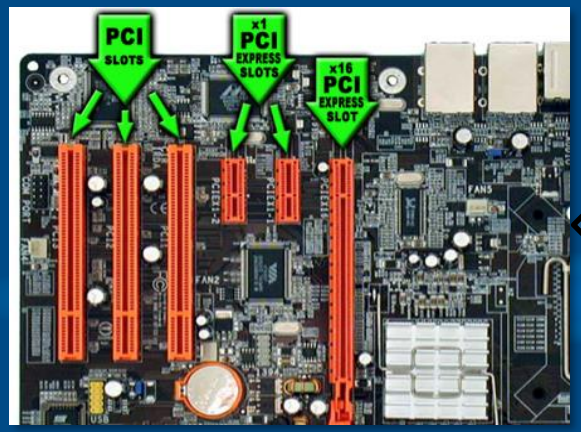


I/O Technology

	Simple I/O, Many Wires	Complex I/O, Few Wires
Advantages	Bump Pitch Scaling	Flexible Die Placement
	Low Power	Std package shoreline
	Low Latency	
Disadvantages	Die Placement Constraints	Higher Power
		Higher Latency
Examples	Intel AIB and MDI	Intel On Package I/O
	HBM Memory	USR/XSR SerDes

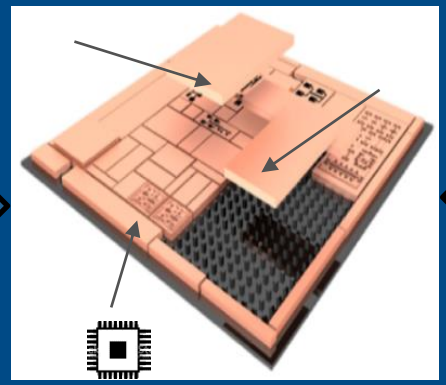
Many wire I/O approach best for unlocking full potential of package-level integration

Physical Integration-Independent IP + Software Model



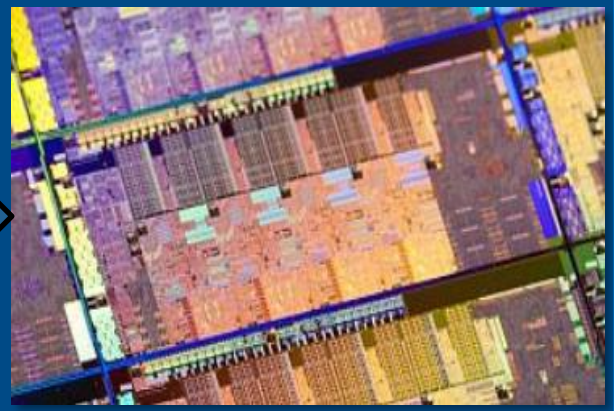
Board-Level Integration

Uniform SW



Package-level Integration

Uniform SW



On-die Integration

- Ideally IP and associated application software are agnostic to scaling and physical integration approach
  - Enables rightsizing functionality for a wide variety of target deployment environments with high reuse of IP, system, and software investments

Summary

- Chiplet approach has tremendous potential to reshape how companies can collaborate to build many classes of chips in the future
- However, there are key adoption and scaling prerequisites that must first be met
- Layer 1 I/O attach and XPU + I/O attach are important early use cases to address
- Using CXL/PCIe to support XPU + I/O attach usages enables more rapid adoption, providing ecosystem carryover with a uniform software model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