Road to Chiplets: Architecture

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Test Challenges & Directions as the industry moves to 3D Heterogeneous Products

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Purpose

- **What are the main test-related challenges the industry is currently facing "On the road to chiplets?"**

  … and Heterogeneous packaged products in general

- **What are existing/proposed solutions to these challenges?**

My perspective in this presentation is mainly: advanced technology, high performance multichip products. (AI/ML, Data Center, Network, Computing)

"Heterogeneous Integration Test Roadmap" *(94 pages of good reference material)*

http://eps.ieee.org/hir

Broadcom Example

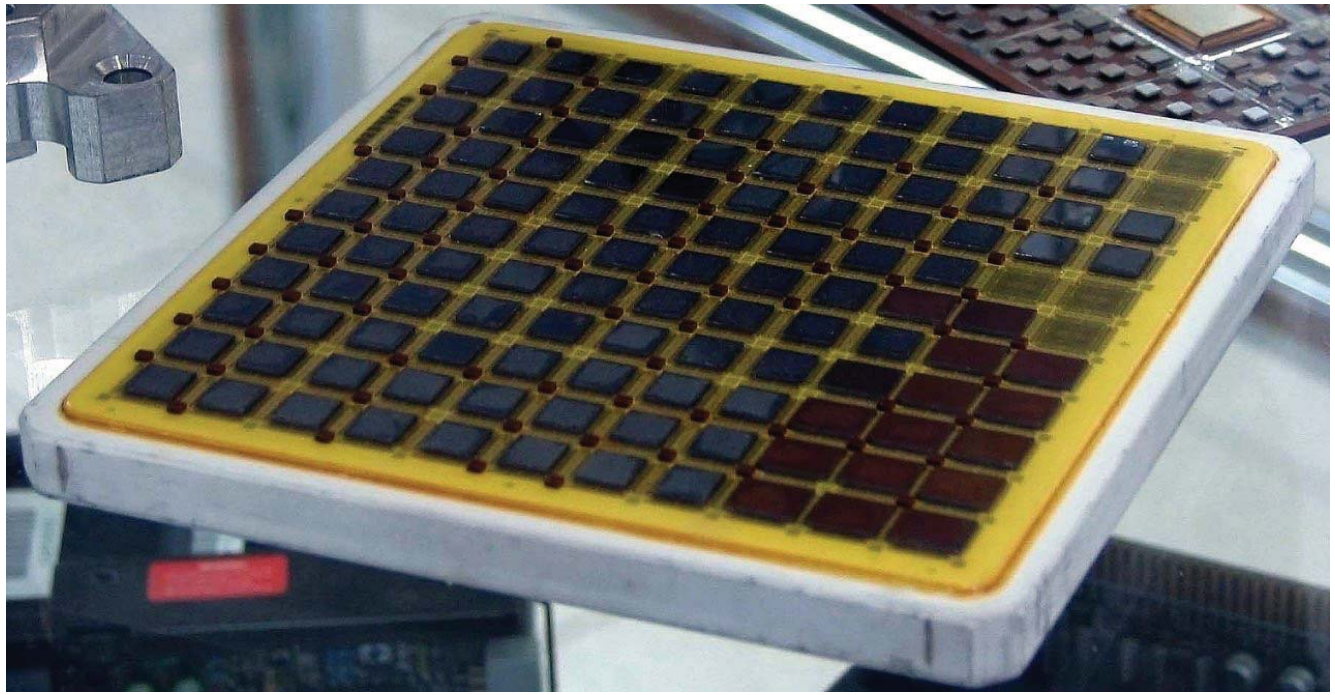
- **Announced November 2020**
- **5nm ASIC**
- *625 mm2, this device incorporates PCIe Gen5 protocol, 112-Gbps SerDes, HBM2e memory operating at 3.6 Gbps, and 3.6-Tbps Die2Die PHY IP utilizing TSMC CoWoS® interposer technology.*

Outline

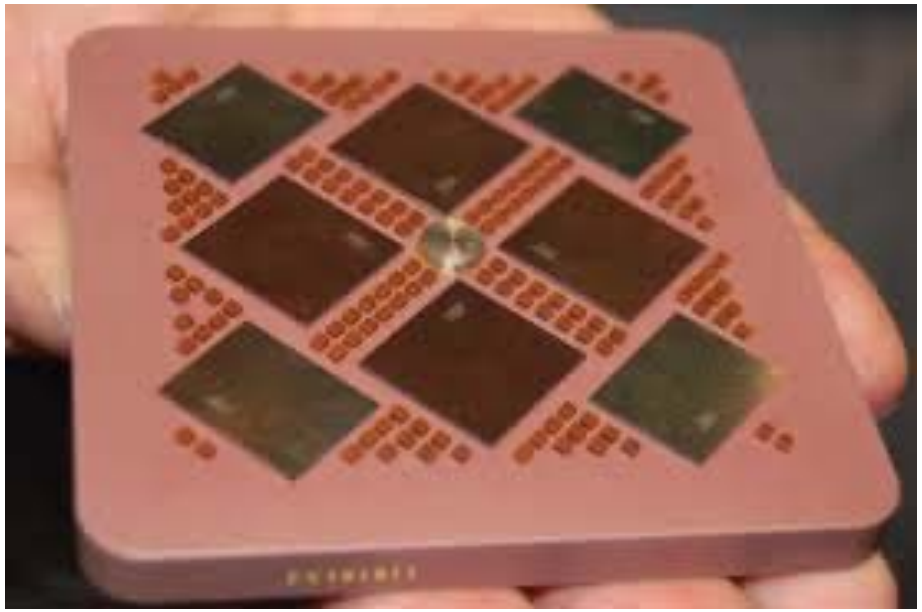
- What is the general challenge related to 2.5D / 3D ?
- Where are we with multichip products today ?
- 2.5D / HBM – mature technology ?
- Bare die supply – what are quality/yield requirements ?
- Test Challenges
- Industry Standards – will they solve the problems ?
- Best practices for chiplet test support moving ahead.
- End-to-End Data Analytics – why is this important ?

My first job (1983)

When one of these dies (90 to 121 per MCM) passed chip-level production test – and only failed at MCM or system test – how to improve production test to detect?



IBM ES/9000



Power5 MCM

Path to Productivity – where are we today ?

[Dave Armstrong, Advantest]

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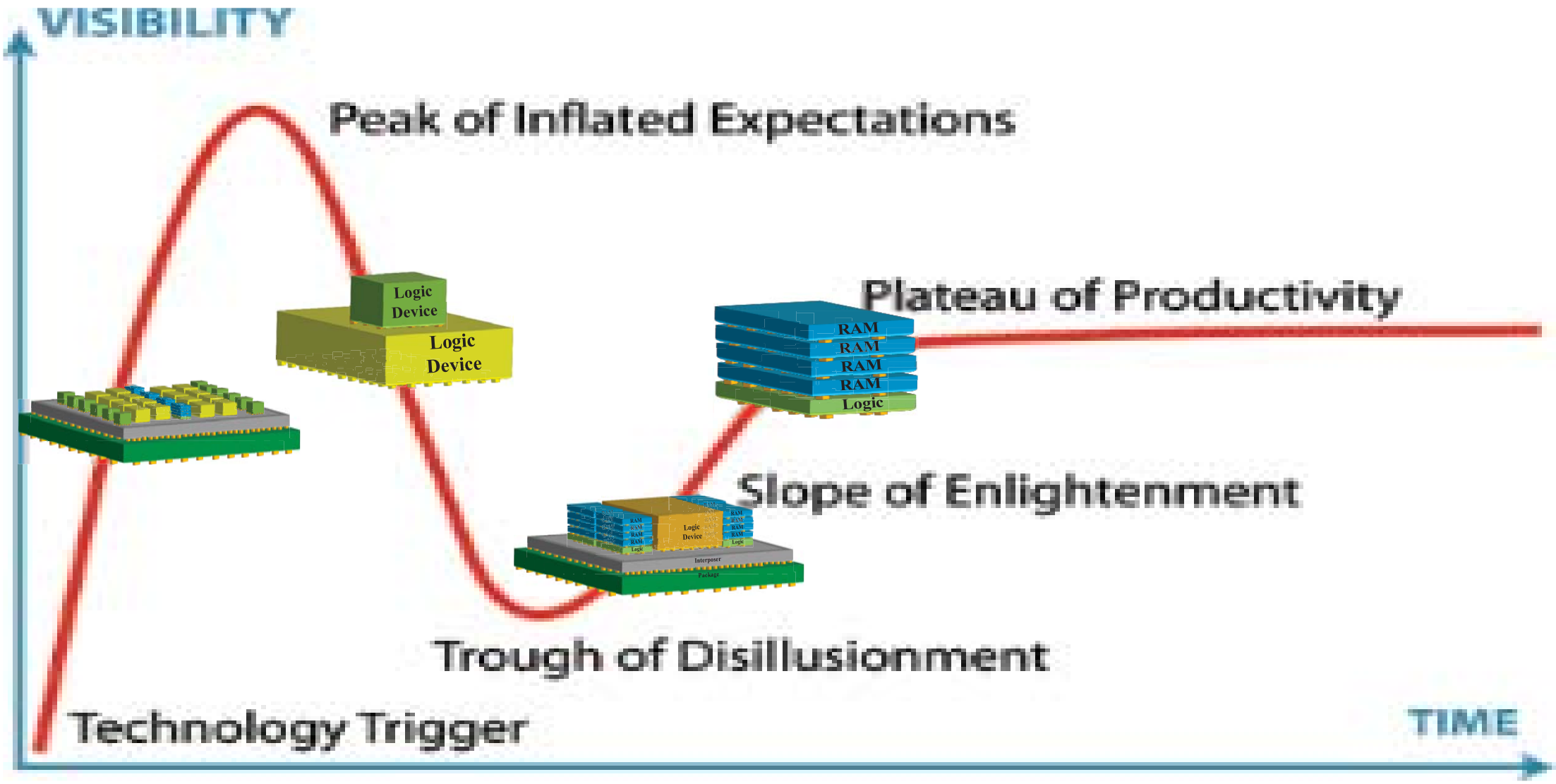

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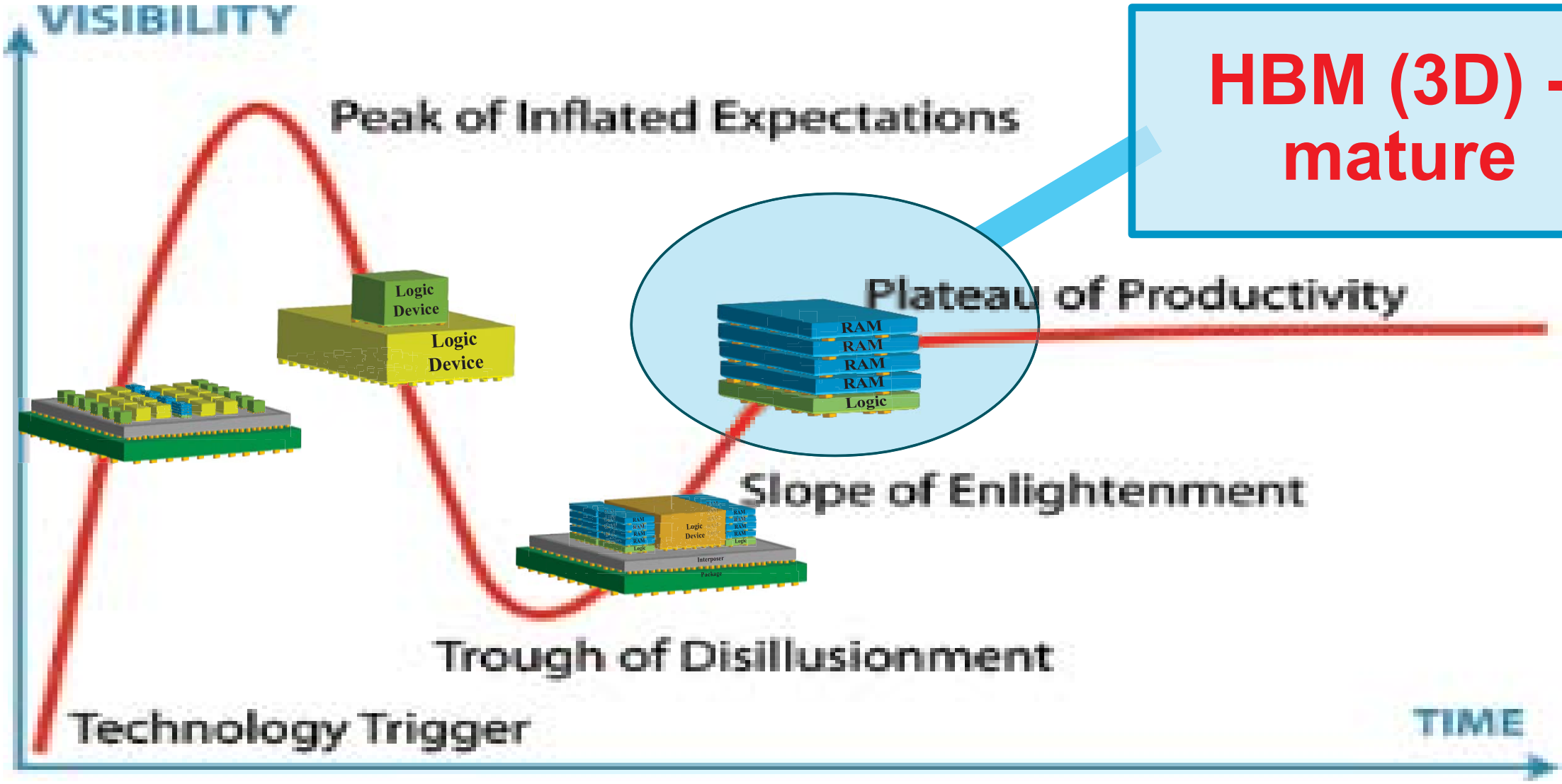
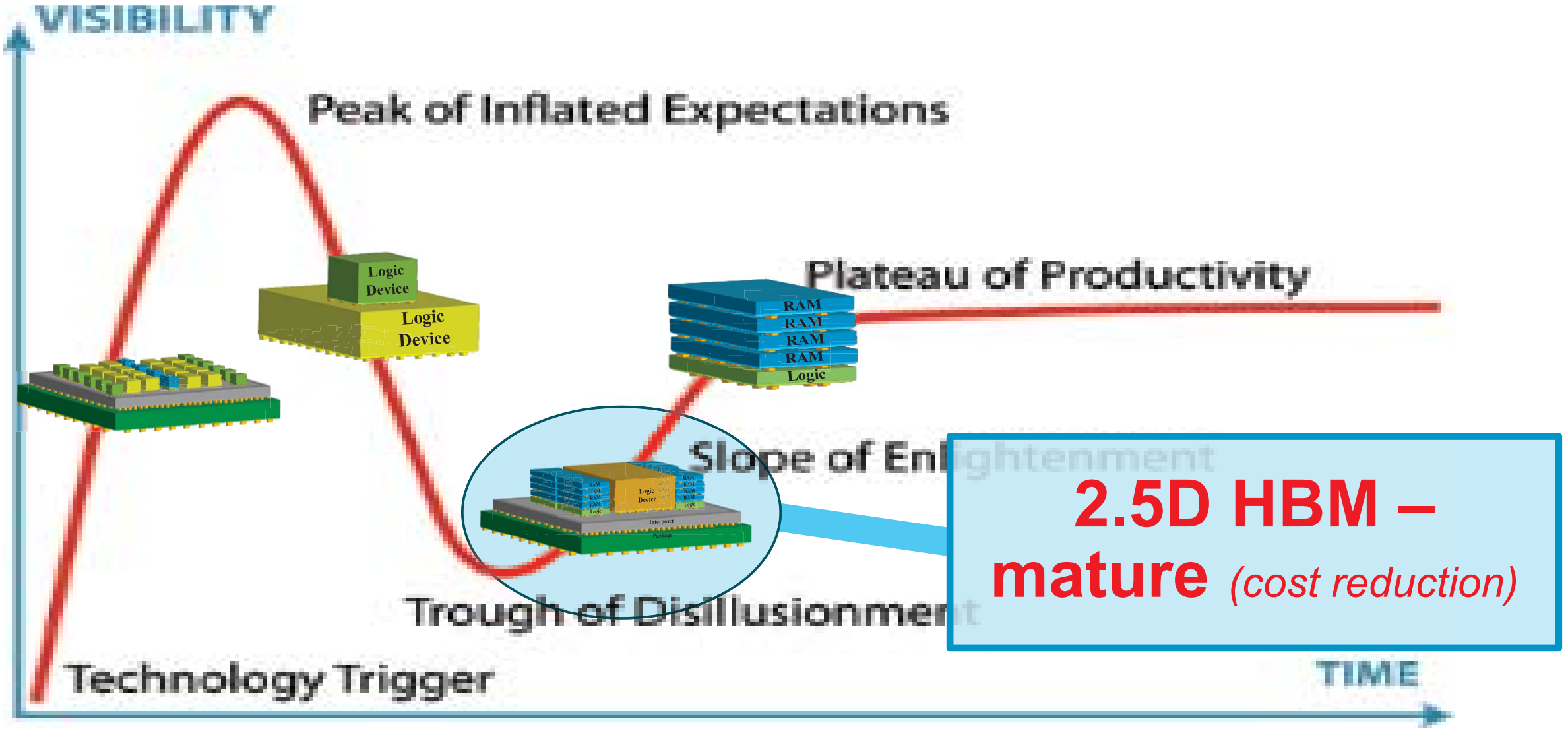


HBM (3D) -- mature

[Dave Armstrong, Advantest]

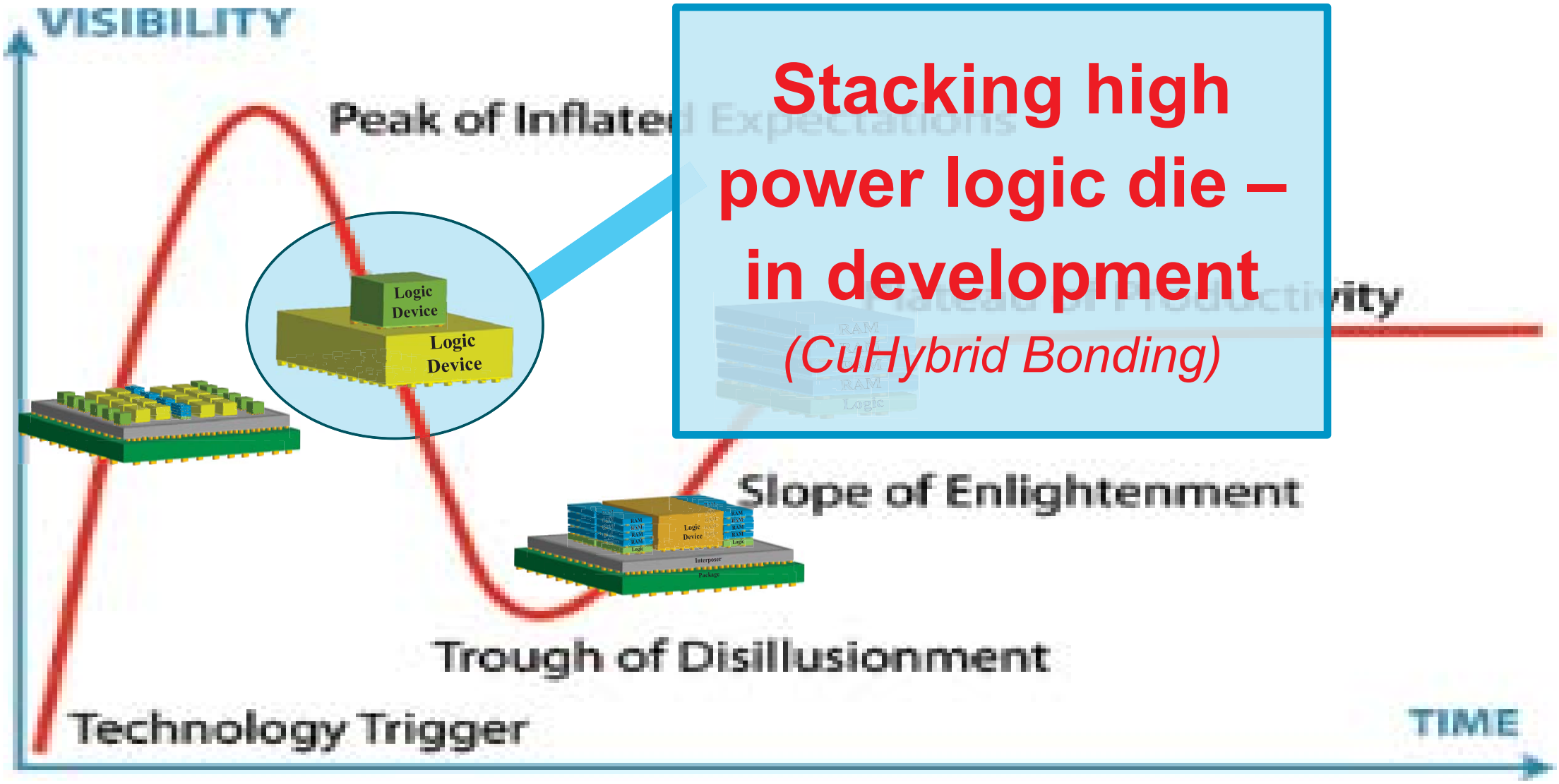
Path to Productivity – where are we today ?



2.5D HBM – mature *(cost reduction)*

[Dave Armstrong, Advantest]

Path to Productivity – where are we today ?

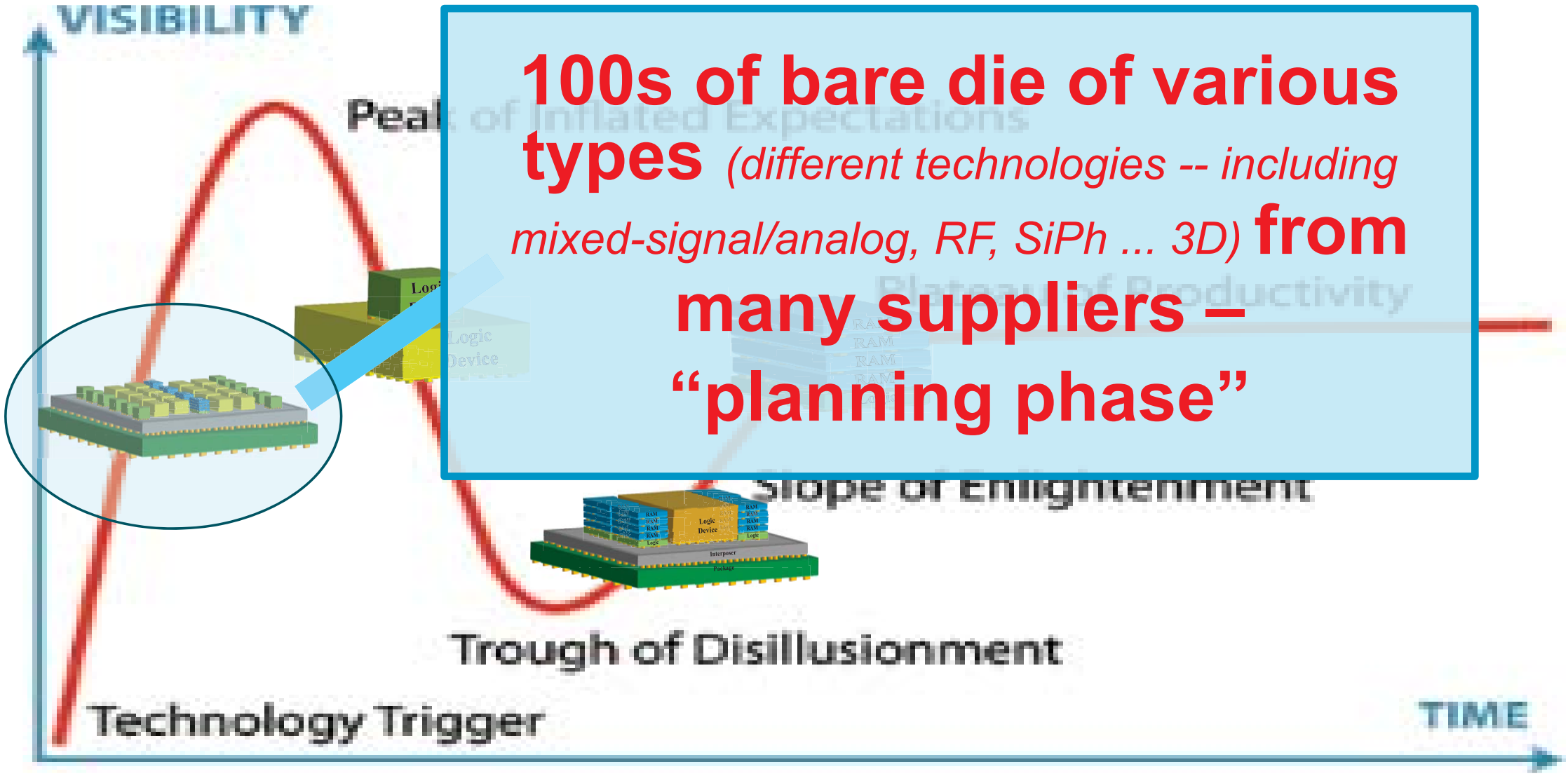


Stacking high power logic die – in development

(CuHybrid Bonding)

[Dave Armstrong, Advantest]

Path to Productivity – where are we today ?

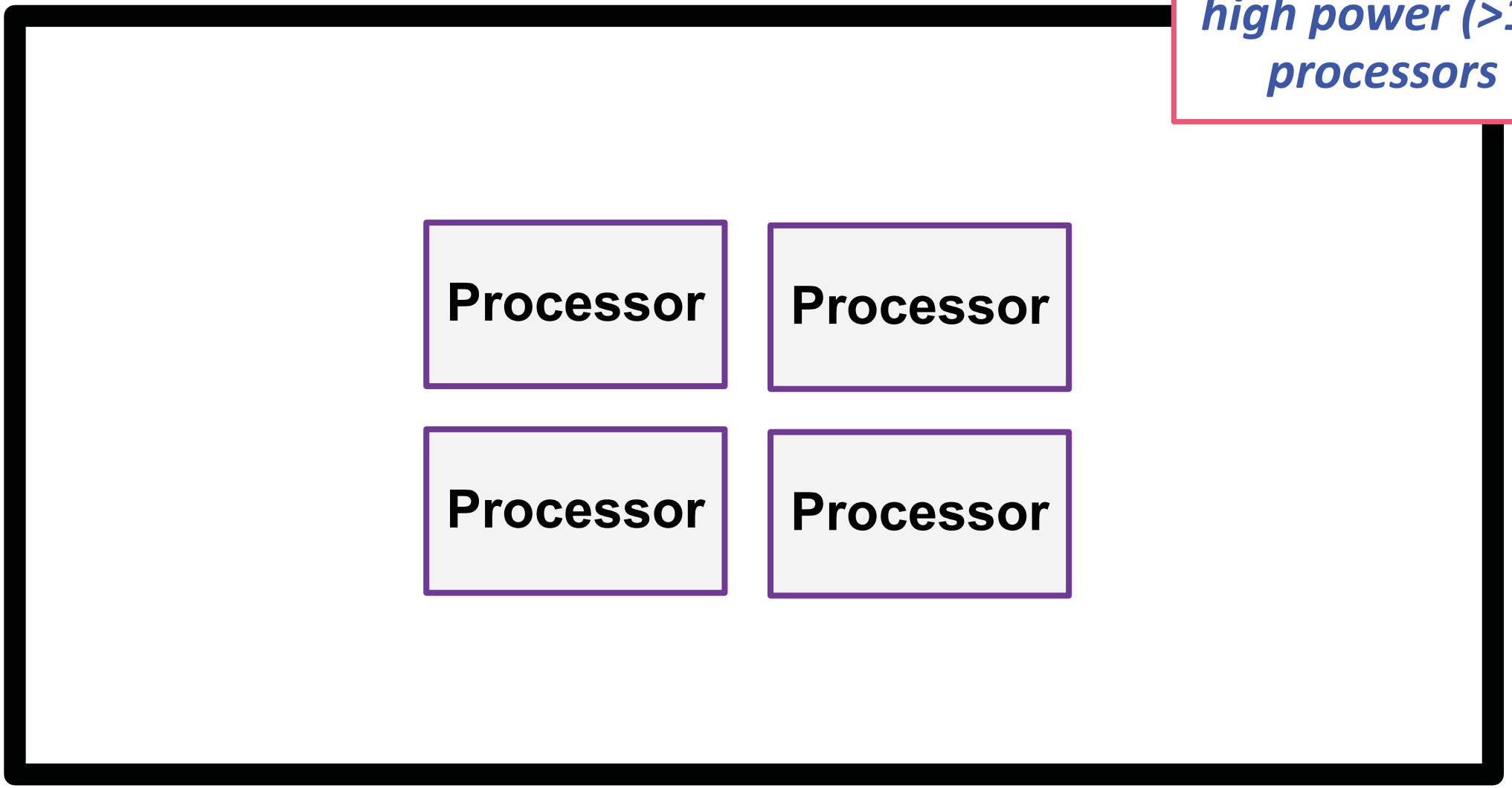


100s of bare die of various types *(different technologies -- including mixed-signal/analog, RF, SiPh ... 3D)* **from many suppliers – "planning phase"**

[Dave Armstrong, Advantest]

The Challenge – Test Support

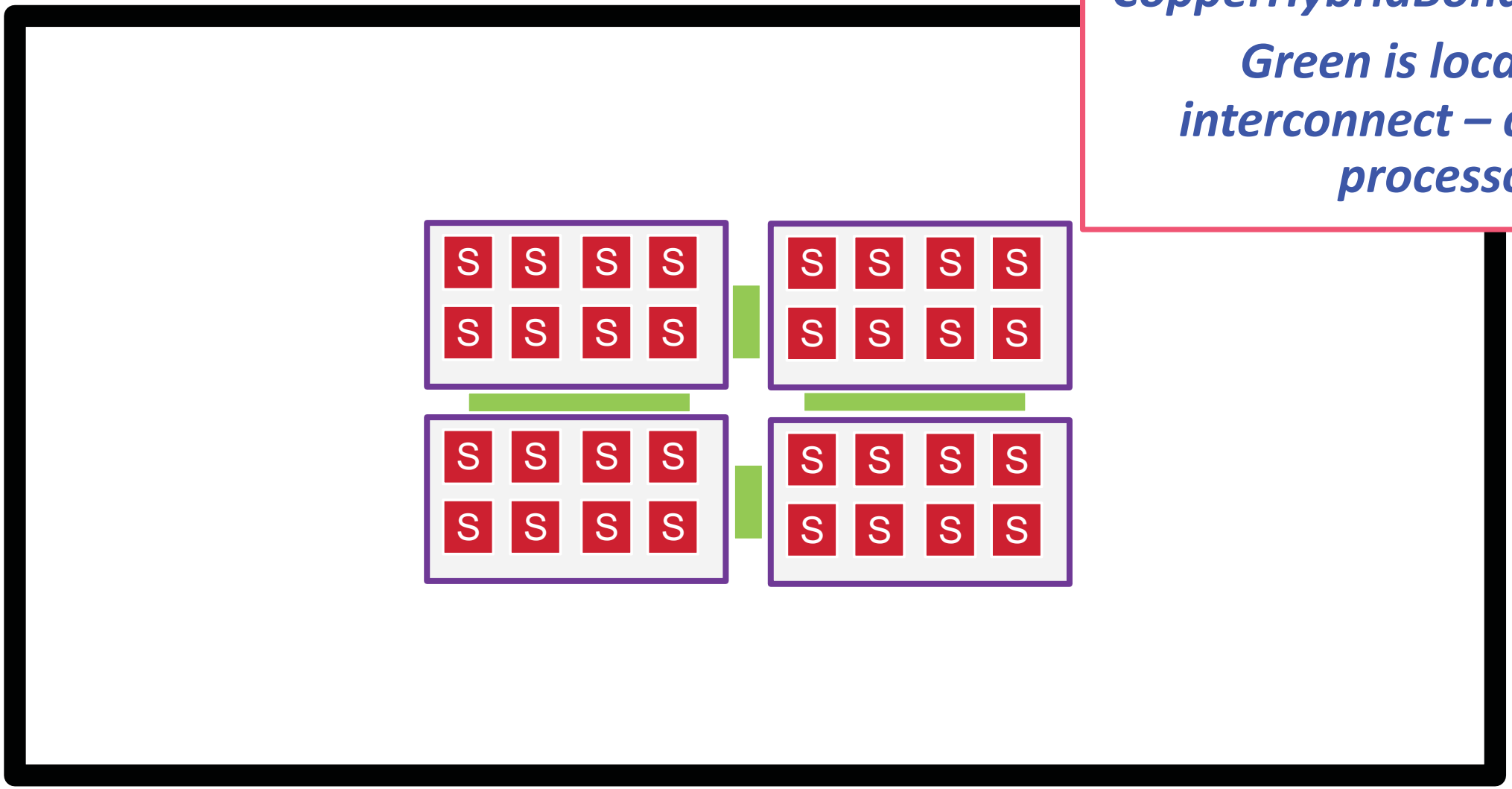
Four high-performance, high power (>100W / die) processors (AI/ML).



The Challenge – Test Support

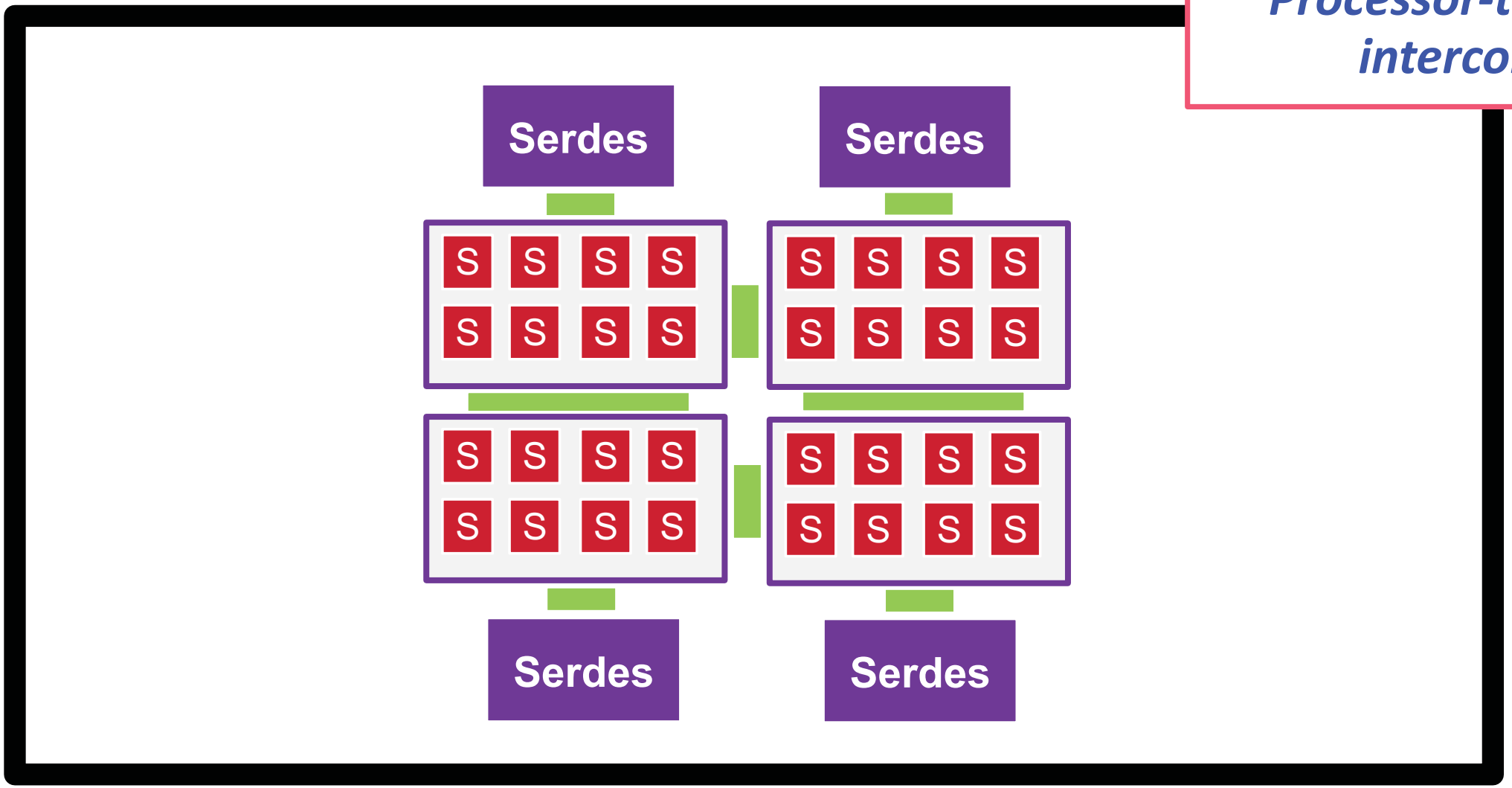
Add 8 SRAM chiplets to each processor using CopperHybridBonding. *(32 total)*

Green is local silicon interconnect – connecting processors.



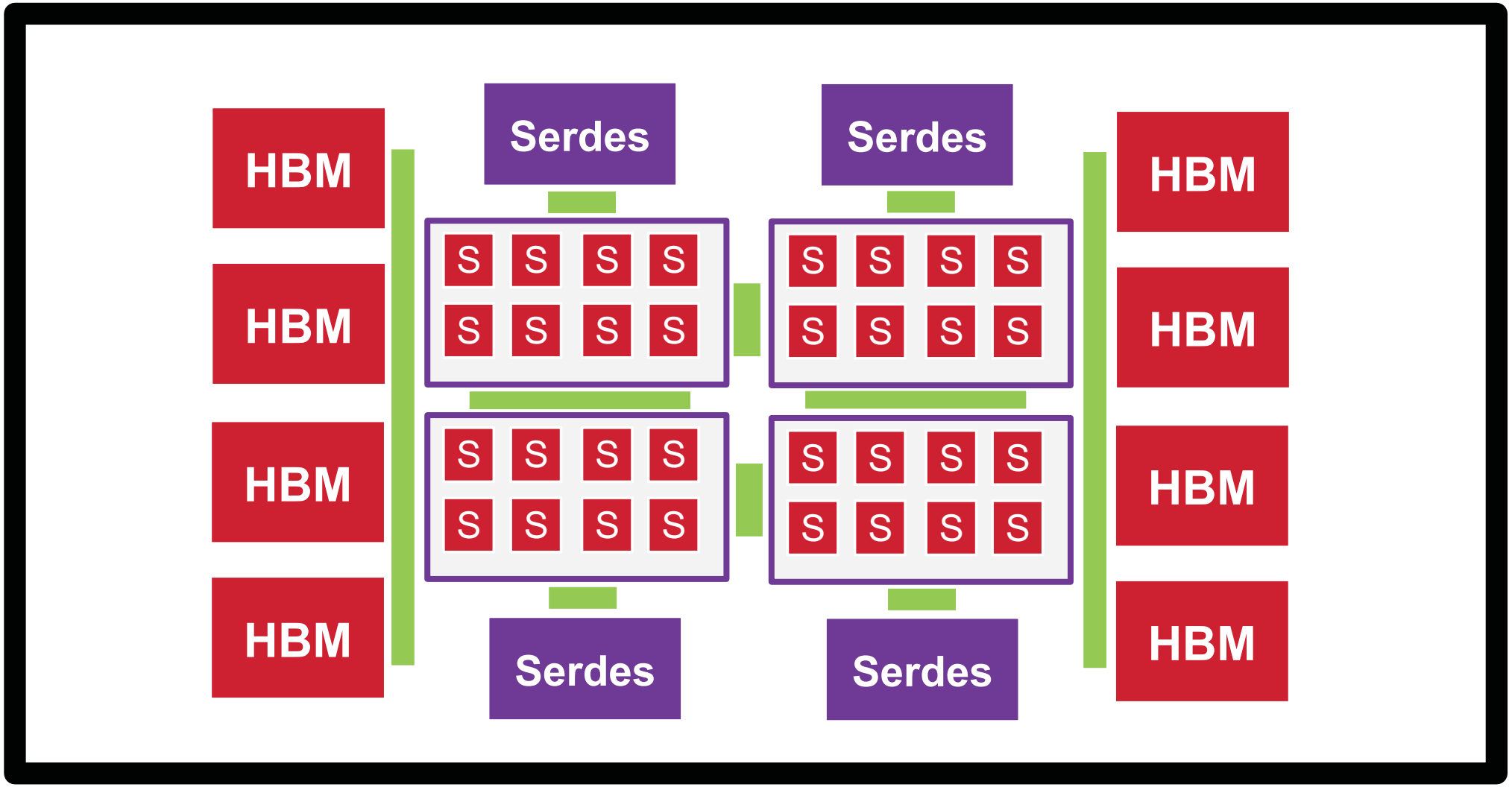
The Challenge – Test Support

Serdes chiplet for Processor-to-external interconnect.



The Challenge – Test Support

8 HBMs … 8 high stacks



122 bare die

Where will we be in 10 years ?

What will the chiplet market look like ?

- ***Will there be a wide variety of chiplet providers where the package integrator can "plug & play" chiplets ?***

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or

- ***Will system integrators only work with a small number of trusted chiplet partners that have been proven ?***

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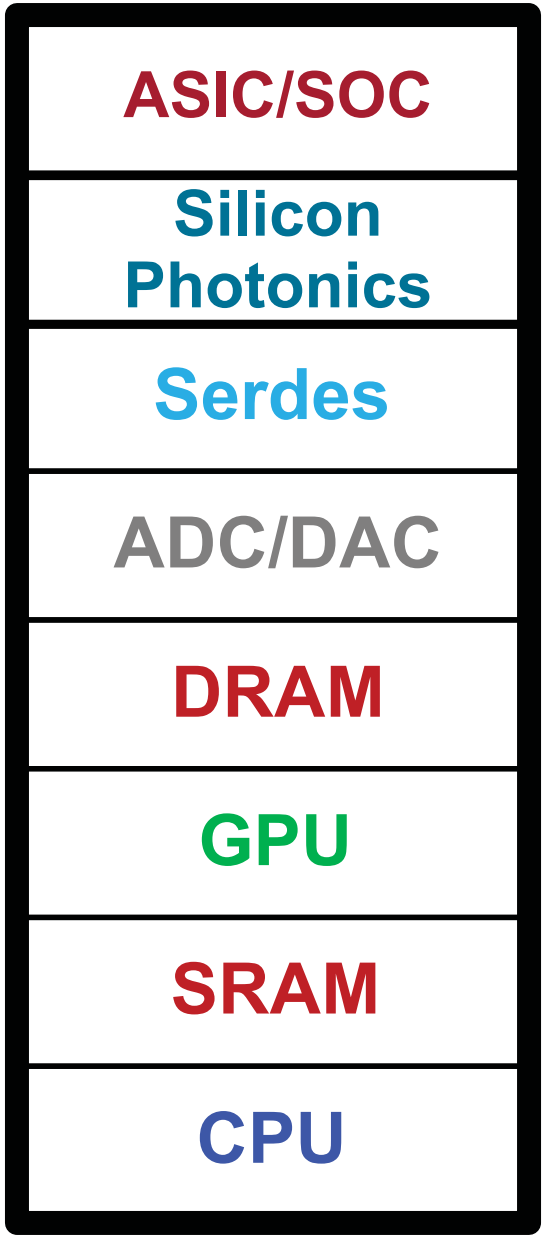
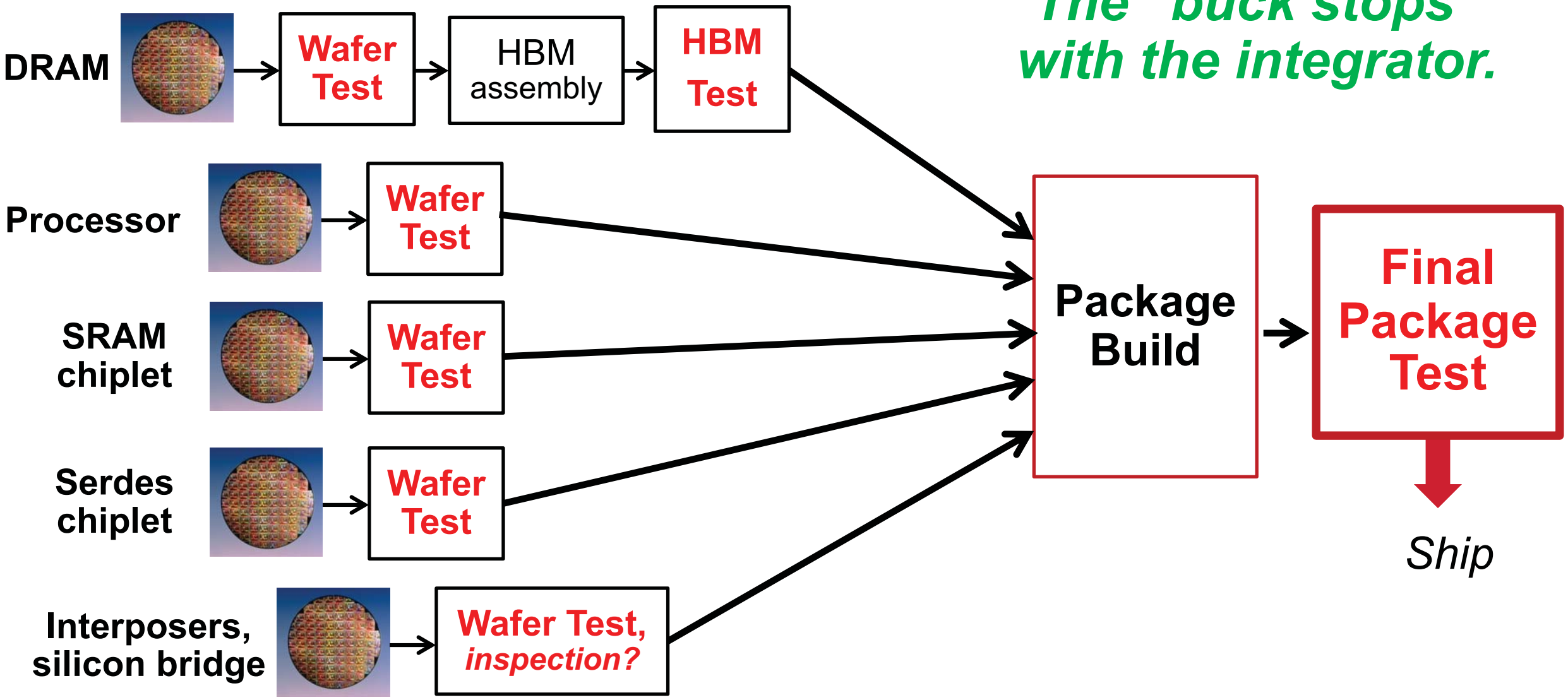


thermal

Example Test Flow

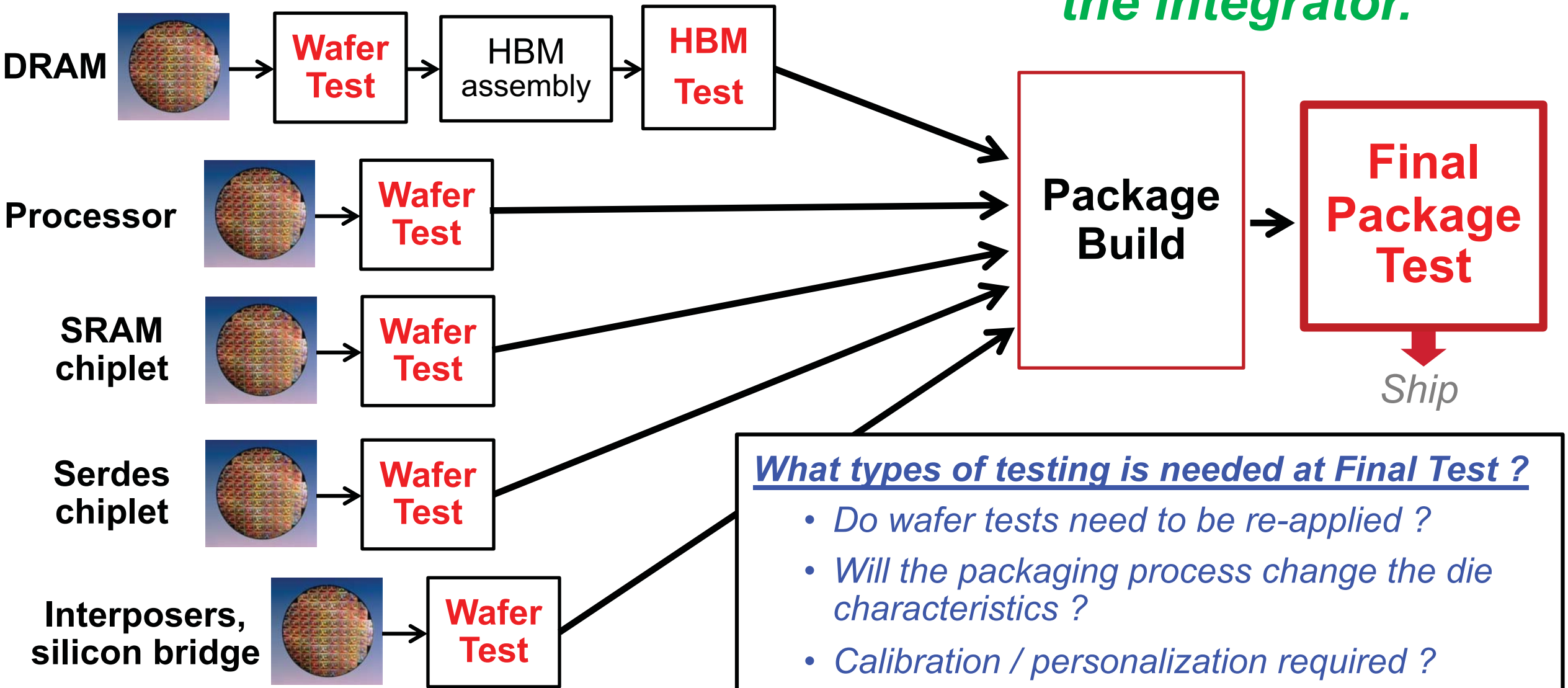
The "buck stops" with the integrator.



Some products use multiple test steps at wafer or final test.

Example Test Flow

The "buck stops" with the integrator.

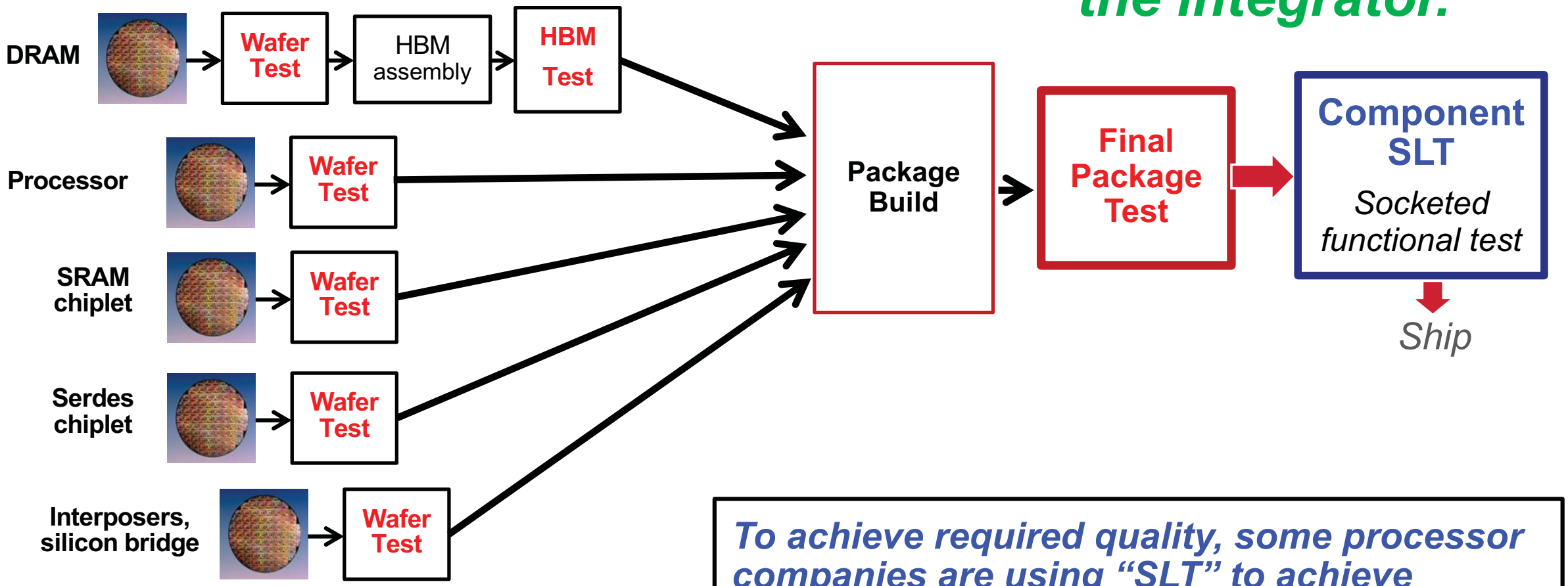


What types of testing is needed at Final Test ?

- *Do wafer tests need to be re-applied ?*
- *Will the packaging process change the die characteristics ?*
- *Calibration / personalization required ?*
- *Lane or bit Repair ?*

Example Test Flow

The "buck stops" with the integrator.

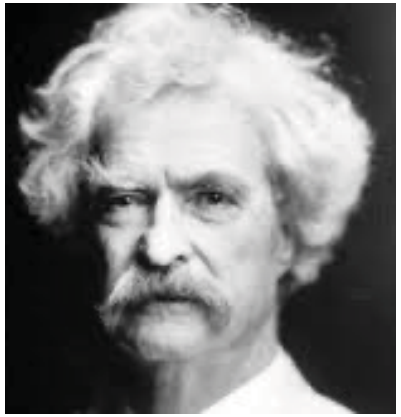


To achieve required quality, some processor companies are using "SLT" to achieve required quality levels.

Testing challenges

- **The main concern really isn't "testing" – it is yield.** *(and quality)*
- **We know how to thoroughly test the final packaged part.**
  - ***BUT … if bare die are not tested thoroughly beforehand (at wafer probe) – then Final Package yield could be poor.***
    - ***30 bare die … each with 99% quality … final package fallout: 26%***
    - ***100 bare die … each with 99.5% quality … final package fallout: 40%***
- **The general requirement is to drive as much testing back to wafer probe as possible.**
- **How much of wafer probe testing needs to be repeated again at package test ?**

Bare Die Quality



- **The industry uses the term "Known Good Die" (KGD) – but there isn't a standard definition on what this means.**
  - ***KGD does NOT mean that all shipped bare die will pass*** *package & system test … and in the field.*
- **Bare die suppliers need to provide:**
  - *% of die that will fail at the next level of assembly test -- maximum*
    - *10dpm … 100dpm*
  - *% of die that will fail long-term (reliability failures) -- maximum*
- **Suppliers need to also provide test data/information for post-bare-die testing.** *(more later)*

Chiplet / Heterogeneous Packaging Test Challenges

- **How do we achieve “low DPM” quality for the end customer ?**
- **How do we drive all testing back to ATE wafer probe test ?**
- **<u>A major challenge is wafer test probing.</u>**
  - *For advanced packages – it is difficult (really expensive) to do full probing today. Tomorrow – it will be impractical.*
  - *So reduced pincount probing at wafer test is required.*
- **When CopperHybridBonding is used – and the number of signal IOs go from <1000 to something like 10,000-30,000 signal IOs.**
  - *Board-level DFT methods like 1149.1 JTAG will have too much area overhead.*
  - *The package part is more like a big SOC – rather than a board.*
    - *If packaging people can build it – they will.*
- **Thus, plan for very limited signal IO pincount testing for wafer probe test.**

Challenges – Final Package Test (Important)

- **Will bare die need additional testing at Final Test ?**
  - *Test / repair faults -- RAM repair, lane repair.* *"Harvesting" – no die left behind.*
  - *Final Calibration (required post packaging)*
  - *To detect defects that occurred during packaging process.*
- **Today – it isn't always possible to re-apply all tests applied at wafer probe by suppliers.**
- ***There are concerns about retesting board/system fails by bare die suppliers.***
- ***What if a new wafer probe test screen is added by one/more of the suppliers ?***
  (for parts beyond wafer test)

I think the "package integrators" should create a Design-for-Test / Test Plan capability to have the option to apply as many wafer probe tests from suppliers as possible.

Challenges – Final Package Test (Important)

- **Will bare d**
  - *Test*
  - *Final*
  - *To de*
- **Today – th** **sts applied at wafer pr**
- **Concerns** **uppliers.**
- **What if a n** **re of the suppliers ?** *(for parts beyond wafer test)*

Will bare die suppliers provide all information needed to enable the final package integrator to apply all tests ?

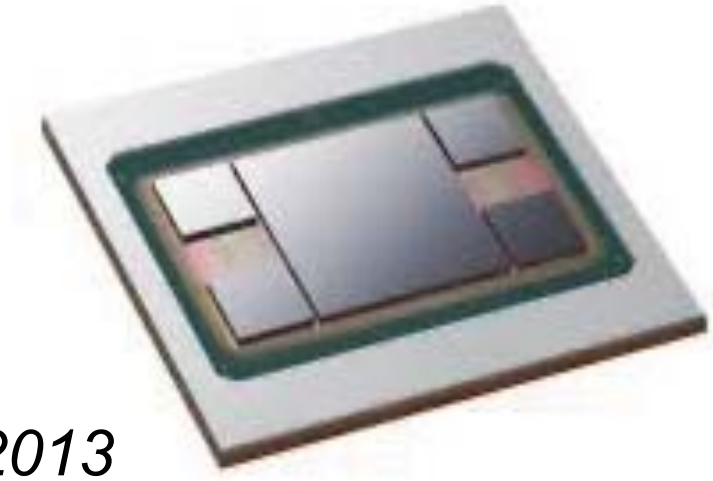
Or will test details be viewed as proprietary – and many details not shared ?

I think the "package integrators" should create a Design-for-Test / Test Plan capability to have the option to apply as many wafer probe tests from suppliers as possible.

Will Industry Standards solve these problems ?

- **HBM – widely used industry standard** *(JESD235x)*
  - *Described tests may not be sufficient for all products.*
- **3D Digital ICs – IEEE 1838** – *getting momentum*
- **2D / 2.5D chip-to-chip interconnect**
  - *Industry is discussing proposals – e.g., Open Domain-Specific Architecture. Bapi Vinnakota is doing a talk tomorrow on OSDA.*
- **Mixed-signal (e.g., high-speed ADC/DAC), RF, Silicon Photonics … no industry standard DFT/Test**

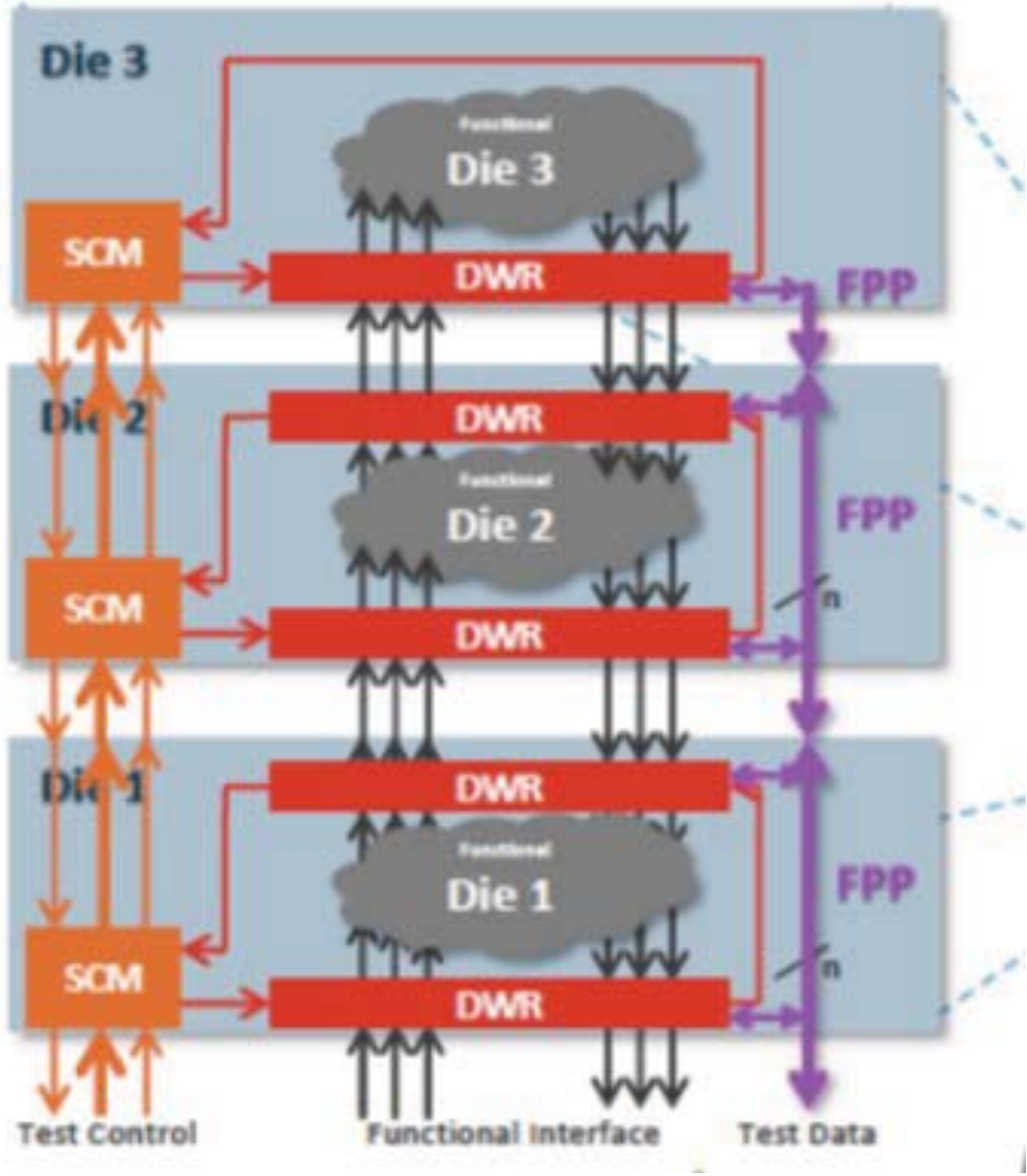
2.5D HBM *(including CPU/GPU/Processor)*



- **Most Test challenges were addressed by industry standard Design-for-Test and Test capabilities. JESD235**x *… initially 124 pages, Y2013*
  - *Describes functional & test operation modes*
  - *Test Modes: including loopback/MISR, Memory BIST, Intest/Extest.* ***(may need additional tests)***
  - *Lane repair, DRAM cell repair (soft/hard repair)*
  - *Die ID, thermal monitors*
  - *Voltage references*

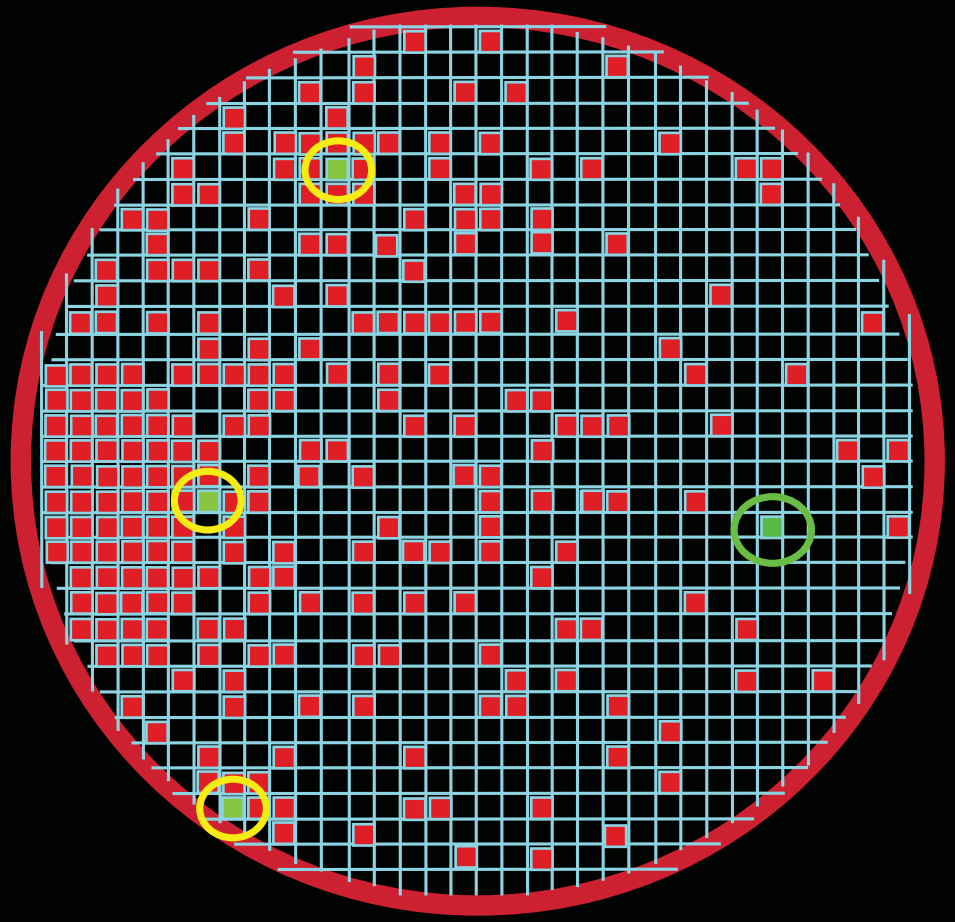
IEEE 1838 – 3D DFT Standard

- **Standard Y2019**
- **Targets stacked die – digital**
- **Enables chip-level access up/down stack**
- **Flexible wrappers around each die**
- **Starting to get industry traction.**
  - *Support from EDA companies*



End-to-End Data Analytics *(long-term view)*

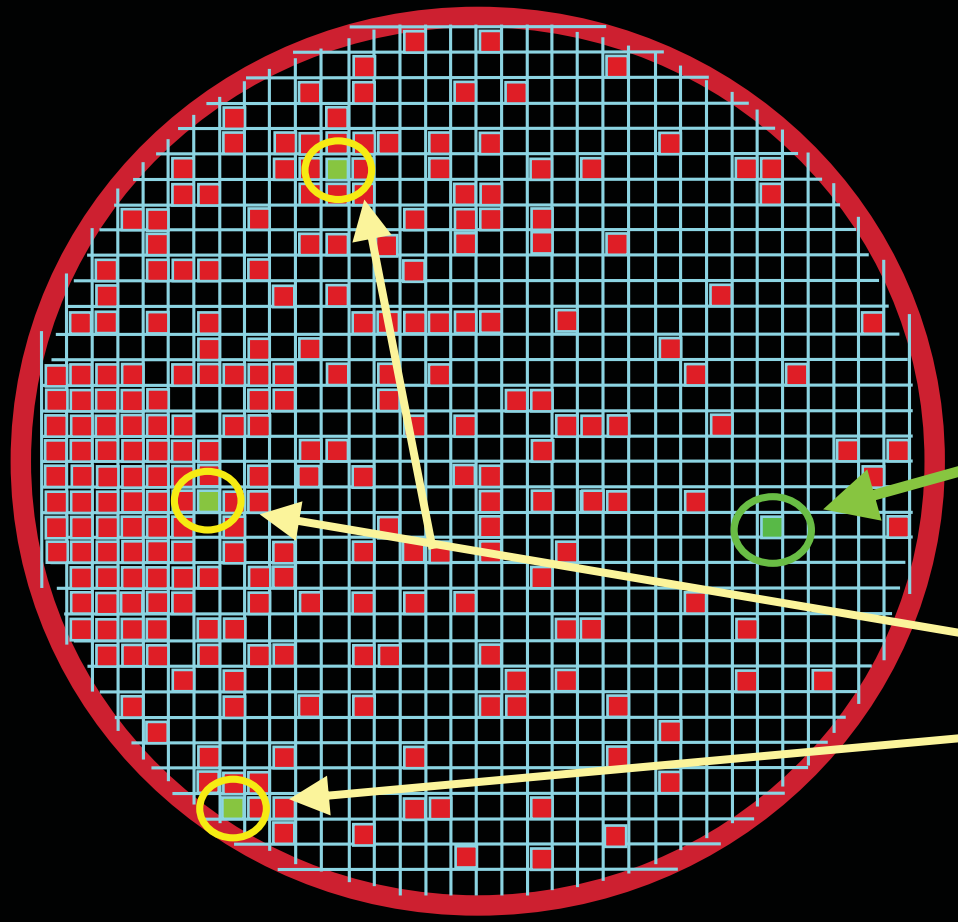
“Statistically more Reliable Dies”



Defects cluster

Red chips are fails ...
*Black & **green** chips are passes.*

“Statistically more Reliable Dies”



Defects cluster

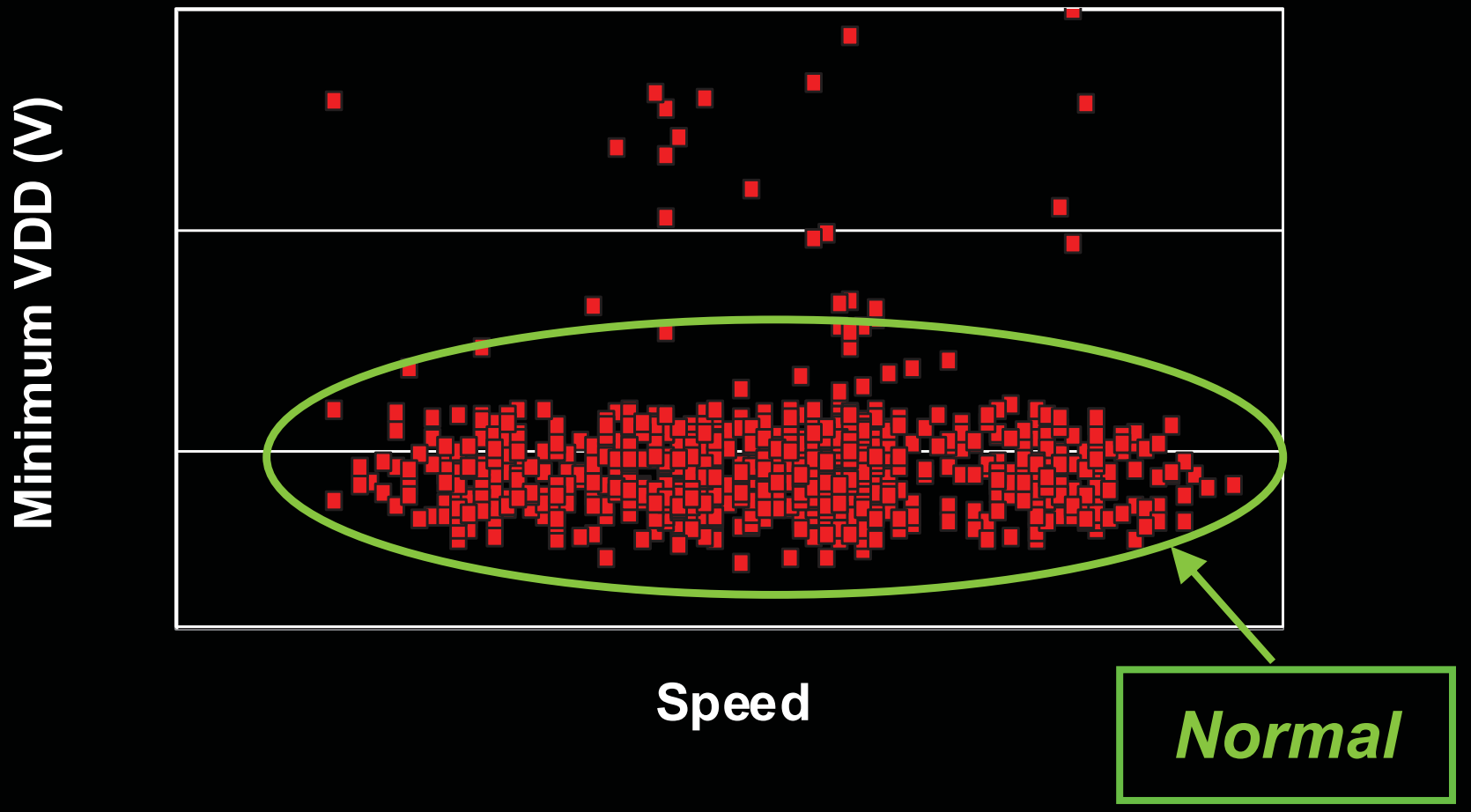
This device

… is more reliable than these three devices. (> 20X)

Red chips are fails …
*Black & **green** chips are passes.*

Statistical Outliers

All devices passed to specification testing



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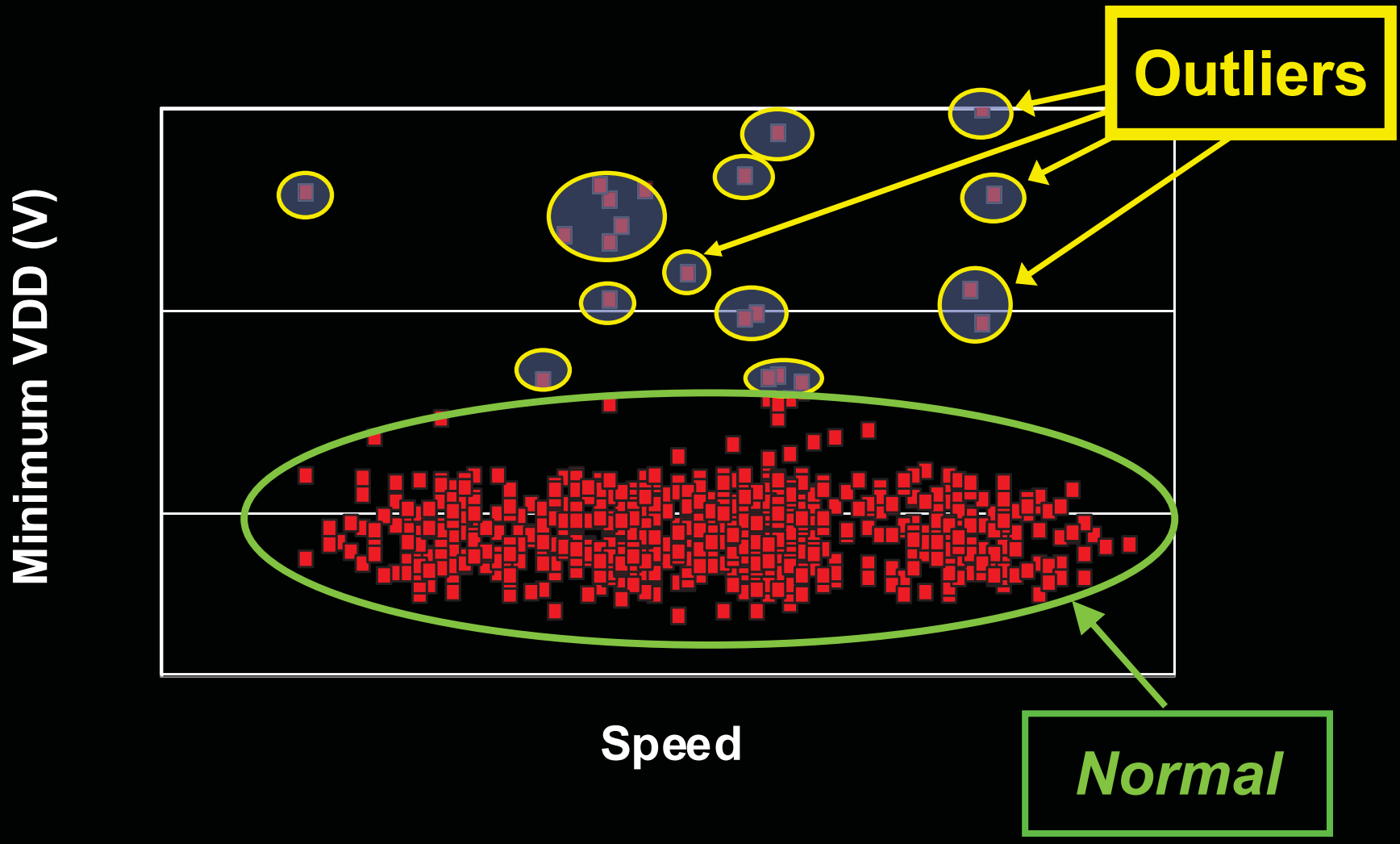


Why is E2E Data Analytics Useful ?

- **Example: Final Test yields drop significantly for a period of time.**
  Let's say it fails a product-wide functional test with poor diagnosis.

- **What is the root cause ?** *(among other things)*
  - *Packaging process?*
  - *Final Test issues?*
  - *A low yield issues for one type of die ?*
    - *If so – the problem could be either a defect issue – or process variability*

- **If low Final Test yield is due to a die yield or process problem – wafer test yield/test data will show the issue.**

- ***But … how do we enable rapid data review for the history of >100 die from 10 different suppliers … and 30 different die types?***

Data Analytic Enablers

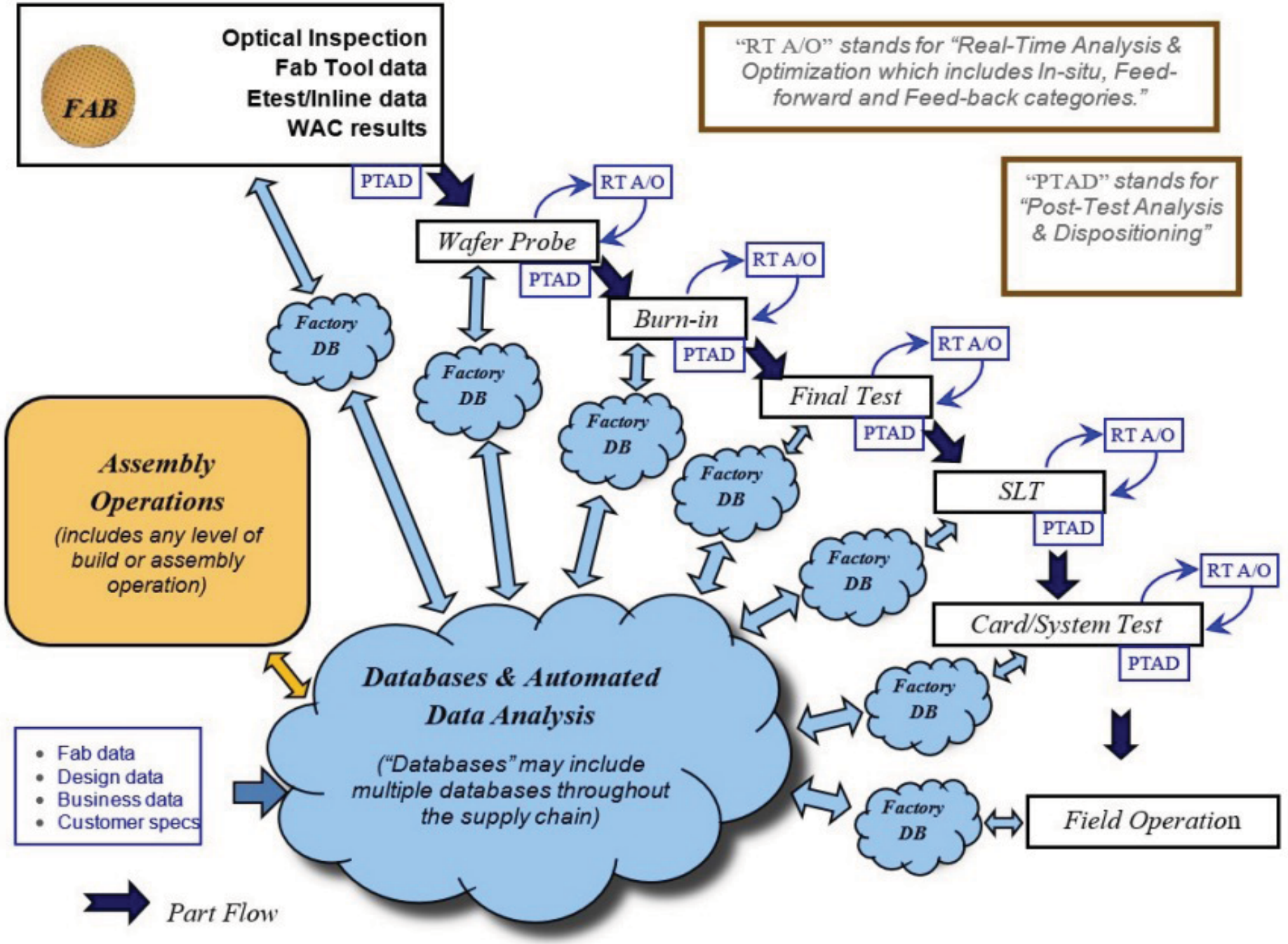
- **End-to-end die traceability.**
- **Commitment to collect Die ID and select data – and share required data in a common end-to-end database.**
- ***Much more detail is in:***
  - ***"Heterogeneous Integration Test Roadmap"*** *– start at page 52*
    http://eps.ieee.org/hir

End-to-End Analytics

Goal is to integrate End-to-End data.

From HIR:

http://eps.ieee.org/hir



Summary

- There are clear test challenges to fully exploit the vision of broad use of chiplets.
- For high-performance, advanced technology heterogeneous products -- the industry is now mainly driven by specific integrators & their trusted bare die providers
- Challenges that need the most focus include:
  - *Wafer probe, reduced-pincount DFT/test methods*
  - *Final Test content & test support logistics*
  - *End-to-End Data analytics*

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