



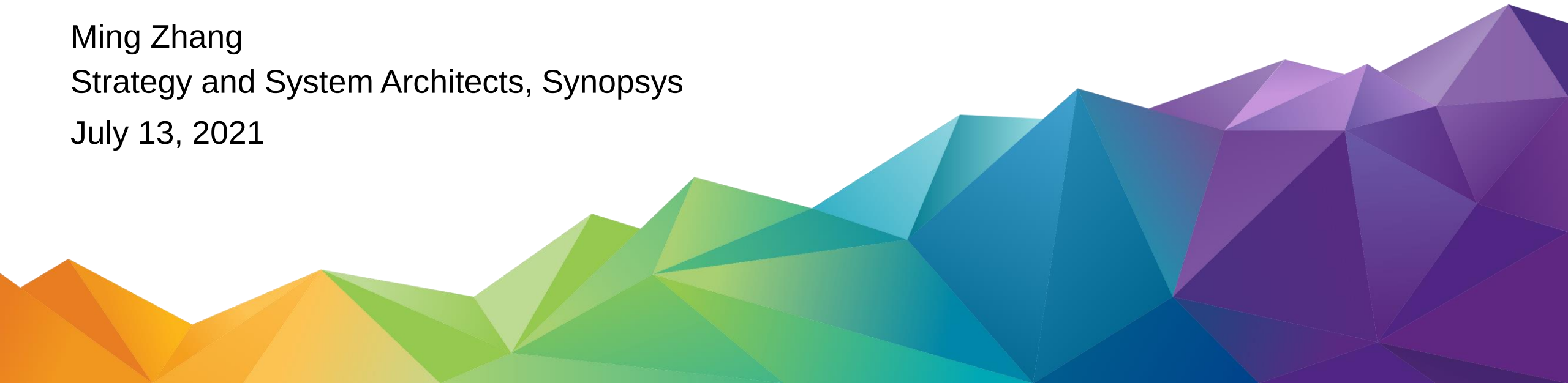
Road to Chiplets: Architecture

July 13 & 14, 2021



Road to *Chiplets*, and the Next **1000X**

Ming Zhang
Strategy and System Architects, Synopsys
July 13, 2021



Outline



Why chiplets, and where

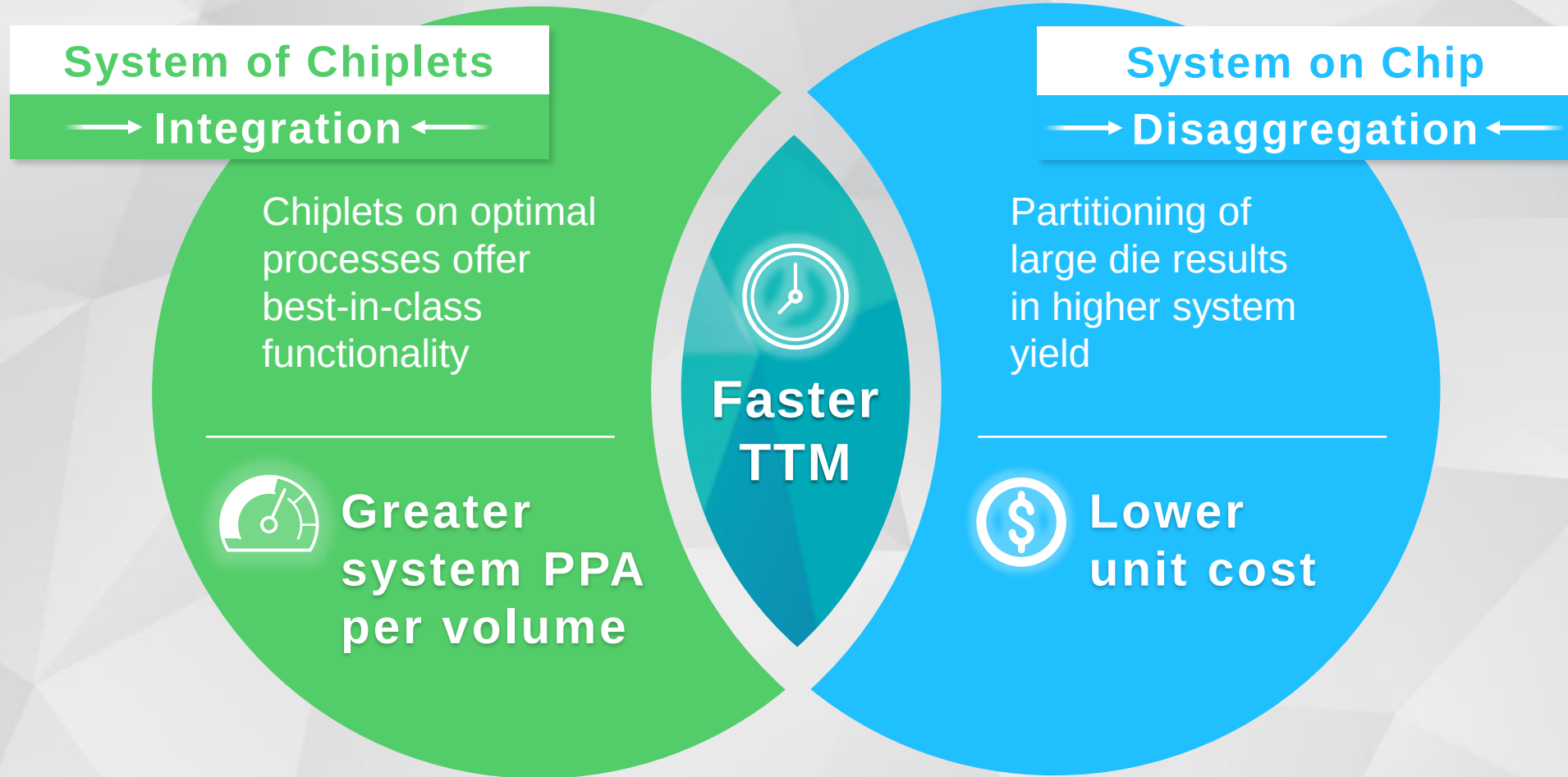


How architecture, design, and manufacturing are now different



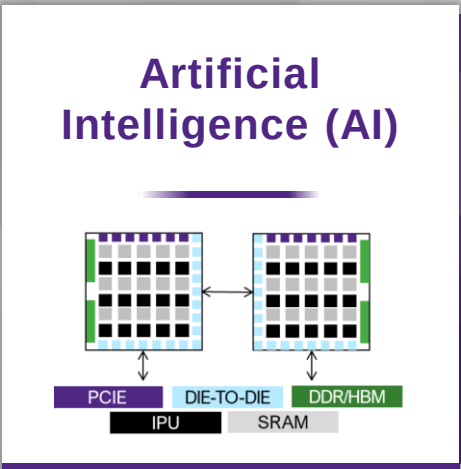
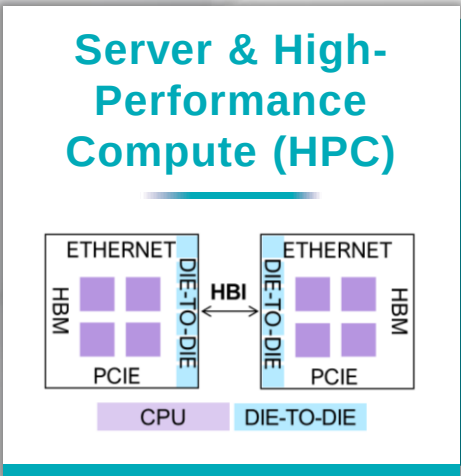
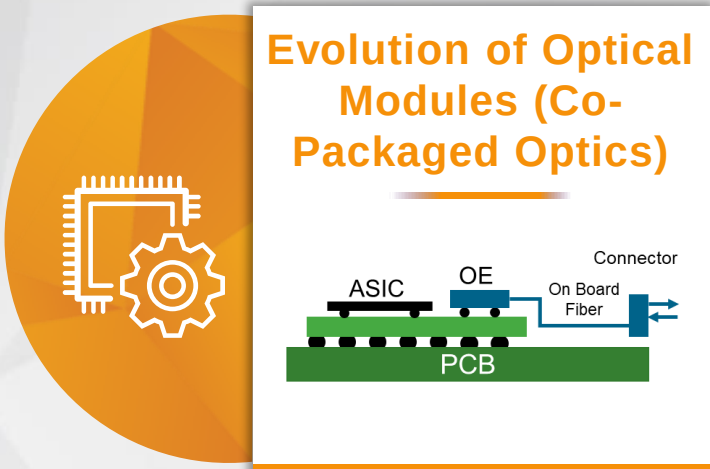
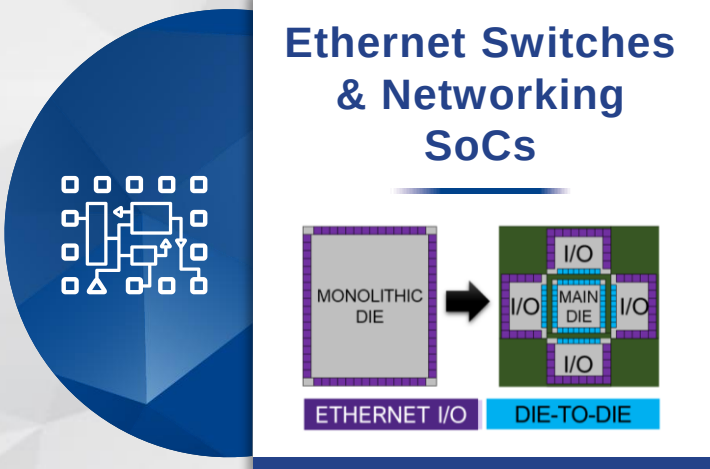
How our industry can give wings to innovators of the next 1000X

Why Chiplets



Common Use Cases

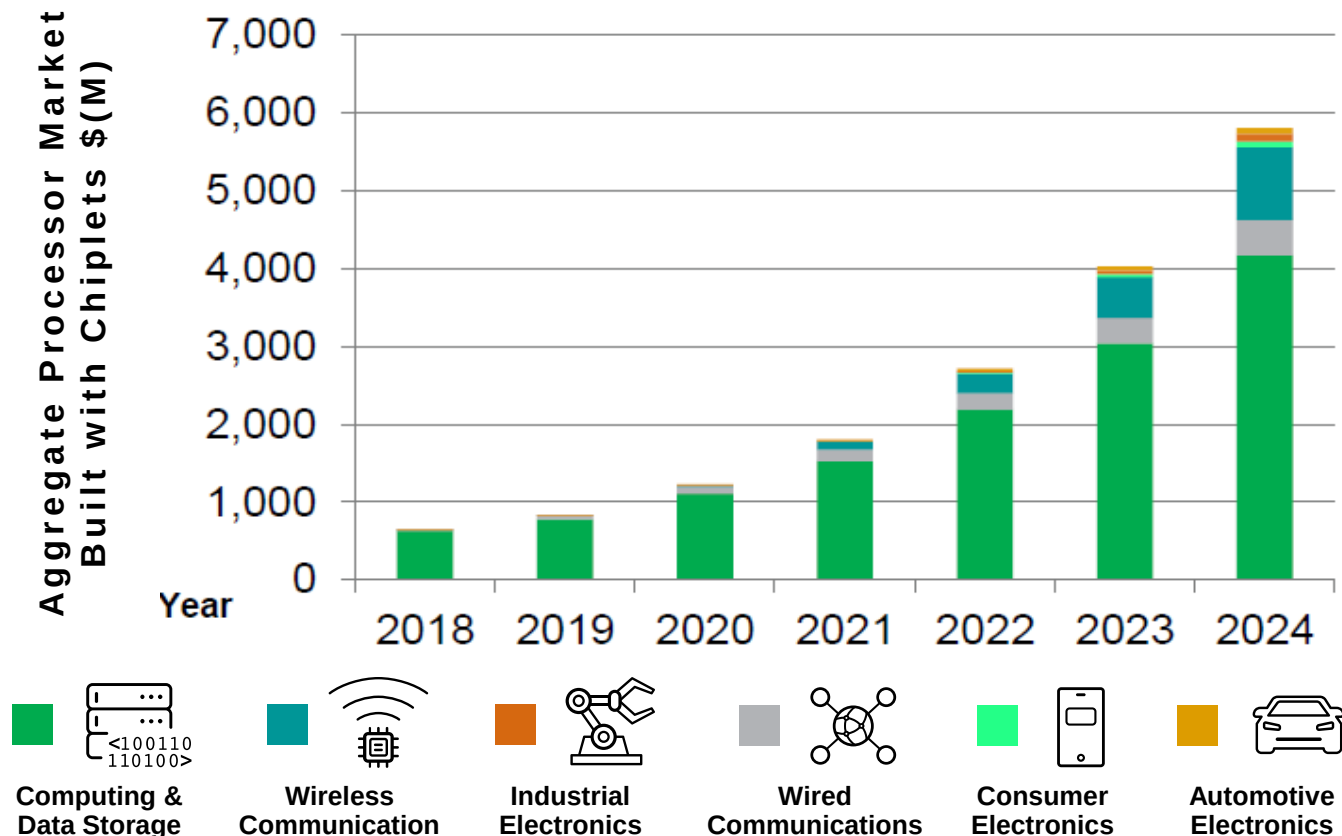
INTEGRATION



DISAGGREGATION

Data Center & Networking Drive Growth

Overall Chiplet SAM by Market Segment

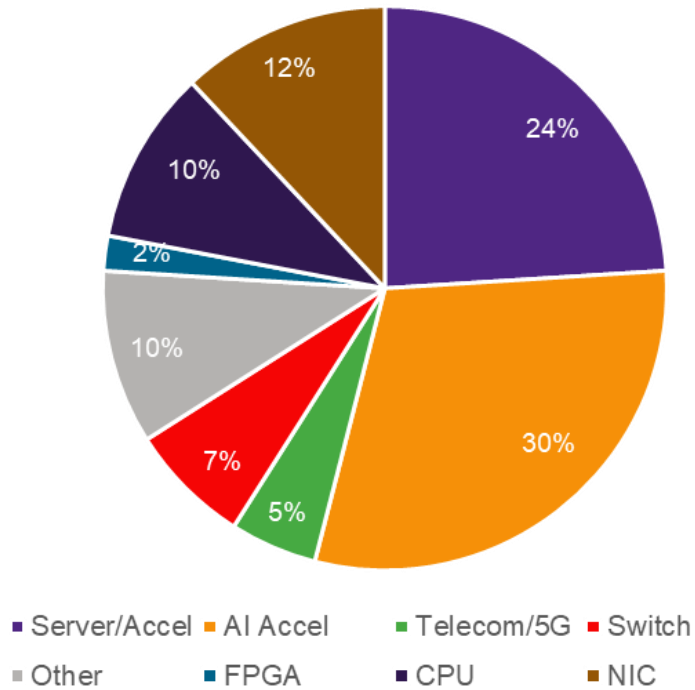


Source: IHS Markit, 2019

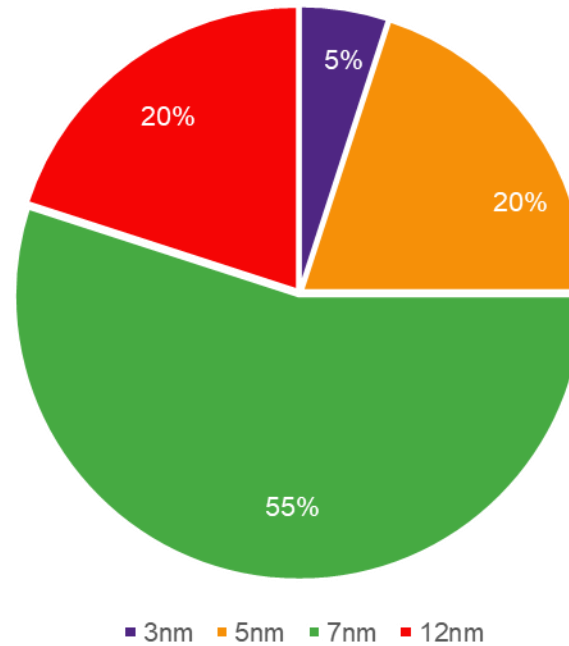
- ~\$6B by 2024 (CAGR of ~10%)
- ~\$60B by 2035
- Initially driven by HPC & Data Center
- Wireless Communications catching up

Diverse Applications Demand Diverse Tech & IP “Menus”

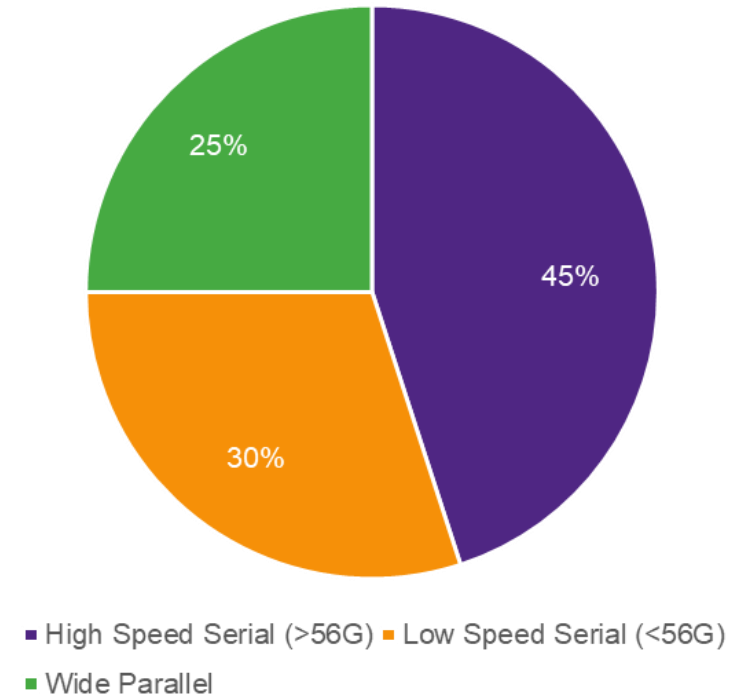
Application



Technology Node

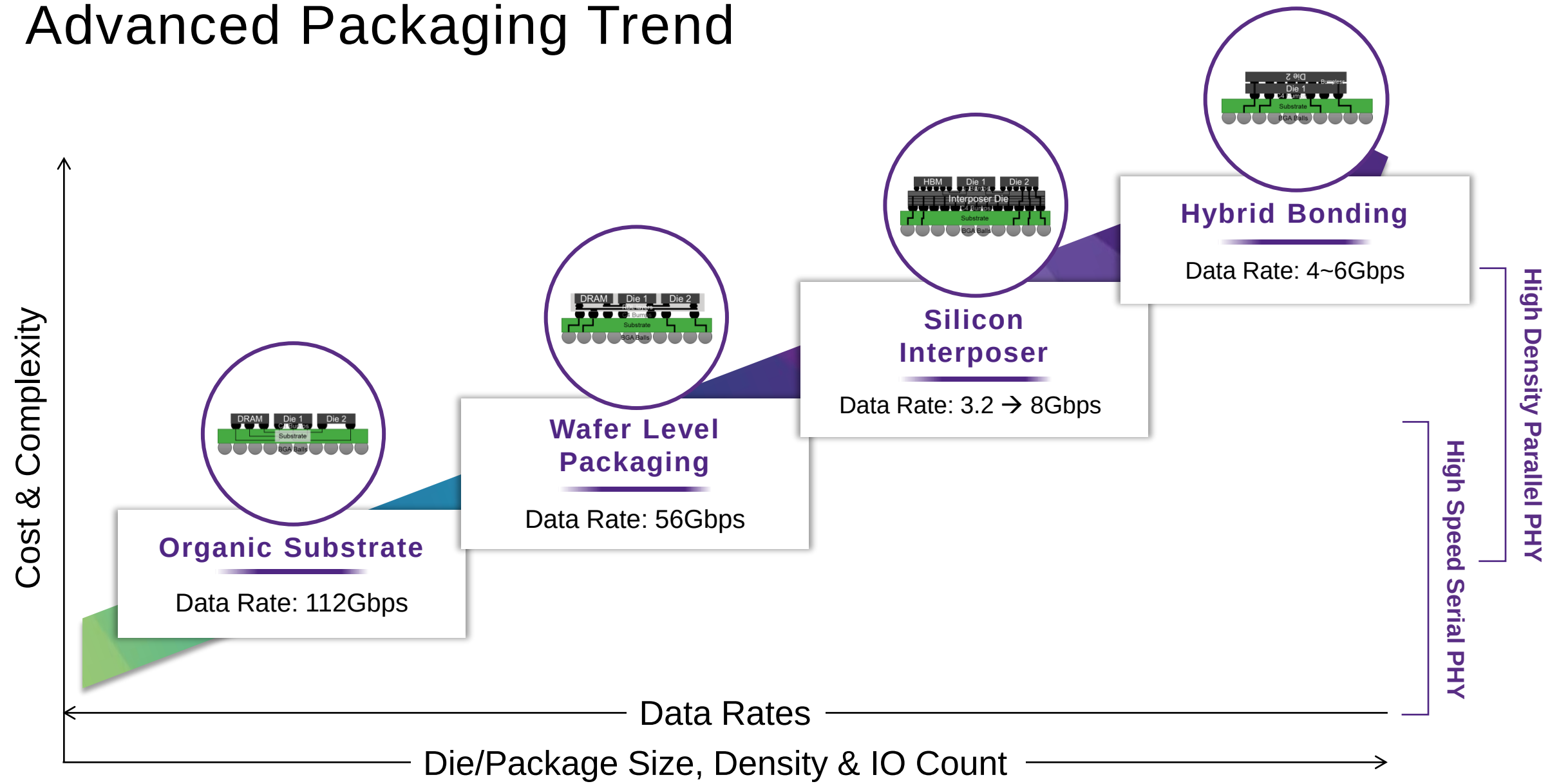


Interface Type



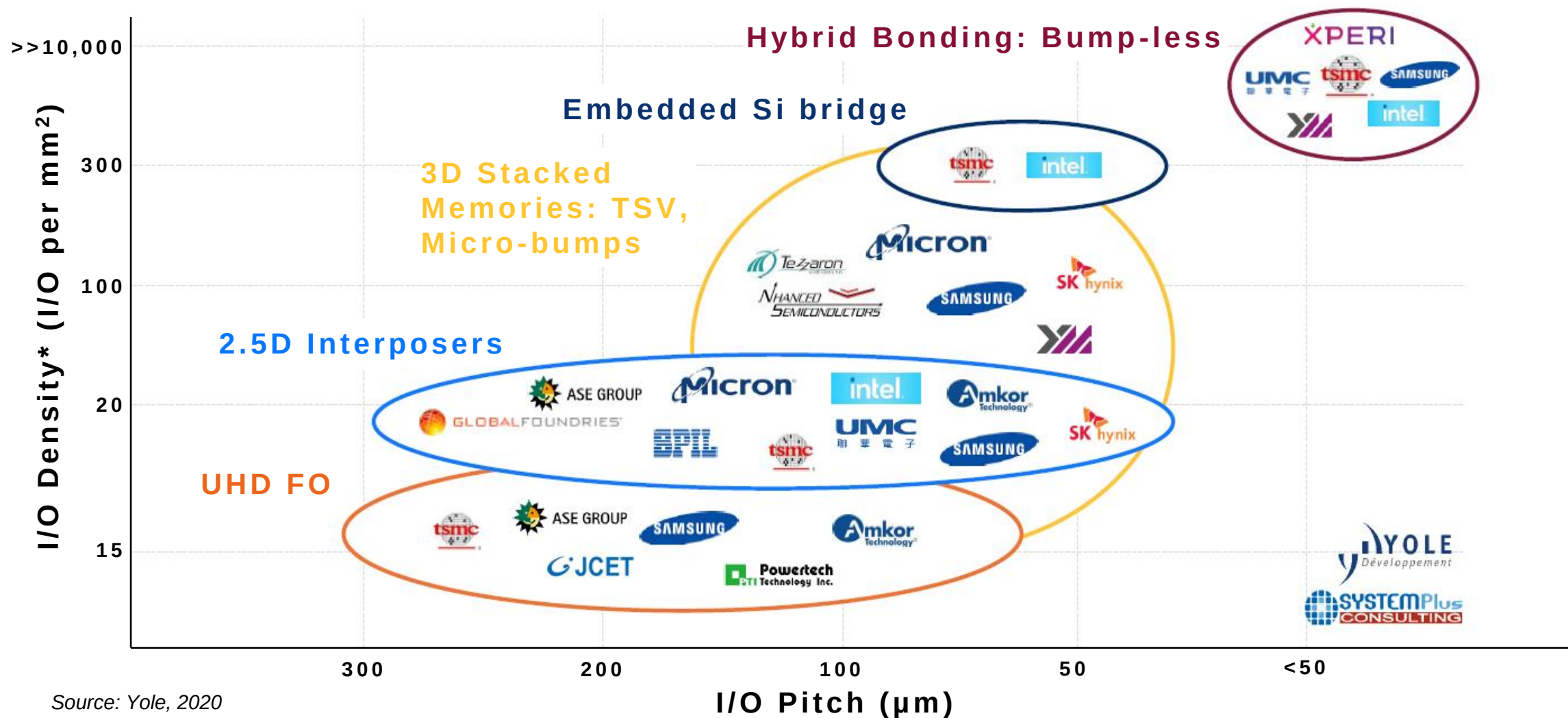
Source: Synopsys Marketing Team, 2020

Advanced Packaging Trend



Advanced Packaging Landscape

Mapping of Players based on Technology



How can We Help Chip Designers Innovate?



Recognize the "new" design targets



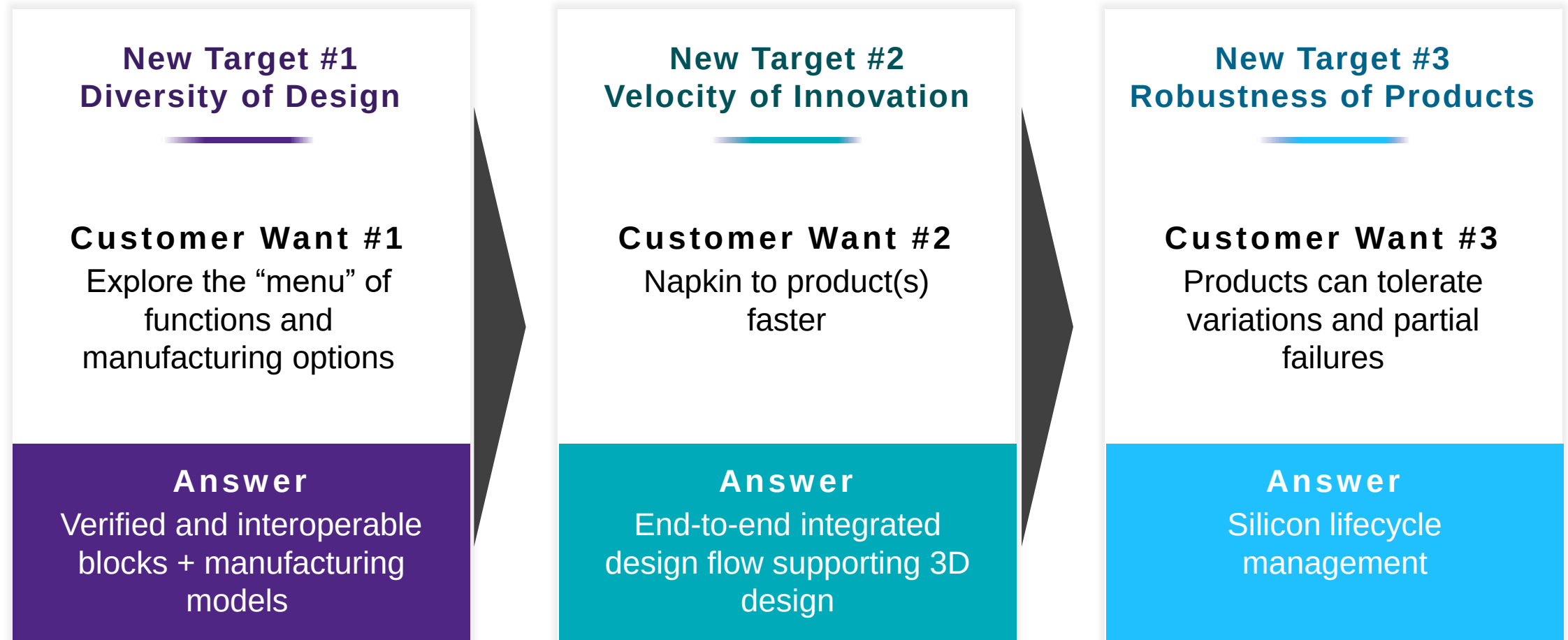
Give them wings



Show them the road (to chiplets)

New Design Targets of The Chiplet Era

Traditional Design Target: PPA

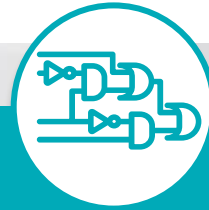


An Ideal Journey for Chiplet-Based Design



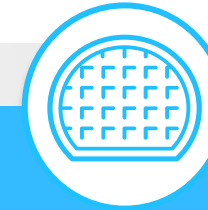
EXPLORE THOROUGHLY

- Substrate choice
- Chiplet / IP choice
- Early PPA / Reliability / Cost



DESIGN RAPIDLY

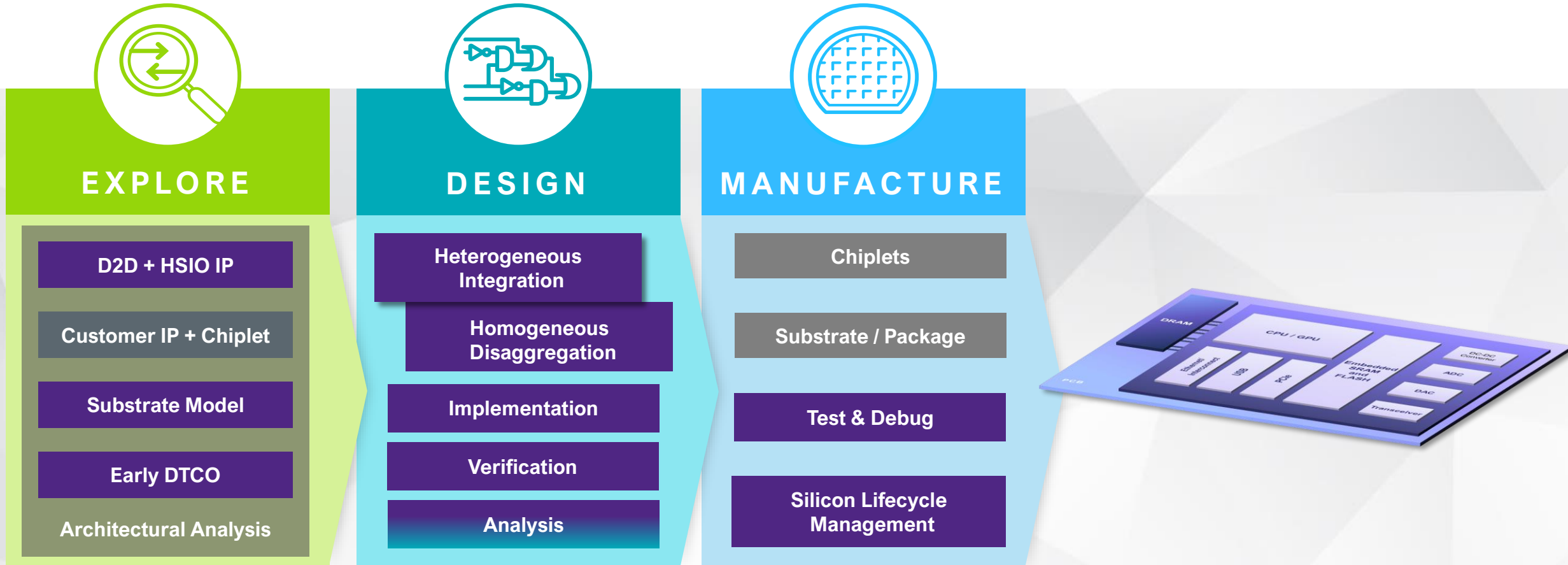
- Design IP, RTL to GDS
- Optimization
- SKU Variation



MANUFACTURE ROBUSTLY

- Cost (Yield)
- Time to Volume
- In-field Safety, Security & Reliability

Total Solution = Interface IP + Design Platform + Manufacturing



Correct by Construction. Secure by Design.

Manufacturing Enablement

KEY: Synopsys Technology

How can We Help Chip Designers Innovate?



Recognize the "new" design targets



Give them wings



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Enabling the New Design Targets

Diversity of Design

Verified and
interoperable blocks +
manufacturing models

Velocity of Innovation

End-to-end
integrated design flow
supporting 3D design

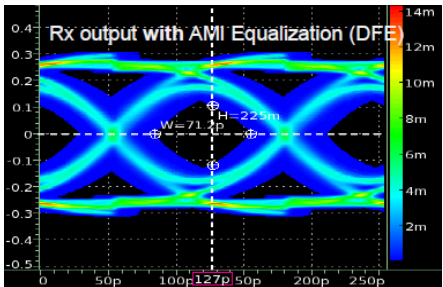
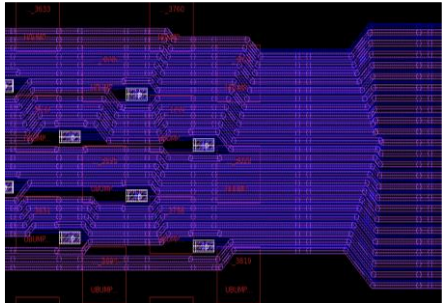
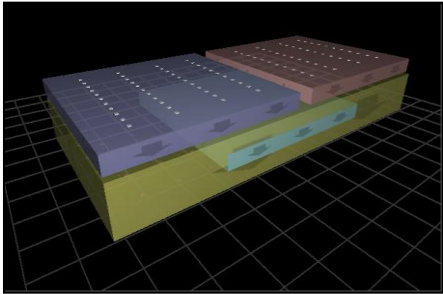
Robustness of Products

Silicon lifecycle
management

Interface IPs Adapt to Diverse Manufacturing Options & Use Cases

Assembly Density / Optimal Integration				
Packaging technology	2D – Substrate	2.5D – RDL Fanout	2.5D – Si-Interposer / Bridge	3D – Die Stacking
D2D architecture	SerDes	SerDes / Parallel	Parallel	Bumpless (Parallel)
Reach	Range			
Bump Pitch				
Data rate / lane				
Power efficiency				
Latency				
Standards	OIF: CEI-112G-XSR/USR JEDEC: JESD204x		OCP: OpenHBI, BoW ChipsAlliance: AIB	
Use Cases	- Heterogenous integration: 5G, ADC, Sensors - SiPhotonics/CPO - Low-cost Server/AI	- High radix Switches - Mid-range/Edge compute - Servers/AI - Automotive	- High-end HPC - AI training, Servers - HBM memory	- High End HPC - SRAM, memory access - Mobile compute

Unified Design Platform from A to Z



3D Pathfinding

3D Design Architecture

Place & Route

Test

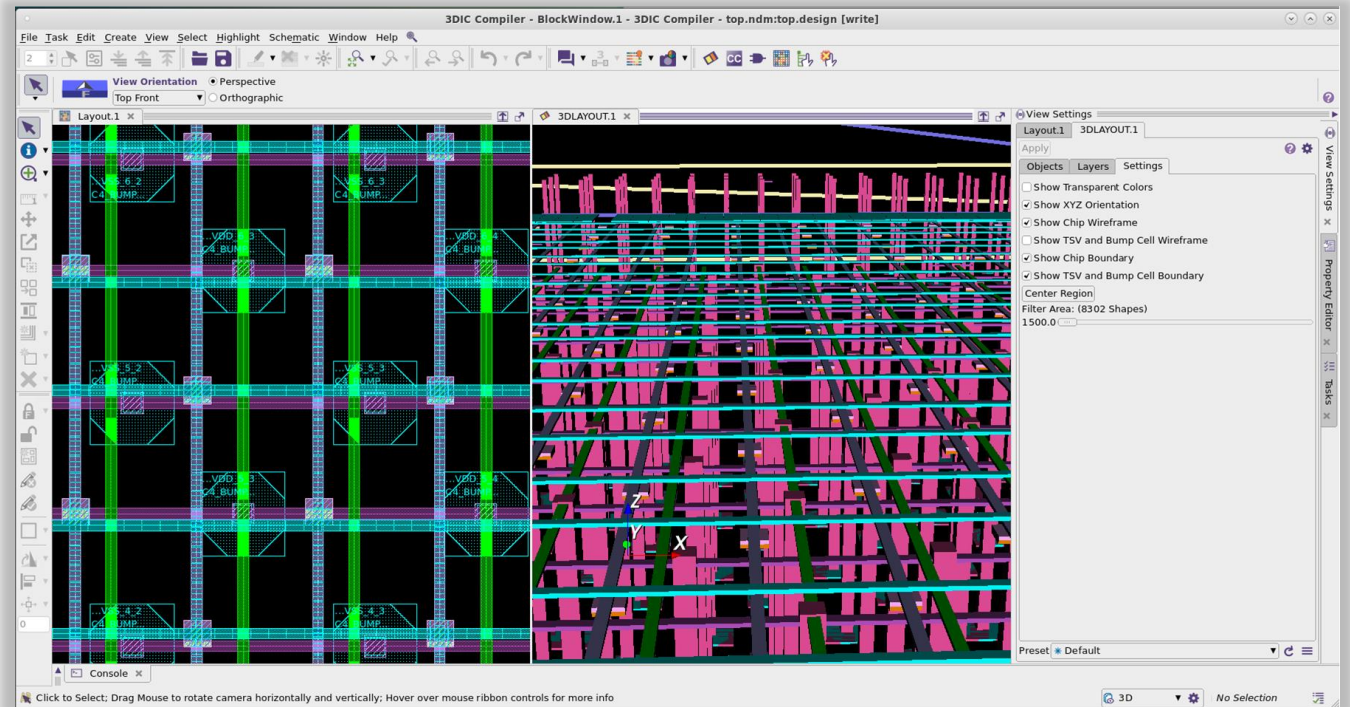
Extraction

Signal & Power Integrity

Thermal Integrity

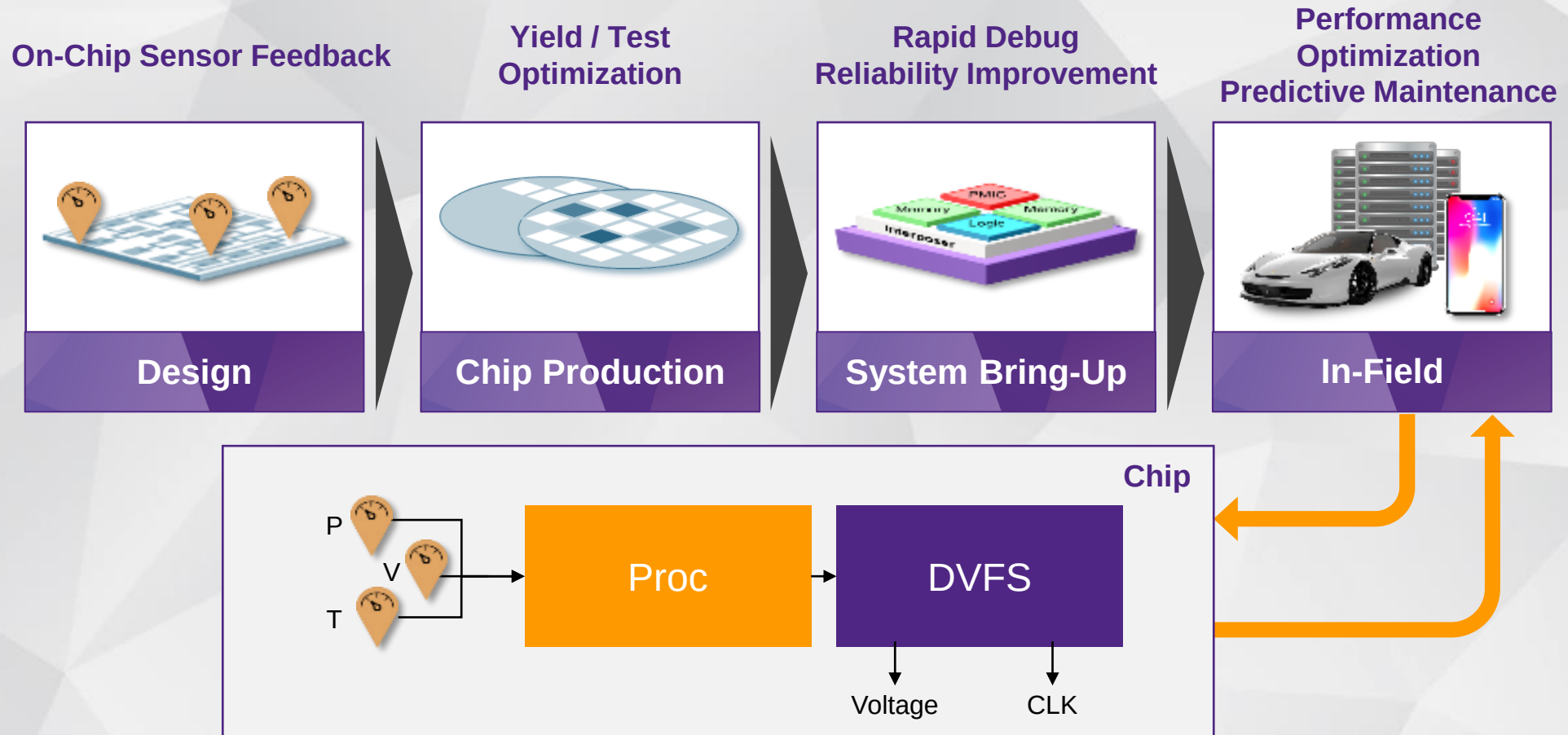
Timing Analysis

Physical Verification



Long Live the Chips

Silicon monitoring and data analytics improve design quality



How can We Help Chip Designers Innovate?



Recognize the "new" design targets

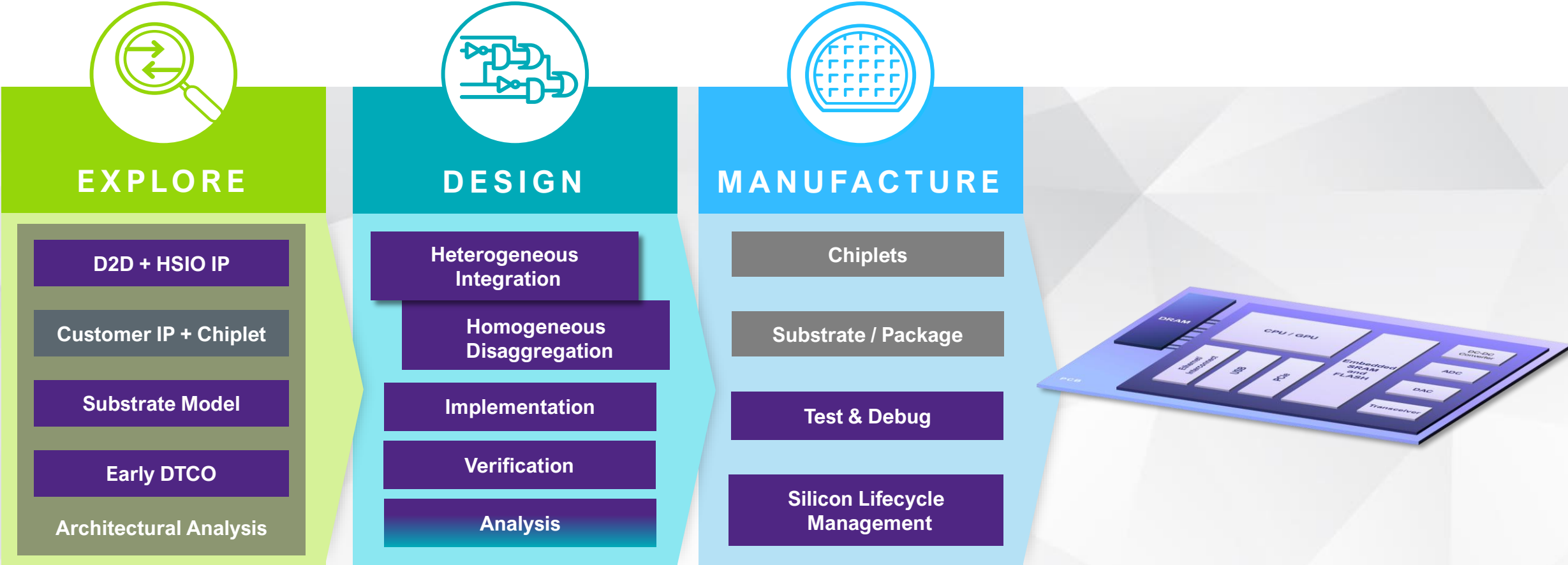


Give them wings



Show them the road (to chiplets)

Total Solution = Interface IP + Design Platform + Manufacturing



Correct by Construction. Secure by Design.

Manufacturing Enablement

KEY: Synopsys Technology

Chiplets are the Road to the Next 1000X

- Holistic system optimization across **X**, **Y** and **Z** dimensions
- Heterogeneous integration of **100+** best-in-class chiplets
- **Billion+** 3D interconnects



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— **Risto Puhakka**, President VLSIresearch

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Engineering Services
Broad Portfolio



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Execution
Automation



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Manufacturing Footprint
Local Sales & Support

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