Road to Chiplets: Architecture

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Design of Heterogeneous Integrated Circuits Chiplets, Modeling, and Data Exchange

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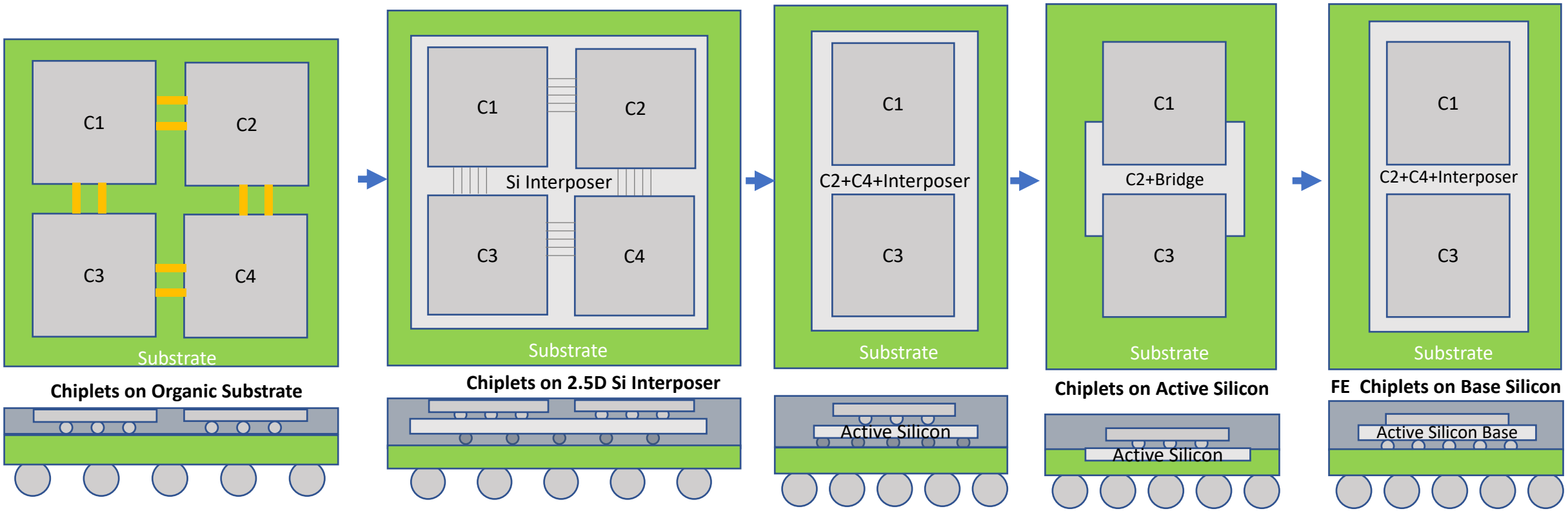
Outline

1. Chiplets
   - Heterogeneous Integrated Circuits with Chiplets
   - Chips vs Chiplets
   - Chiplet Models
   - Early-stage architecture and design For heterogeneous IC designs
2. Design of Heterogeneous ICs
   - Design Steps and Workflow
   - Power Mechanical and Thermal
   - Signaling
   - Test
3. Operations and Test
   - Testing Strategy and Ops Flow
   - Design for System Level Test
4. Summary

Integrated Circuits With Chiplets

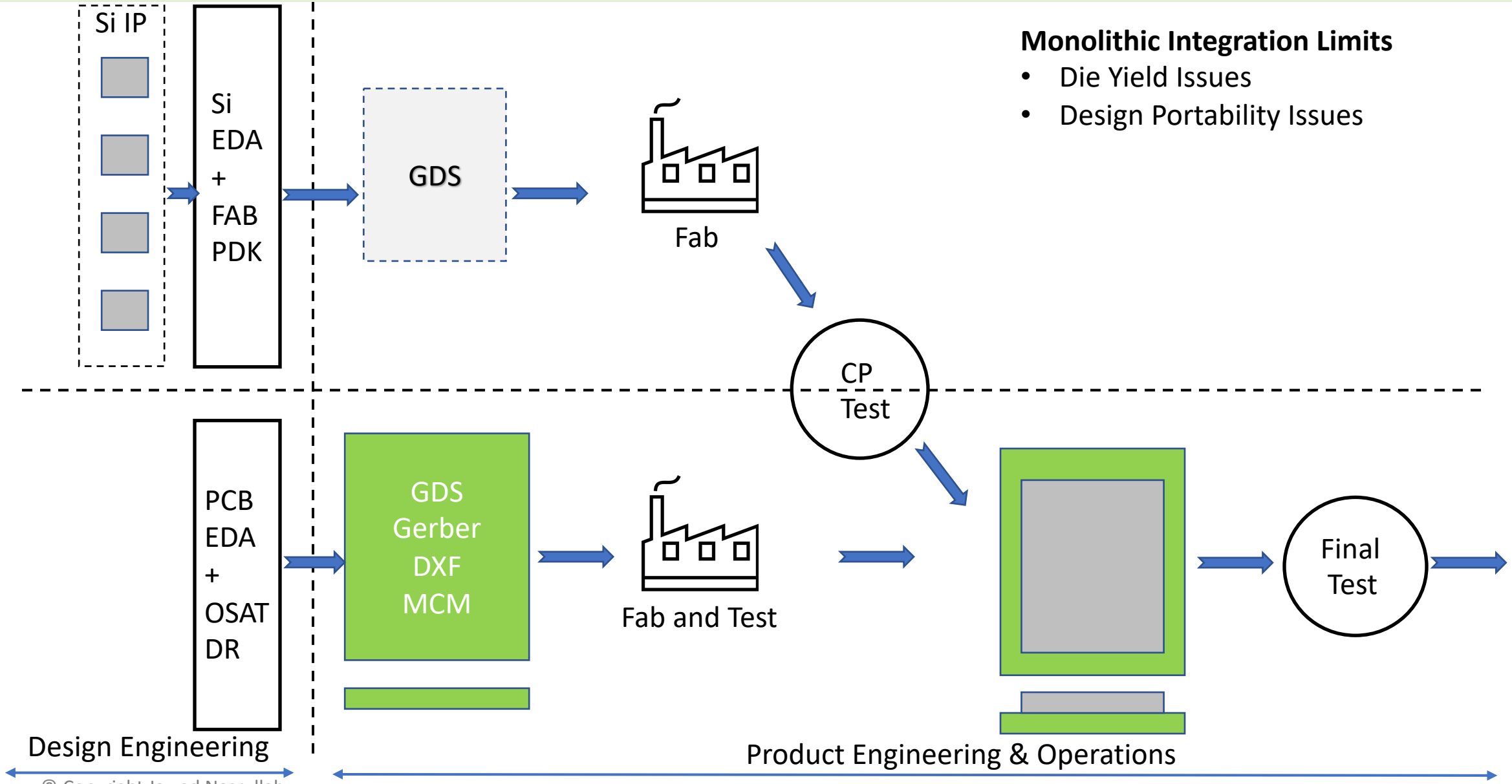


Chiplet on Organic	2.5D Chiplets	Active Interposer	Si Bridges	FE Chiplets
Substrate/Fanout, Si (--)	Si, Substrate/Fanout (++)	Si, Substrate/Fanout (++)	Substrate/Fanout, Si (-)	Si, Substrate/Fanout (++)
$	$$$	$	$$	$
Value	Value++	Value++	Value+	Value+++

Chips vs Chiplets

	Chips	Si Hard/Soft IP	Chiplets
State	Physical Goods	IP	Physical Goods
Trading	Buy/Sell with Warranty	Buy/Sell with Warranty	Buy/Sell with Warranty
Warranty	Warranty for DPPM	N/A	Warranty for DPPM
2L Assembly	SMT Capable	N/A	SMT or Wire-bond
Packing	Tape & Reel	N/A	Tape & Reel or Wafer Sale
Verification	Verified with support from IP vendors.	Supports Chip verification.	Supports Assembly verification.
Testing	Testable by Manufacturer. Some have JTAG boundary scan.	N/A	Testable by Customer. Need boundary scan at least.

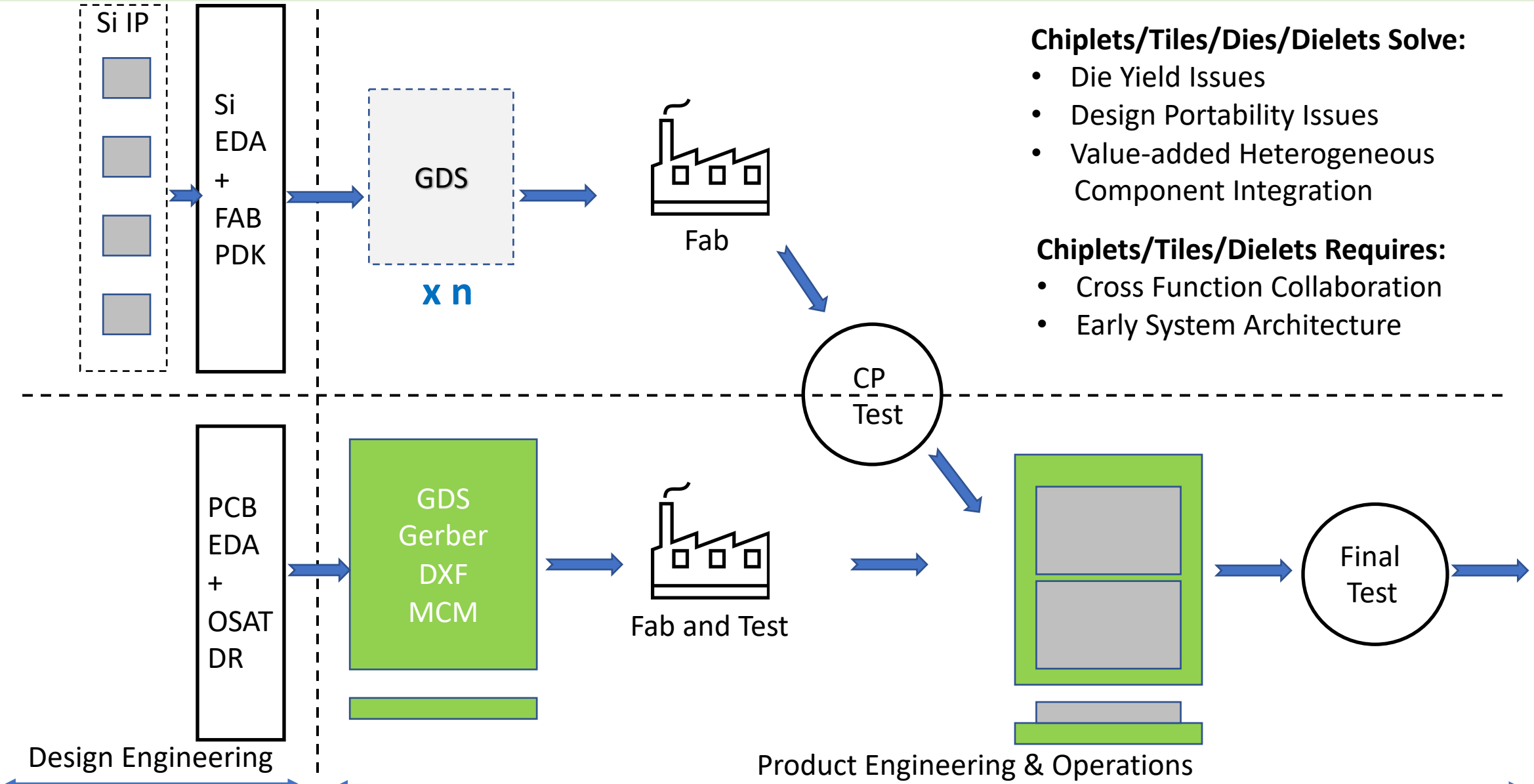
Chips vs Chiplets



Monolithic Integration Limits

- Die Yield Issues
- Design Portability Issues

Chips vs Chiplets



Chiplets/Tiles/Dies/Dielets Solve:

- Die Yield Issues
- Design Portability Issues
- Value-added Heterogeneous Component Integration

Chiplets/Tiles/Dielets Requires:

- Cross Function Collaboration
- Early System Architecture

Chiplet Models

Models	Chips	Si Hard/Soft IP	Chiplets
Mechanical	Data Sheet	N/A	MCM, DIE, XDA, AIFF, LPB, ZEF, GDS, Gerber, DXF, JEP30, Verilog AMS
Thermal	Data Sheet	N/A	ECXML
Behavioral	Data Sheet	Verilog/System C	Sys Verilog/ Verilog AMS/System C/Data Sheets/ESL
IO	Data Sheet	Verilog A/AMS	IBIS
Electrical	Data Sheet	Data Sheet	CDX / EC Tables / IP-XACT
PI/SI	Data Sheet/CPM		CPM
Test	Data Sheet/JTAG	Verilog	IEEE 1149.1/1149.6/1500/1838/…

- Chip design can generally be done top down due to the very rich, well supported ecosystem.
- Chiplet based designed are a mixture of top down and bottom up as it is a nascent ecosystem.
- We need all the support for chiplets with electronically sharable models.
- ODSA/CDX whitepaper to make chiplet model recommendations soon.

Design and Manufacturing Steps—Chips / Chiplets

DESIGN STEPS

1- Architecture

2- Design Entry
- IO Planning
- RTL Design and Verification
- Schematic Capture
- Component Placement

3- Chip Layout / Routing / Package Layout

4- Verification
- Functional/Formal
- Electrical
- Thermal/Structural

5- Send to Manufacturing

MANUFACTURING STEPS

1- Wafer Fab, Contact Probe

2- Package Fabrication (Optional), e-test

3- Bump/Assembly/CSP/BGA

4- Packaged Part Test

5- ESD and Latchup Tests (sampling)

6- Reliability Tests (sampling)

7- Infant Mortality Burn-in

8- Final Test

Design and Manufacturing Steps—Chiplet Integration

DESIGN STEPS

1- Architecture, Chiplet selection, Package Technology Selection

2- Design Entry
- IO Planning
- RTL Design and ESL Verification
- Schematic Capture/Netlist Gen
- Component Placement

3- Substrate/Interposer Routing and Layout

4- Verification
- Functional
- Electrical
- Thermal

5- Send to Manufacturing

MANUFACTURING STEPS

1- Interposer Fab, Contact Probe

2- Substrate Fab, e-test

3- Chiplet Assembly/Packaging

4- System Level Test (structure, function)

5- ESD and Latchup Tests (Sample)

6- Reliability Tests (Sample)

~~7- Infant Mortality Burn-in~~

Development Activities for Chiplet Integration

Architecture

Choose Multi-Die Technology
Choose Chiplets and Signaling
Cost Analysis
Performance Modeling
Early Power Estimation
Choose A Thermal Solution
Design For Structural Integrity
Design For Testing
System Level Test Development

Design

Multi Die Design
System Connectivity
Power Delivery Integrity
Signal Integrity
Cross-Die Timing
Noise Analysis, EMI, IR, XTalk
Detailed Power Model
Thermal Analysis
Structural Analysis
Verification
Design Sign Off

Manufacturing

Wafer Probe
Organic Material Testing
Bring Up Testing
System Level Test
Environment Reliability
Later Life Failure Testing
HVM

Power, Mechanical, and Thermal

“Power Is Everything”

Power Profile	10^{-1} W	10^{0} W	10^{1} W	10^{2} W	10^{3} - 10^{5} W	10^{6} W
Applications	AIoT, Trackers, Wearables	Mobile	Laptops Pads	Servers	Racks	Data Centers
Energy Efficiency Challenge	✓	✓	✓	✓	✓	✓
Thermal Design Challenge		✓	✓	✓	✓	✓

Chip Active Power Top Usage: IO/SerDes/Optical/RF, Compute, Storage

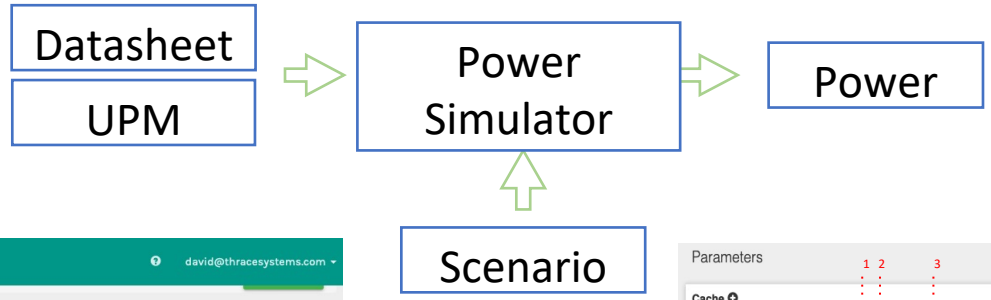
Chip Static Power Top Usage: Transistor Leakage, DC Biasing

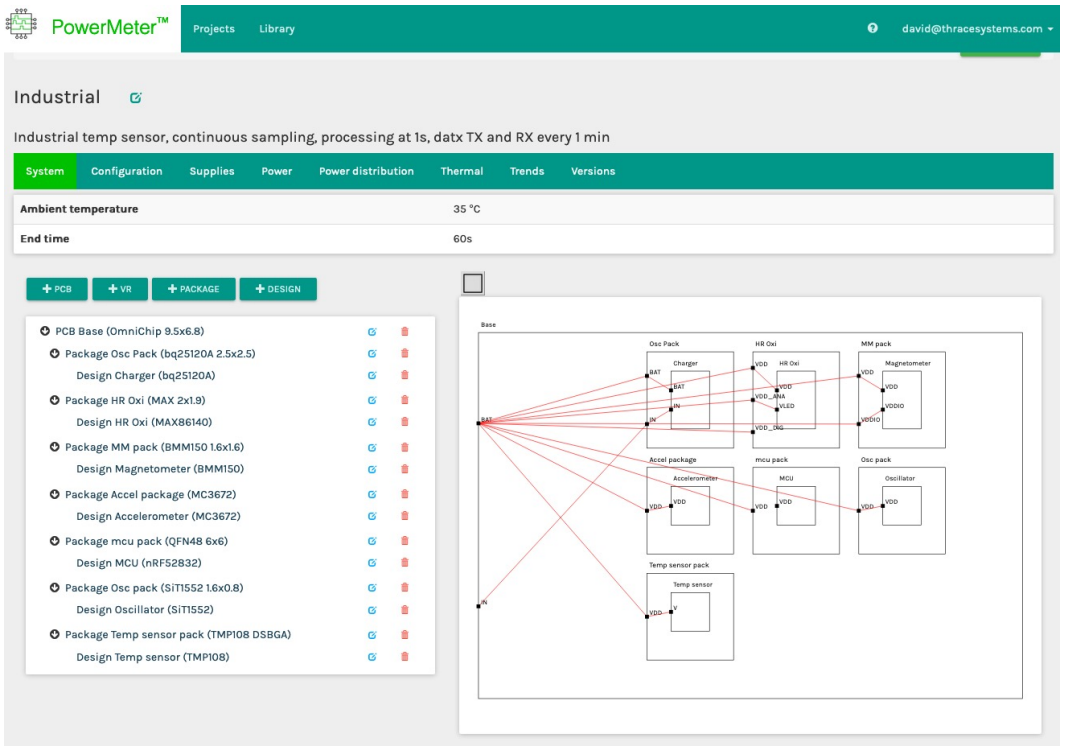
Chip Thermal Design Range: 1mW-1000W

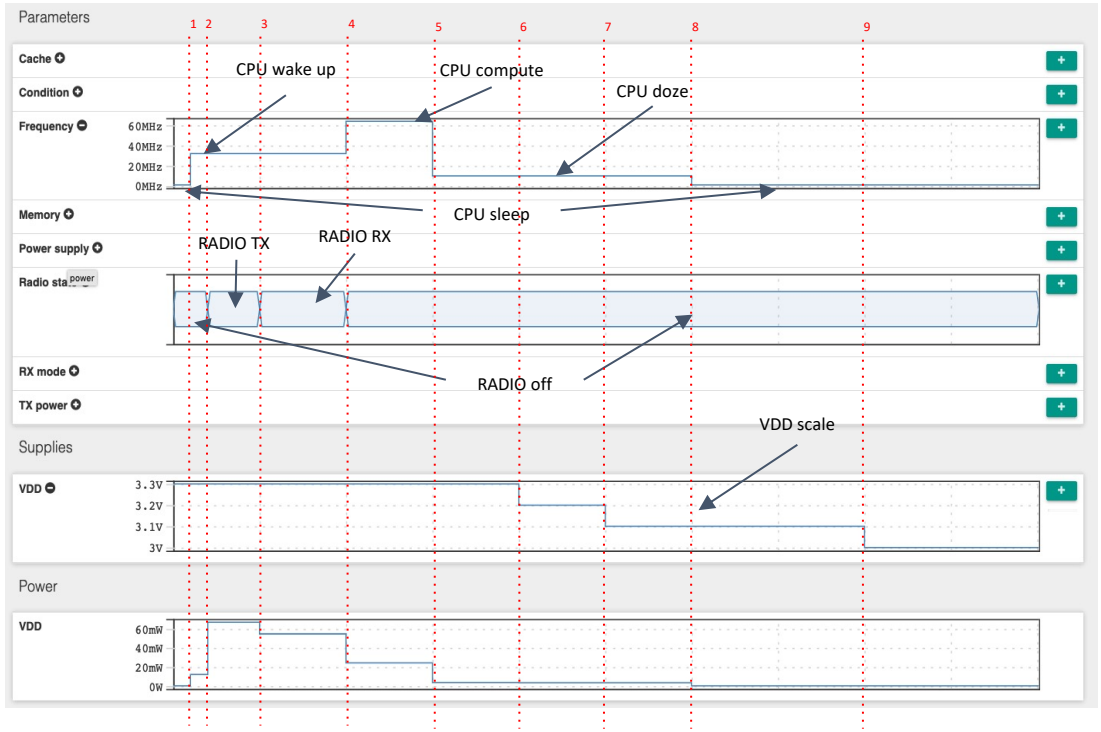
Chiplet System Power Estimation

OPEN DOMAIN SPECIFIC ARCHITECTURE

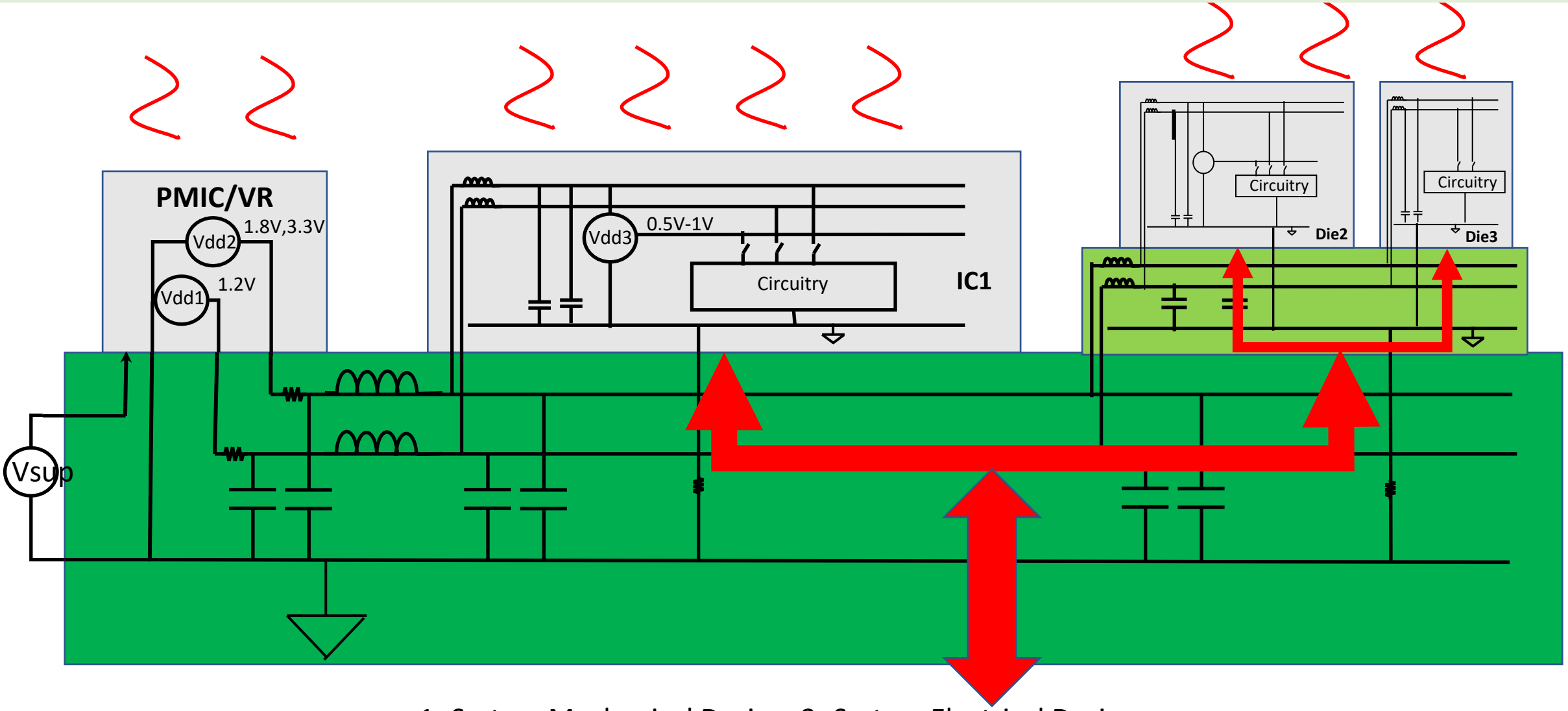
CDX







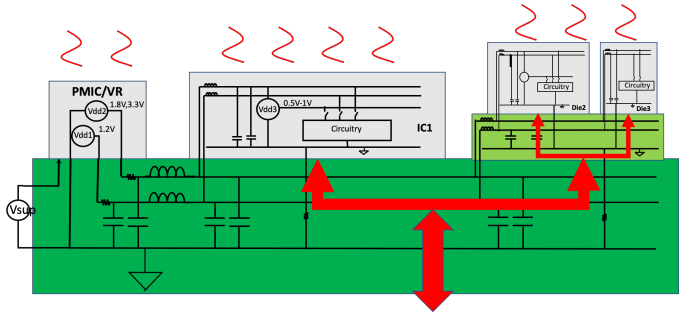
Design for Chiplet Based Systems



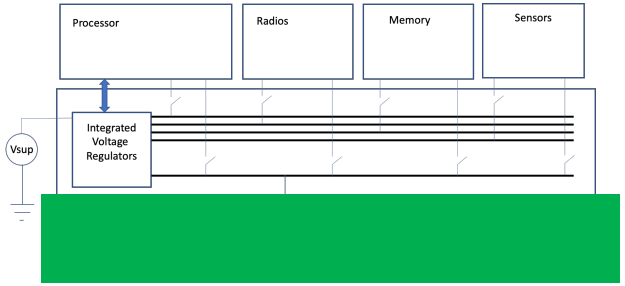
1- System Mechanical Design 2- System Electrical Design

Need for Early Power Modelling

- Side-by-Side Placement (Cheaper and Good-Enough Performance)
  - Easier Shrink of the System (Improves IO Power Dissipation somewhat)
  - Critical Dimensions Shrinking (cost advantage)

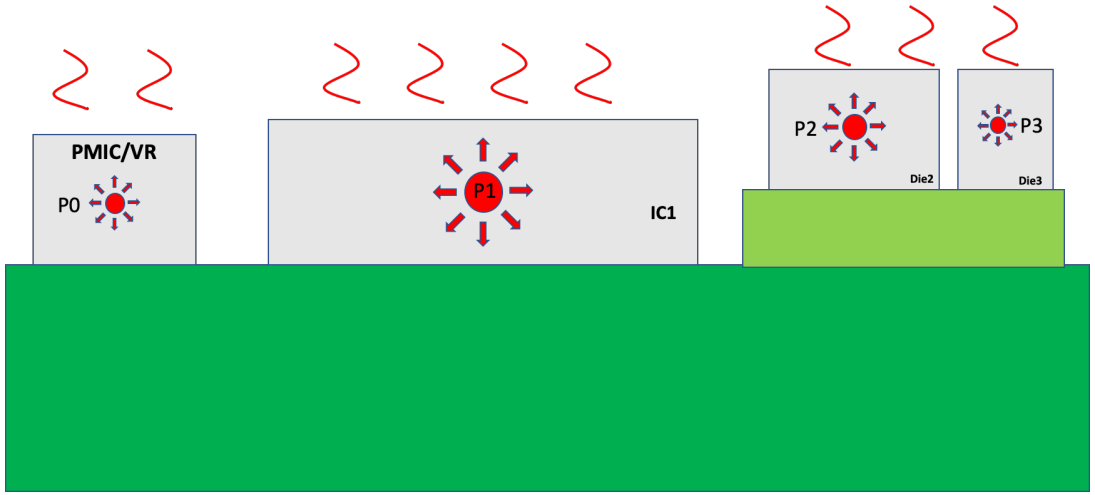


- Vertical Stacking (New Technologies)
  - Vertical Interconnect (Significantly Improves performance and power)
  - Vertical Power Management (Significantly Improved Co-designed Power Management)



Mechanical and Thermal Design

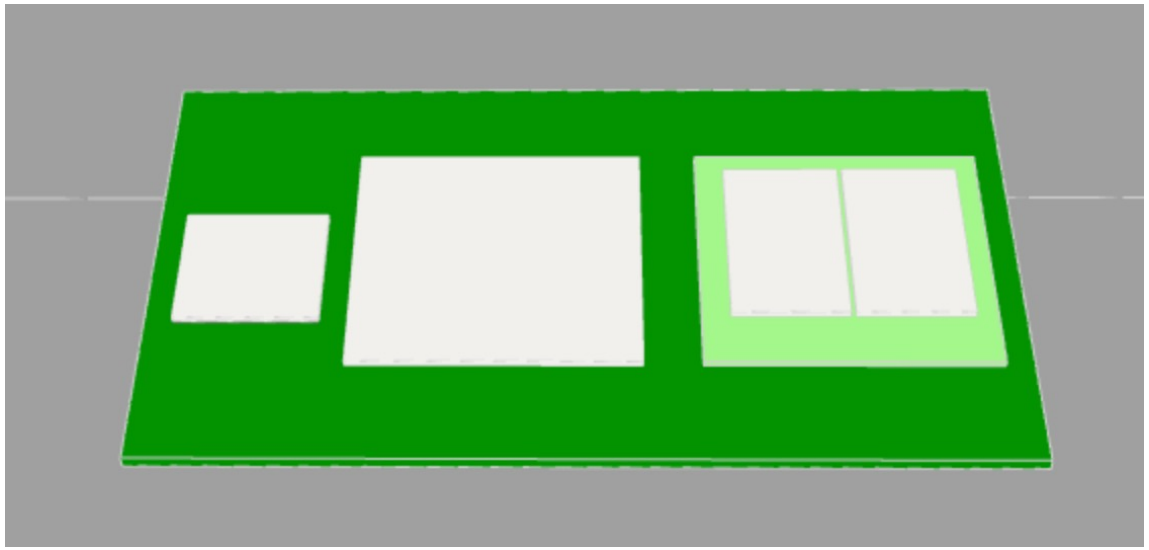
- Thermal and Floor planning
  - Technology Selection
  - Vertical OR Side-by-Side Integration

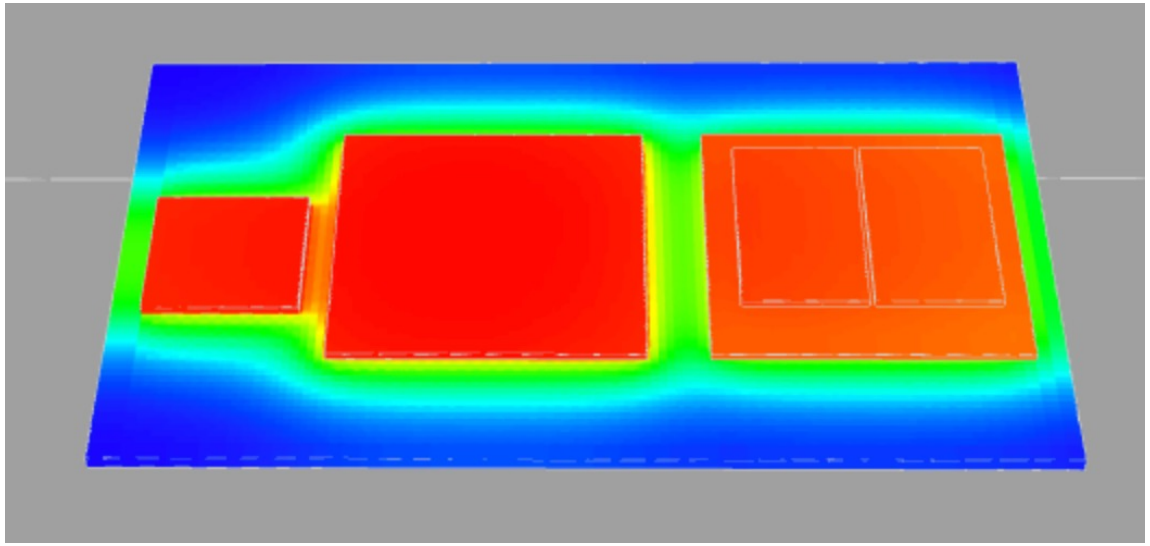


- Power Dissipation Design
  - Heat Spreader, Heat Sink Design
  - Accurate power model is needed for accurate power model (recursive)

  (Leakage model depends on temperature which depends on accurate leakage model among others)

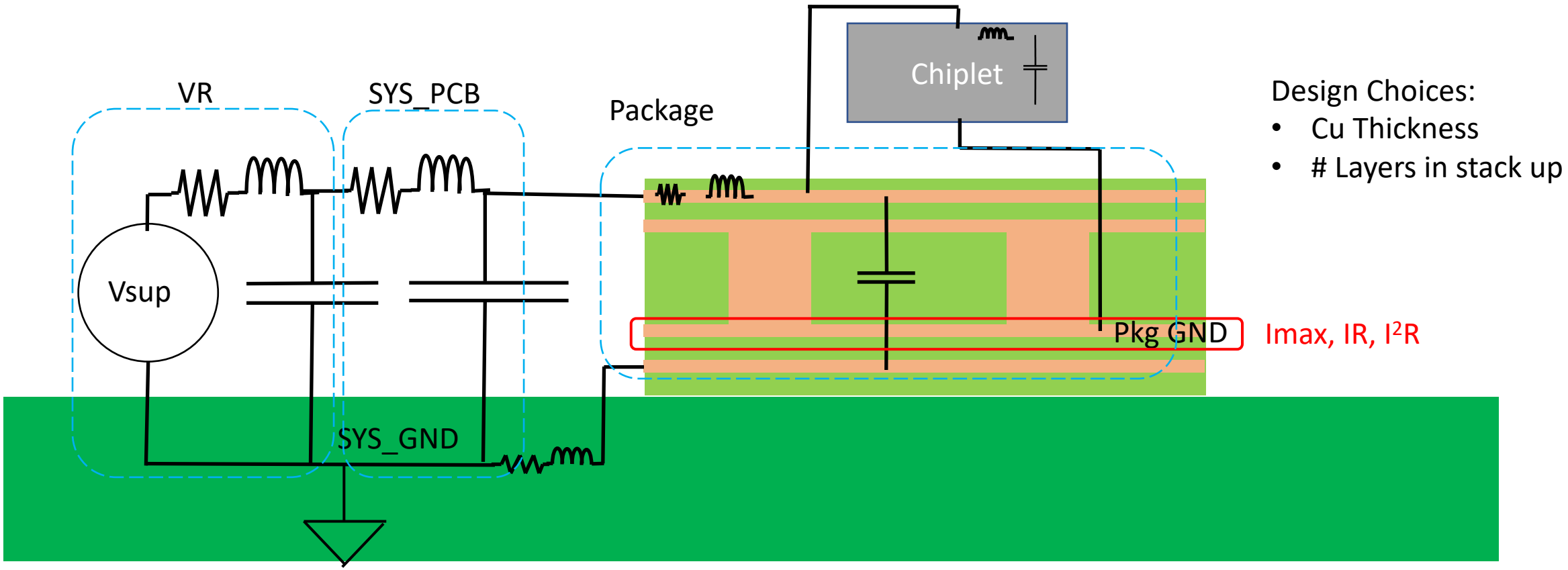
Mechanical and Thermal Design





Thermal Cross Talk and Desensitization
Thermal Run Away
Architecture Power Modulation
Package DVFS

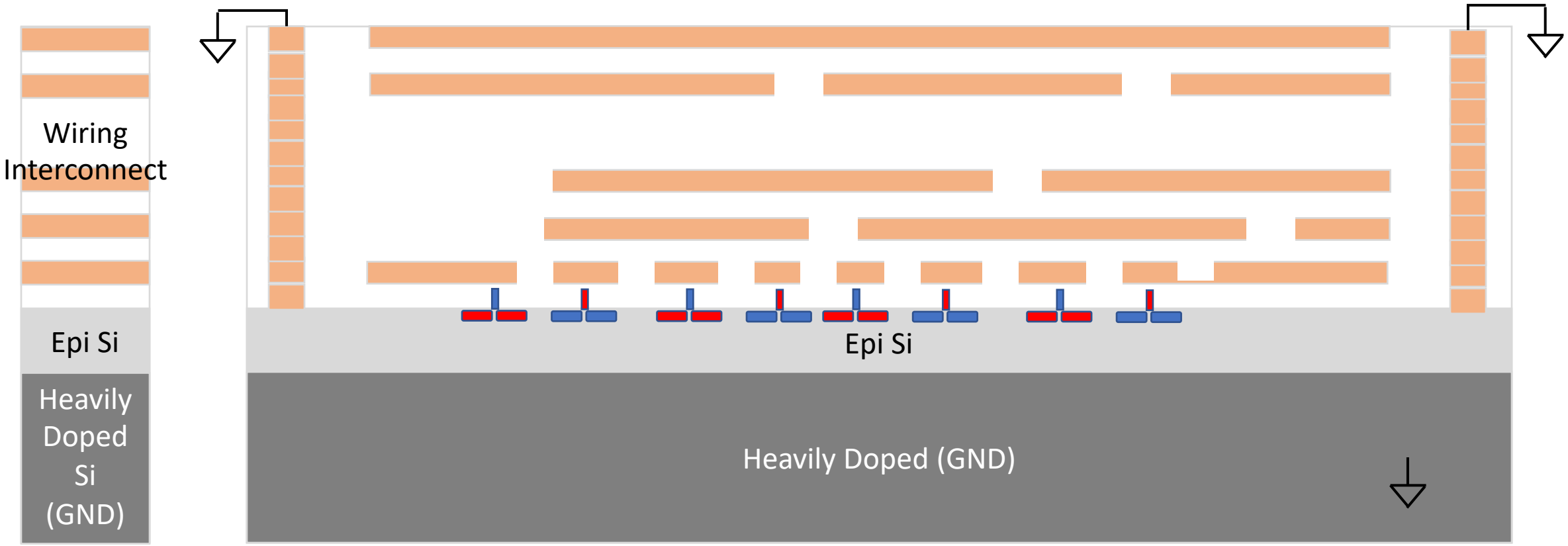
Power Delivery Network Design



- Ground and Power Planes Need to Support IR, I^2R, Droop. Decoupling Capacitors needed.
- Cu Thickness Helps IR, I^2R.
- Little Room for Overdesigning.

Signaling

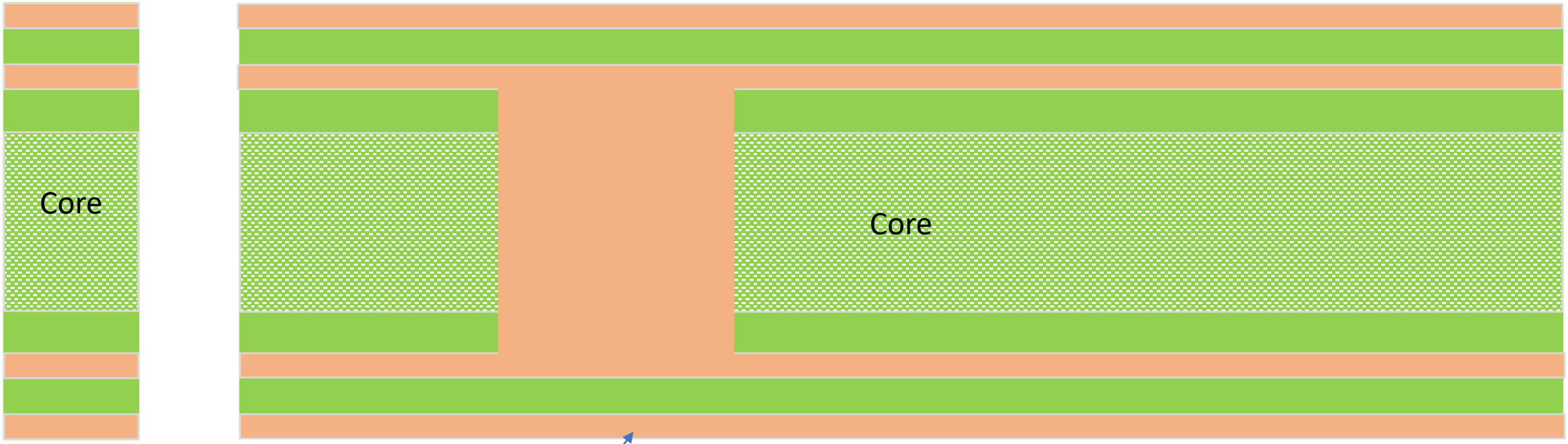
Signaling On Chip

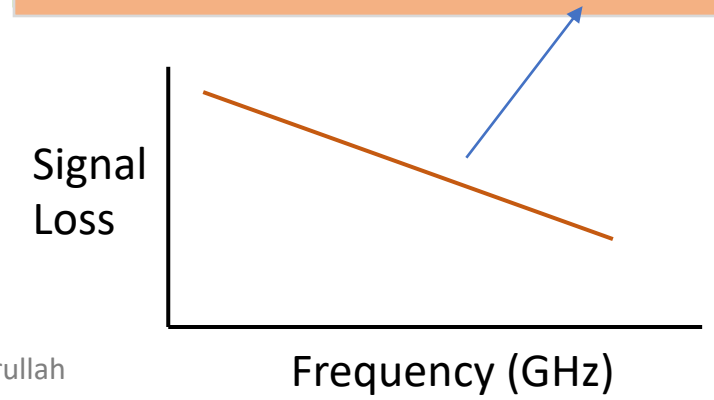


On Chip Signaling = Rail to Rail
IO Signaling = Low Swing, SerDes

C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

Signaling On Chiplet Substrates

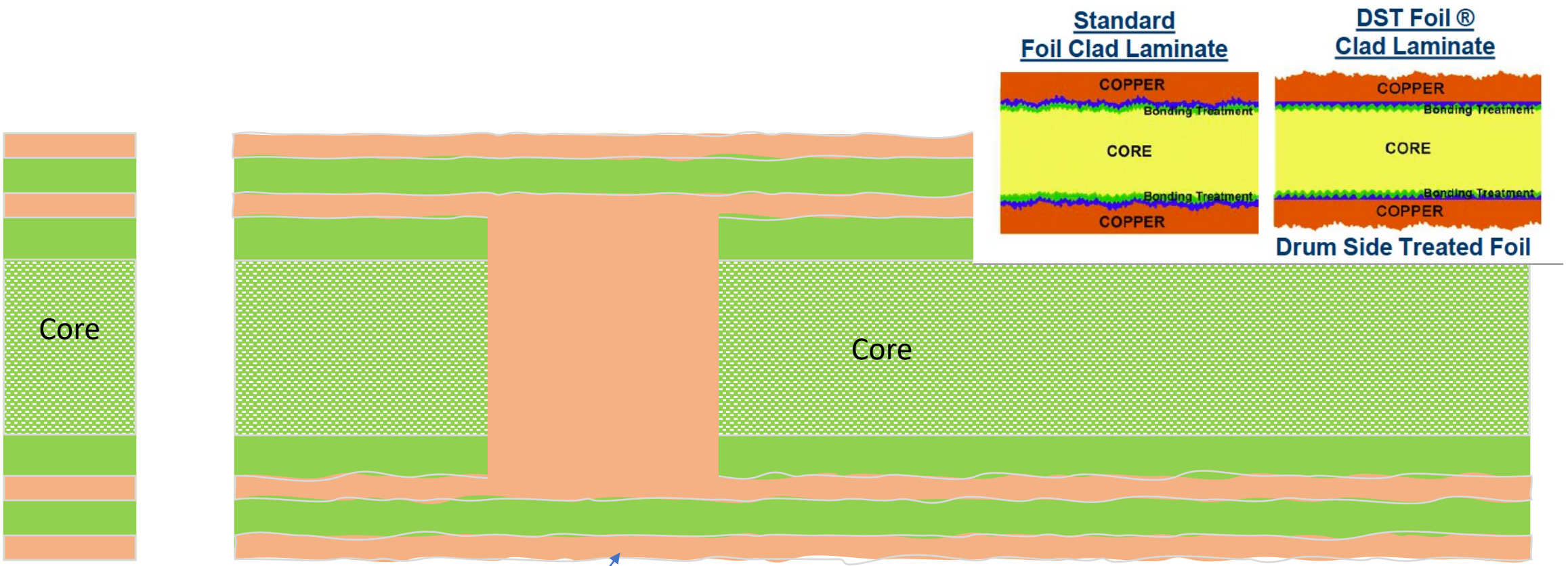


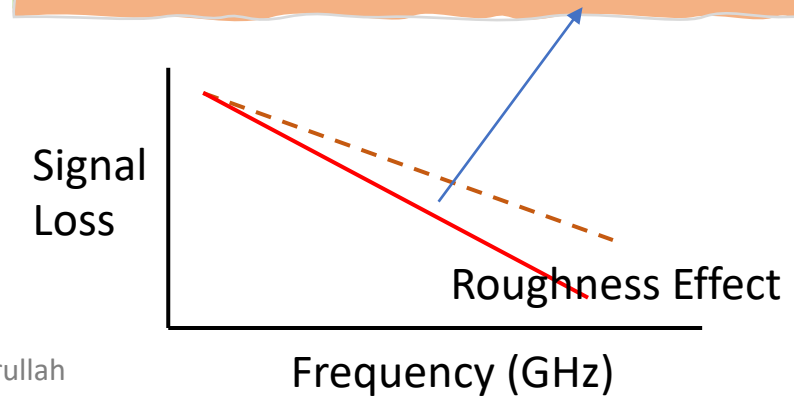


IO Signaling = Low Swing, SerDes
Side-band Signaling = Rail to Rail

C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

Signaling On Chiplet Substrates





IO Signaling = Low Swing, SerDes
Side-band Signaling = Rail to Rail

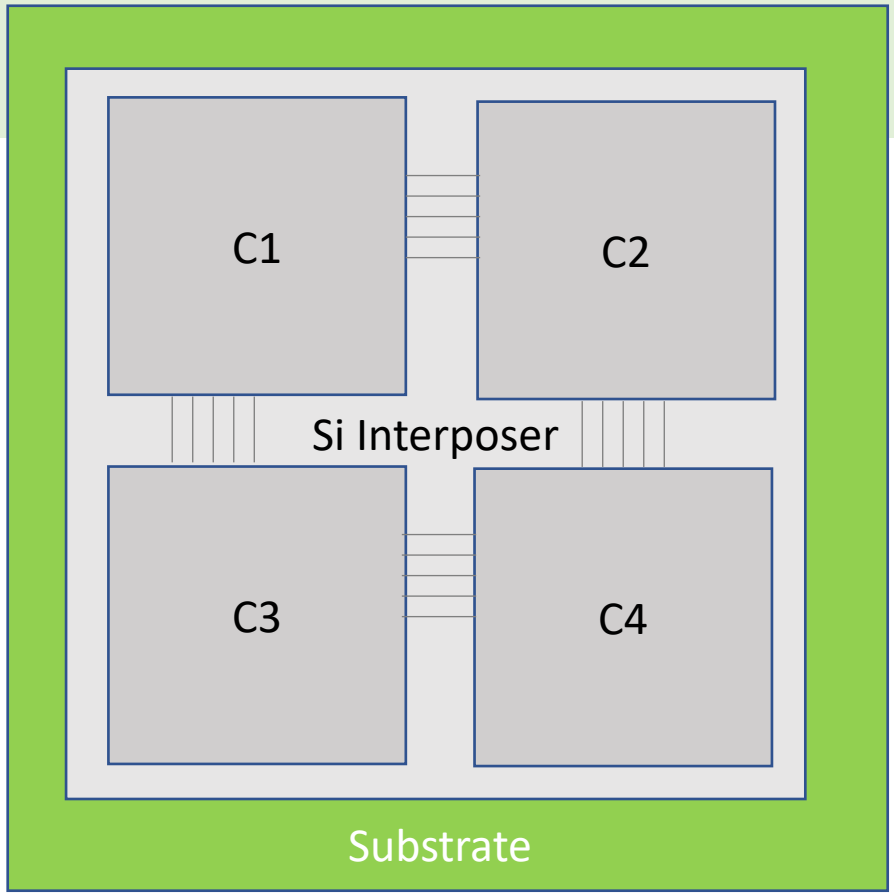
C_wire/mm ~ 250 fF
E/bit/mm ~ 0.1 pJ

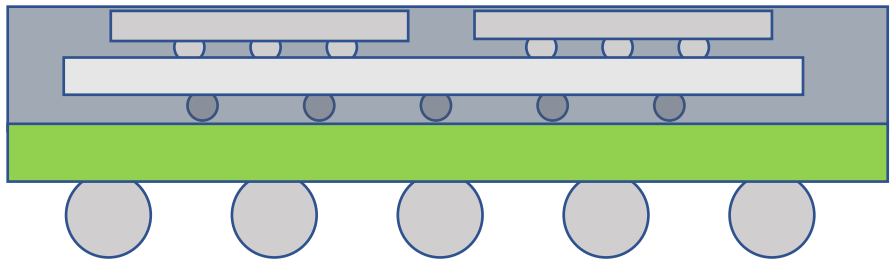
Die-to-Die Signaling

	Coarse Pitch Wiring (Organic)	Fine Pitch Wiring (Silicon/Organic?)
High Latency (High Bandwidth/wire)	SerDes PCIe USR/XSR • High Phy Energy/Bit (~6pJ) • Low Wire Count (~50) • Low Symbol Transition Current • Low Swing Differential • High Fundamental Frequency (~4-28 GHz)	
Low Latency (moderate Bandwidth/wire)	DDR BoW • Lower Phy Energy/Bit (~2pJ) • High Wire Count (~100) • Higher Symbol Tansition Current • Large Signal, Low Voltage Swing • Low Fundamental Frequency (~1-5GHz)	HBM/HBI AIB BoW • Low Phy Energy/Bit (~1pJ) • Highest Wire Count (~4000) • Highest Symbol Transition Current • Low Fundamental Frequency • PDN Issues (~1-5GHz)

Manufacturing and Testing

Testing for Heterogeneous Chips



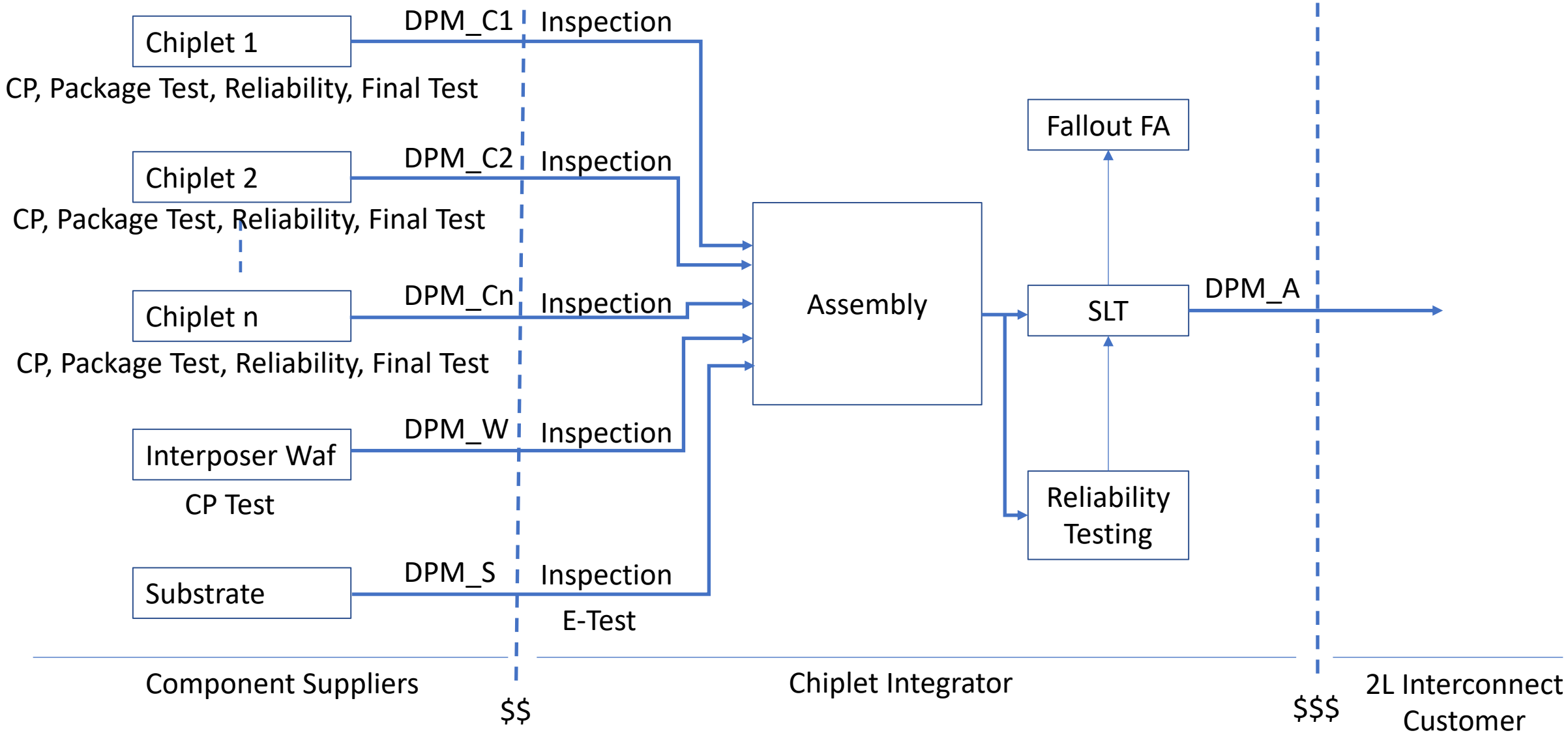


DFT & Verification:
- Need ESL (transaction level) and IBIS Models for all Chiplets
- Need Mechanical Models for all Chiplets for Thermal/Mech Simulations
- Simple JTAG in each Chiplet

Incoming Material:
- Visual Inspection
- Quality of Chiplets to be guaranteed by the Vendor
- E-test for substrate
- CP test for Si Interposer

After Assembly:
- Inspection (e.g. x-rays)
- System level testing to verify assembly process (JTAG needed)
- Reliability testing

Chiplet Integration Ops Flow



Anatomy of SLT

1- Find Assembly Defects

- Open/Short (validate the connectivity)
- Open/Short Repair

2- Validate System IDDQs

- Check Power Down IDDQs on all Chiplets
- Validate all IDDQ combos

3- Validate Functionality

- Load/Run SLT FW
- Test Bootup, Pairwise communication
- Outside connectivity Loop Backs. Eye scans.
- Run a bare minimum system function/customer app
- Test Mechanicals and Thermal

4- Save Program/Repair/FW/Keys

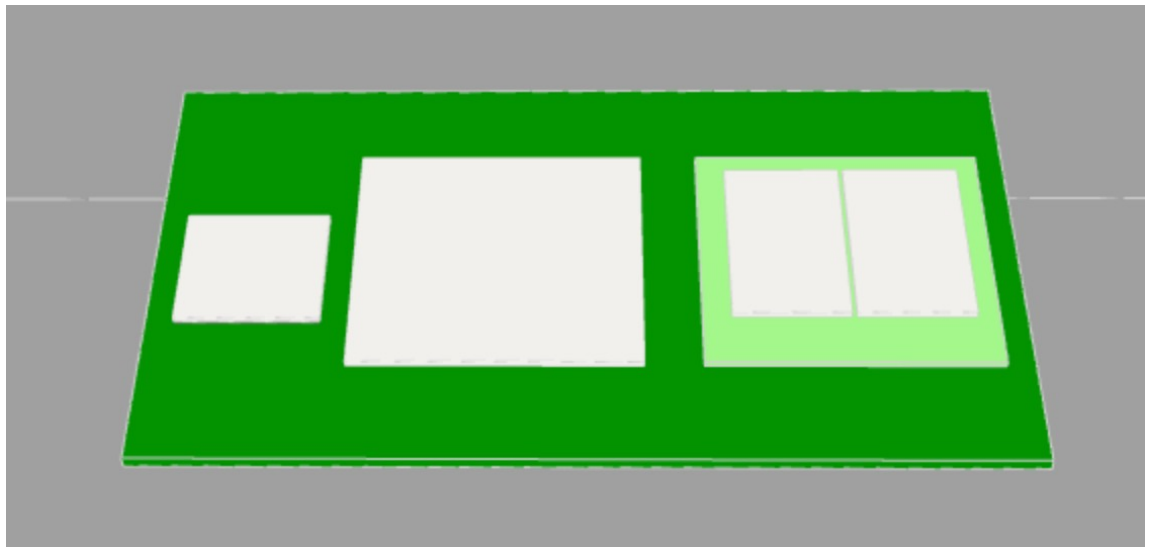
- Store data in the IC

Design For System Level Test (SLT)

EVT->DVT->PVT:
- Design for SLT in EVT Phase

Assembly Design:
- Design Open Short Testing BIST
- Simulate the system for open shorts. Identify sensitivities for Test Engineering.

System Design:
- Add JTAG to every component
- Add instrumentation circuits (Imon, Eyescan…)



Develop Bench Test FW in EVT:
- Precursor to SLT FW and Automation
- Test Bootup, Pairwise communication
- Outside connectivity Loop Backs
- Run a bare minimum system function

Power Delivery Network Design:
- Design for systematic Power Down and Power Up for Test Engineering

D2D and External IO:
- Design for pairwise chiplet test
- Design for external loopbacks (SerDes/RF)

Summary

1. Chiplets
   - Physical Goods. Testable. With Warranty.
   - Early-stage architecture across EE, ME, Packaging Eng, and Material Science is key.
   - MCM -> 2.5D -> Si Bridges -> Si Interposers -> Front End Fab Chiplet based 3D-ICs.
   - Chiplet Models are machine readable and different from Chip Data Sheets.

2. Design of Heterogeneous ICs
   - Early Power Estimation drives packaging technology choice.
   - Early Power Estimation helps with Thermal and Mechanical analyses and wise choices.
   - Clean power delivery requires thicker Cu layers and adequate decoupling.
   - Large and small signal D2D signaling requires capacitances reduction and smooth surfaces.

3. Operations and Test
   - System Level Test, System Level Test, System Level Test.
   - Yield is workable IFF design has no pair-wise bugs, cross talk, sensitivities.
   - Work out ELF in Chiplets and not after integration.

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