Road to Chiplets: Architecture

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Why Chiplets?

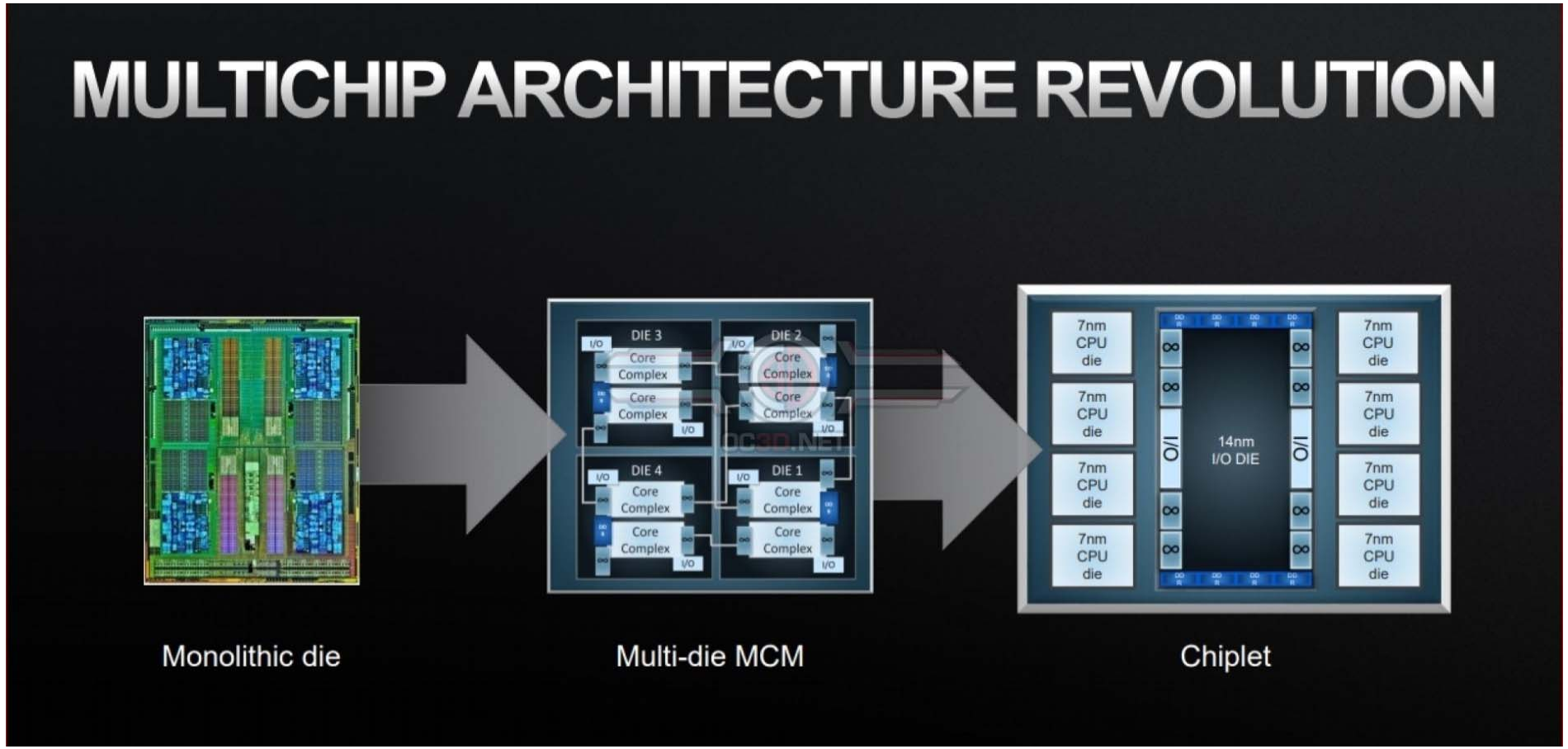
- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

E. Jan Vardaman, President and Founder

TechSearch INTERNATIONAL

New Era of Semiconductor Packaging

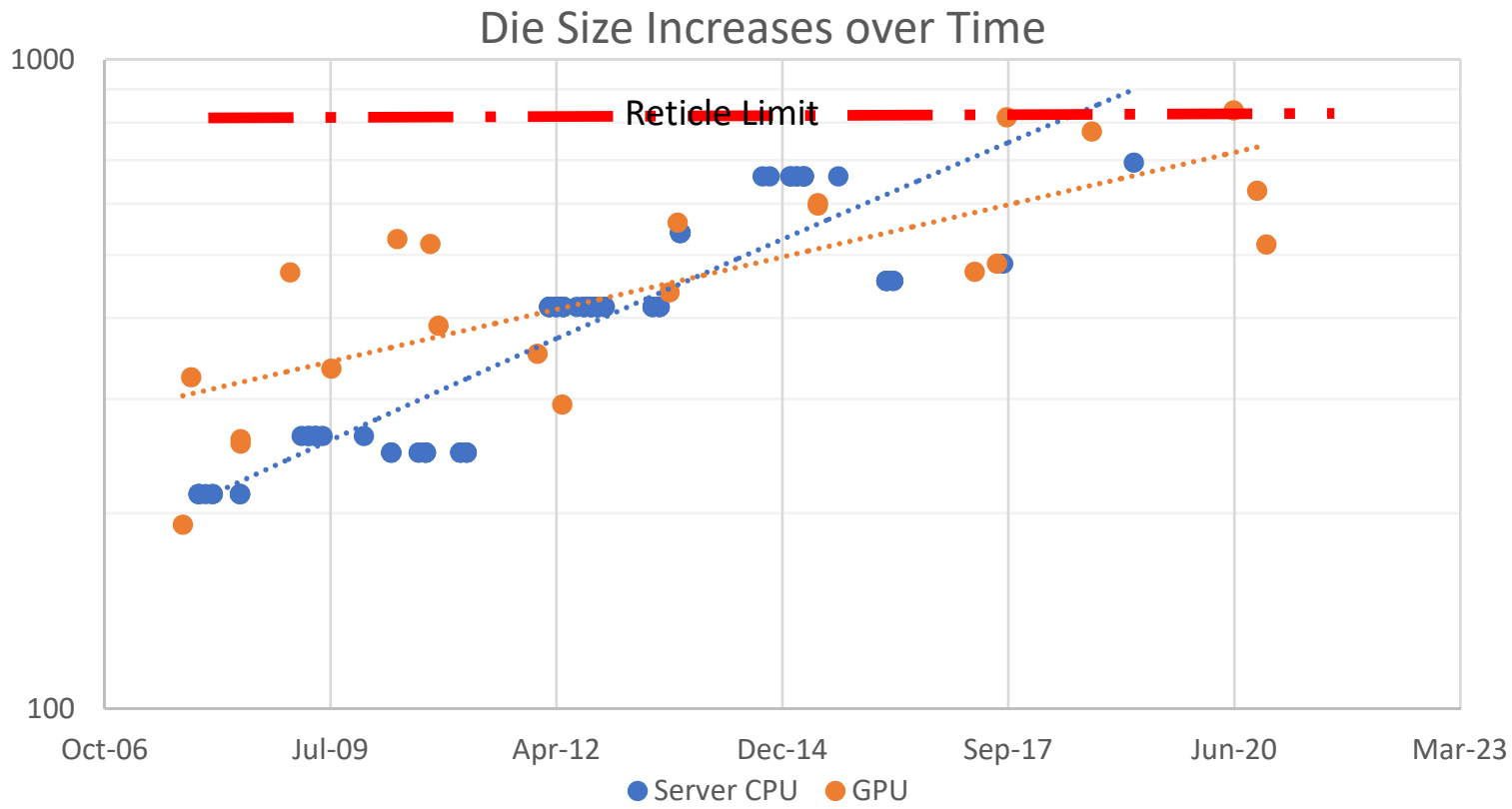


Source: Overclock3d.net.

- **Chiplets will be a key enabler for next 10-20 years (to quote from TSMC's Doug Yu)**

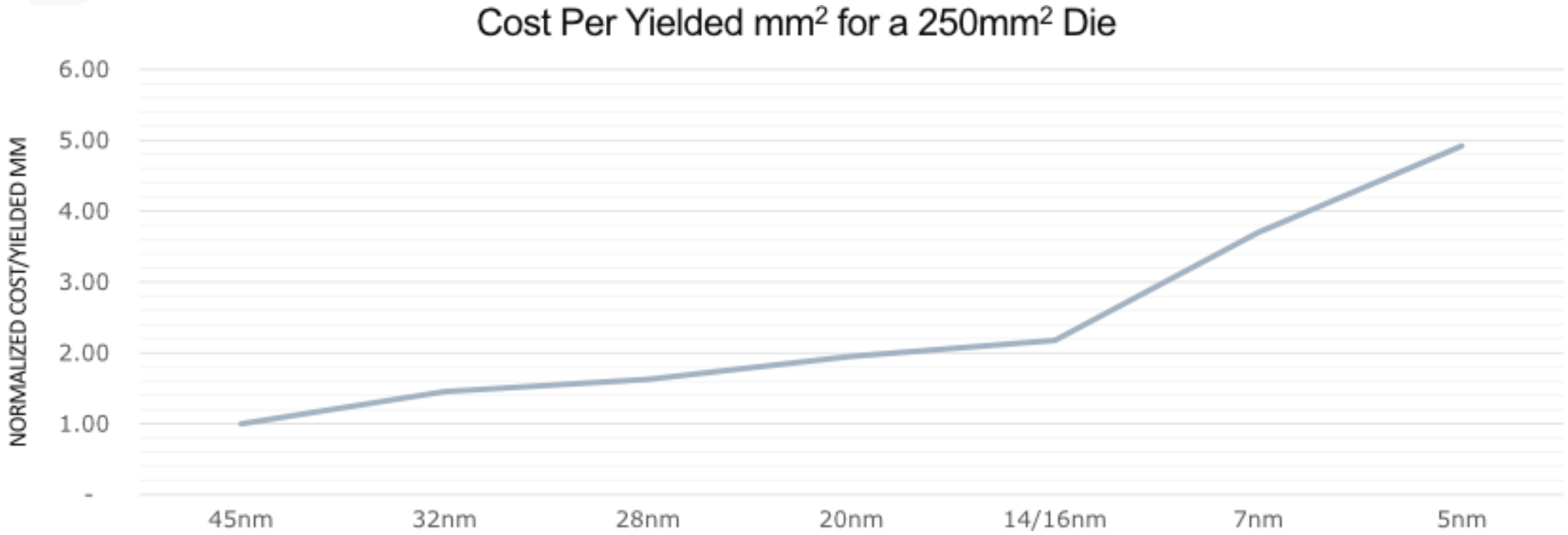
Die Size Growth: Major Driver for Adoption of Chiplets

- **Die sizes continued to increase over time for server CPU and GPU**
- **Performance requires more transistors, but industry needs a new, more economical approach**



Source: AMD internal analysis.

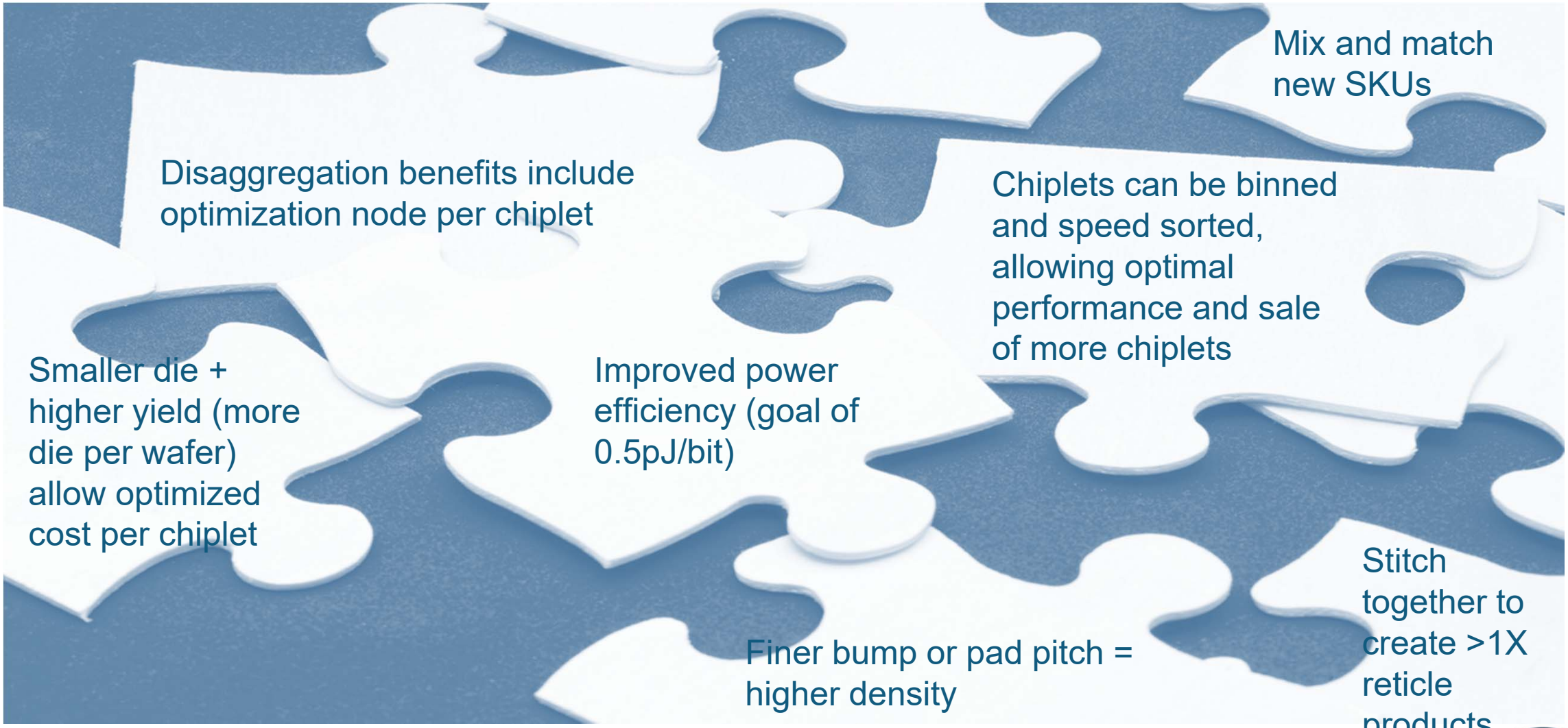
Cost of Fabricating a Large Die Continues to Increase



Source: AMD internal analysis.

- **As companies move into <7nm semiconductor nodes, the cost to fabricated a large die becomes uneconomical**
- **The industry needs a new approach to achieve the economics previously achieved with scaling**

Drivers for Chiplet Adoption

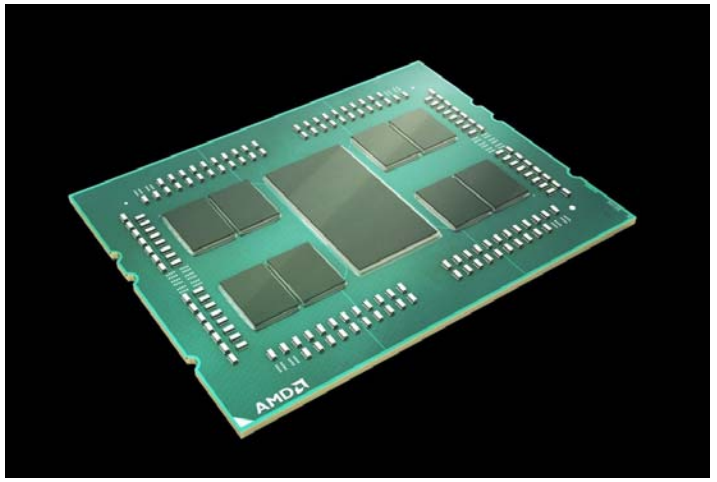


How Do We Define Chiplets?

- **A chiplet is an integrated circuit block specifically designed to work with other chiplets to form a larger more complex system that often makes use of reusable IP blocks**
  - A chiplet can be created by partitioning a die into functions that are more cost effectively fabricated (smaller die, higher yield, and less advanced nodes)
  - A chiplet is a hard IP block
  - Functions with other chiplets, so design must be co-optimized and silicon cannot be designed in isolation
  - Made possible by communication using chiplet interface (proprietary today)
- **Differs from SiP or traditional MCM in that it is a new design, not just a combination of different "off-the-shelf" chips**
- **Chiplet is not the package, it's the design philosophy**
  - Change from "silicon centric thinking" to "system-level planning" and "co-design of IC and package"
  - The industry has to think about chip design in a new way
  - Same impact as when the industry moved from a peripheral chip layout to area array!

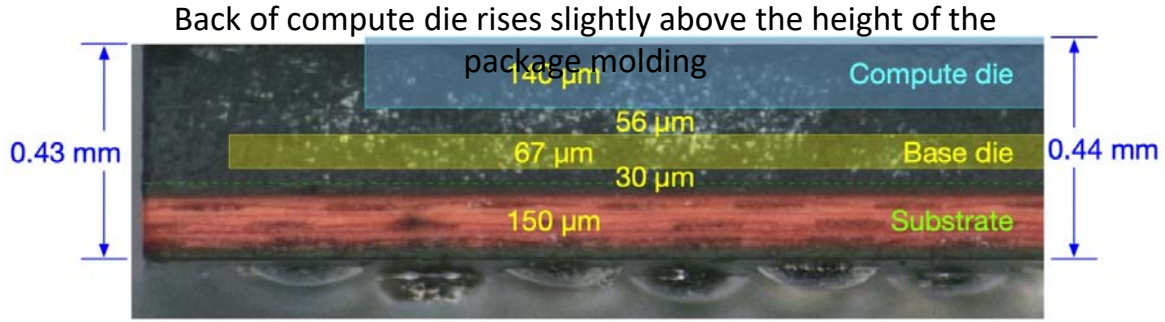
What is A Chiplet Package?

- **Many package options "no one size fits all"**
  - Organic substrate, including an embedded bridge
  - Silicon interposer
  - Fan-out on Substrate or RDL interposer
  - 3D configurations with µbumps or hybrid direct bonding



Source: Wired.com.

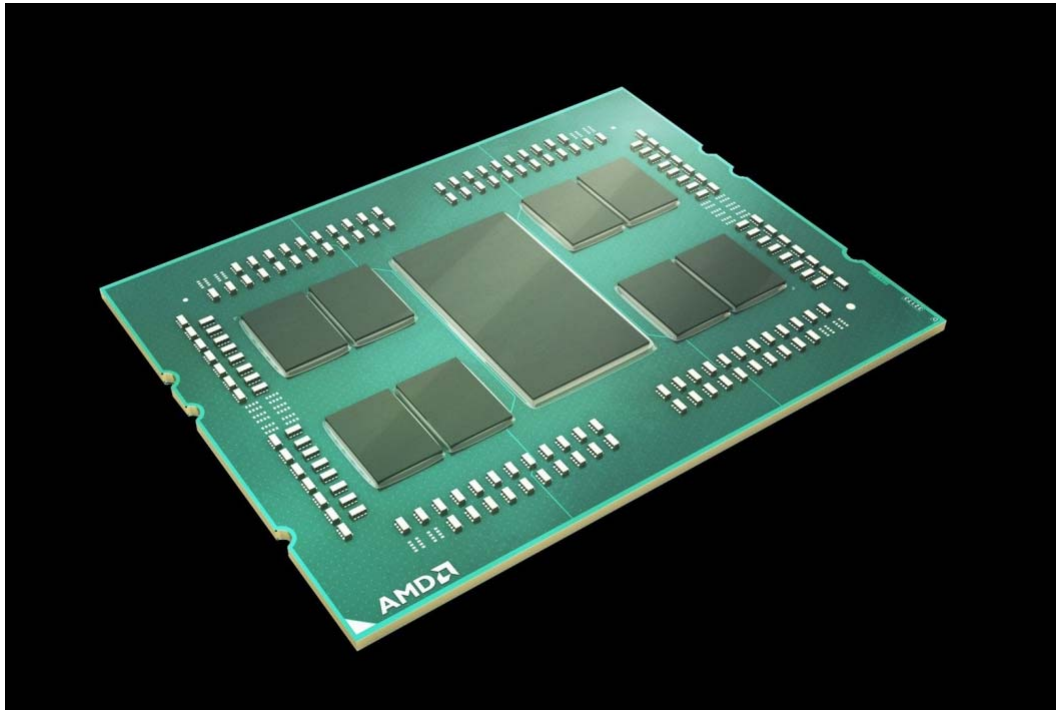
Source: Xilinx.



Source: TechSearch International, Inc. teardown.

AMD Multiple Chiplet Product Introductions

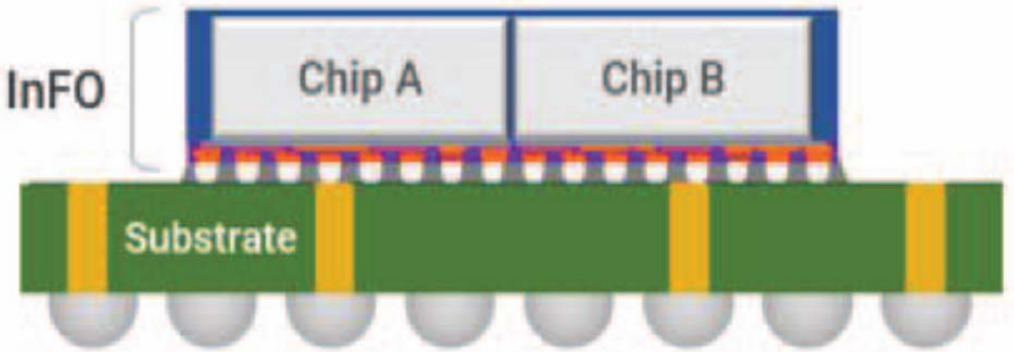
- **Multiple generations of desktop and server products using chiplets with organic substrate**
  - Split out analog functions from advanced 7nm logic
  - Chiplets can be binned and speed-sorted before assembly on the substrate
  - Better memory access
  - Minimize local latency
  - 1, 2, 4 or 8 CPU chiplets plus an I/O chiplet are attached to an organic interposer

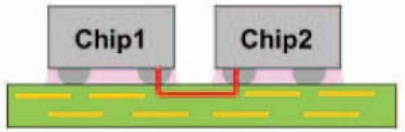
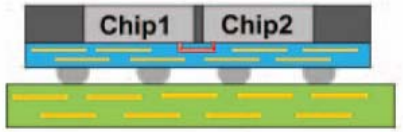


Source: Wired.com.

TSMC InFO_oS for Chiplets

- **TSMC has proposed the use of its InFO process as a chiplet packaging solution targeted at AI, networking, & edge computing**
- **Alternative to the laminate MCM package for chiplets**
- **Demonstration of 2.5x reticle of fan-out (51mm x 42mm) on a 110mm x 110mm substrate**
  - 5 RDLs (4 with 2/2µm 1 with 5/5 µm)
  - D2D I/O pitch 36 µm

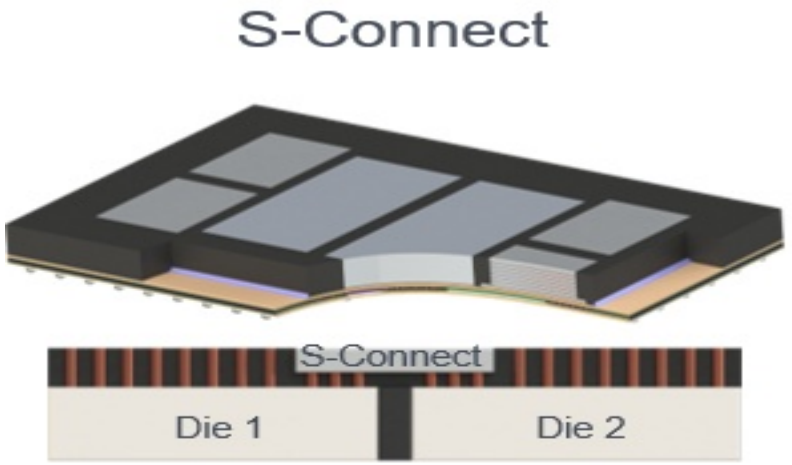


Technology	MCM	InFO_oS
Structure		
Min. Line W/S	15/15 um	2/2 um
Line counts/mm	34	250
BW/mm	1x	7.3x

Source: TSMC.

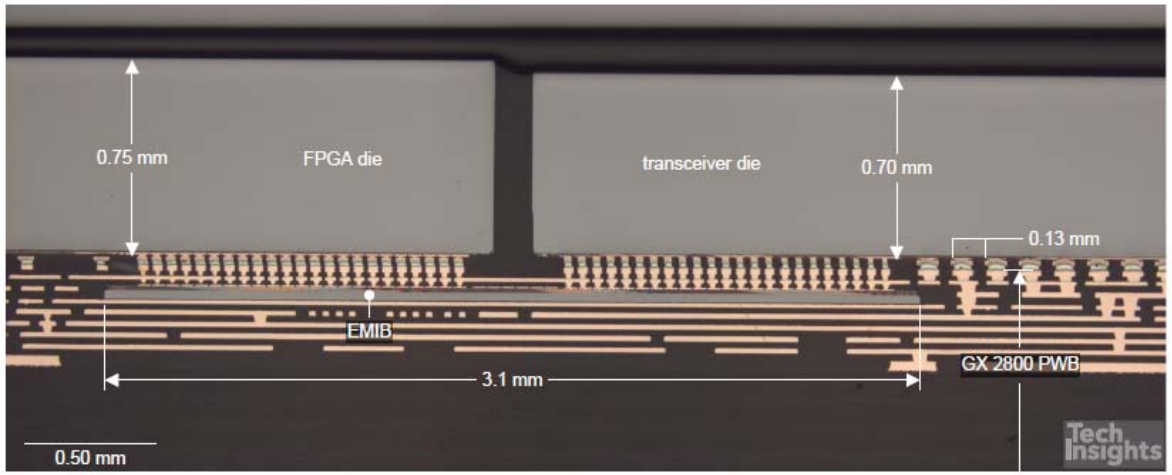
Fan-Out and/or Embedded Bridge Solutions for Chiplets

- **Many companies with embedded bridge solutions or FO solutions**
  - Amkor
  - ASE
  - IBM
  - Intel
  - SPIL
  - TSMC

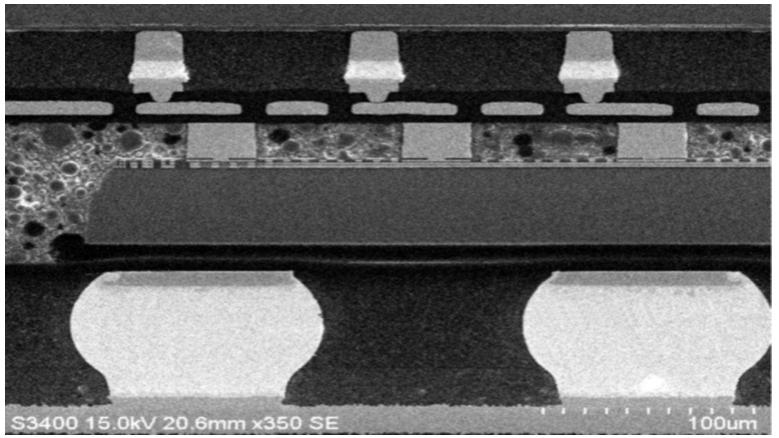


Source: Amkor Technology

Intel's Embedded Multi-die Interconnect Bridge (EMIB)



Source: TechInsights.

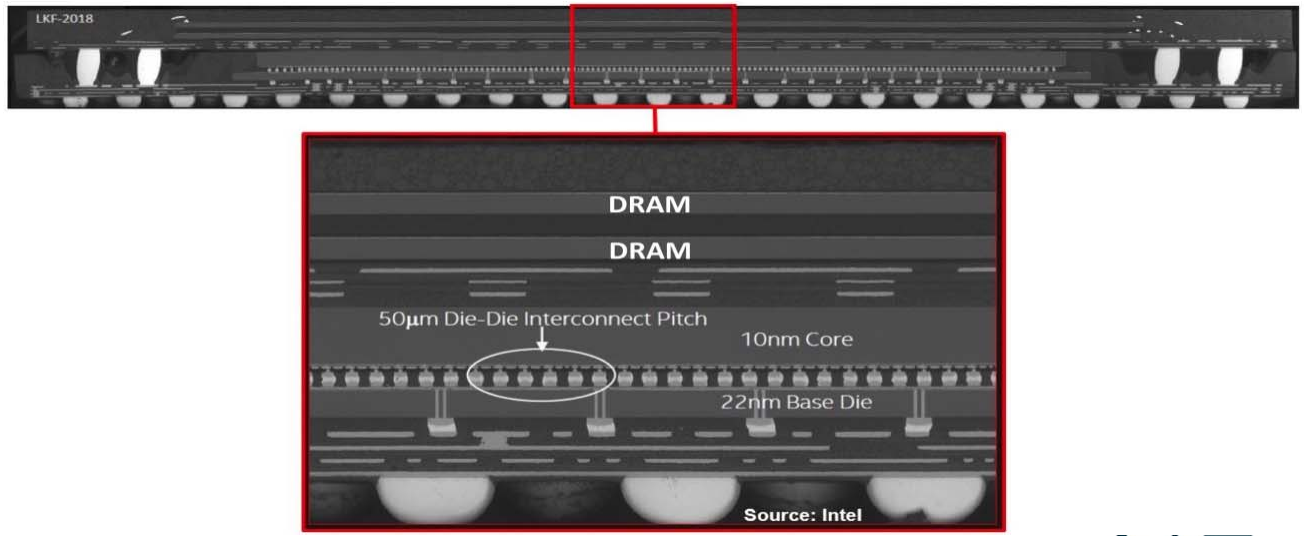


Source: ASE.

Intel Foveros Technology

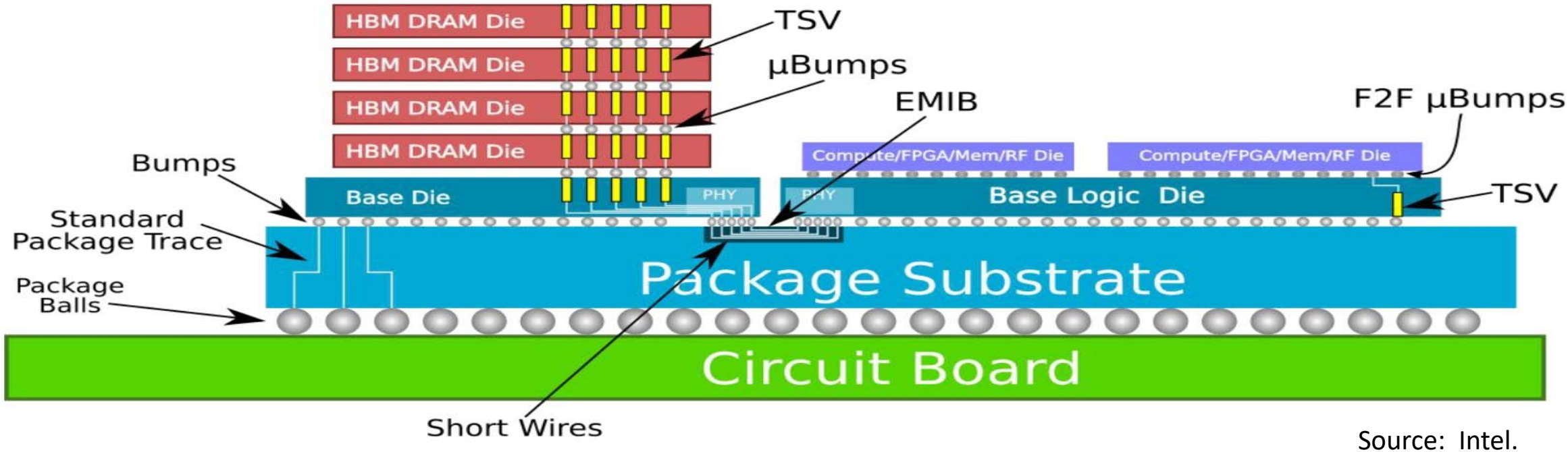
- **Intel's Foveros technology die are stacked in 3D**
  - Base die, using less advanced node, can include power management features, voltage regulators, DC/DC converters
- **Benefits include**
  - Reduced voltage drop
  - Power efficiency
  - More immediate power delivery to the CPU cores
  - Elimination of passives on substrate
  - System-wide communication across multiple chiplets/dice vs. the limited die-to-die communication capability enabled by passive Si interposers
- **Used in the Samsung Galaxy Note S (Mobile PC)**
  - Longer lasting battery
  - No fan
  - Very thin package, allows thin product

Intel's Lakefield CPU
- 10nm CPU
- 22nm Active Si Interposer



Source: Intel.

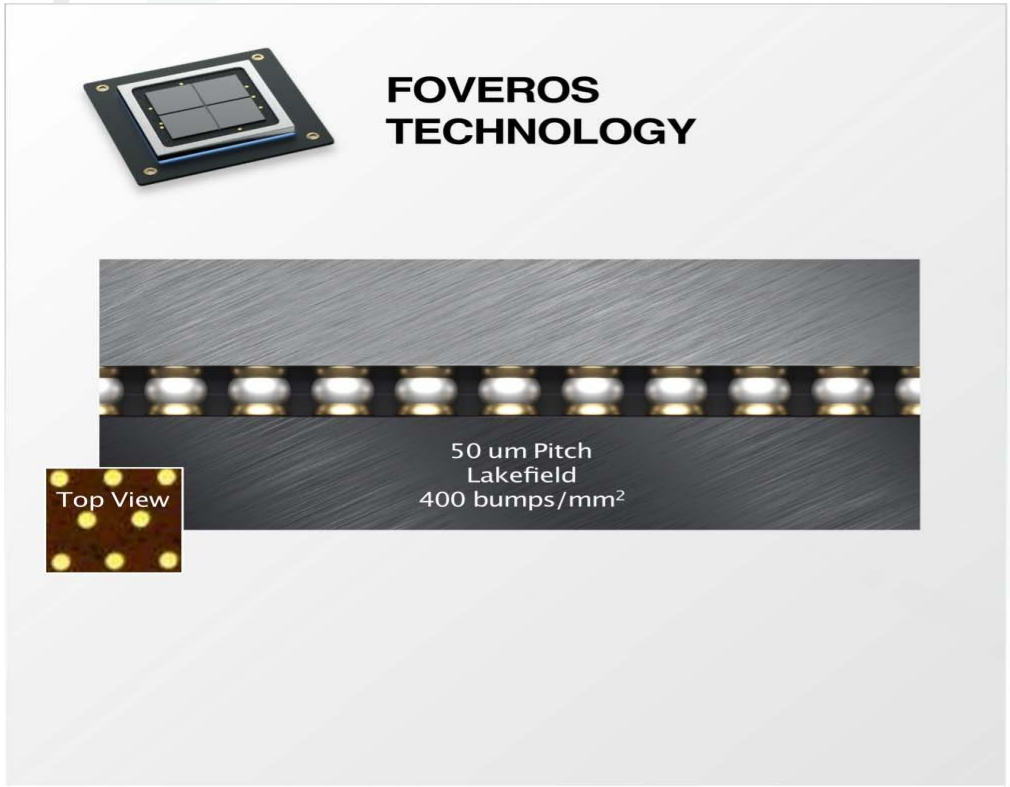
Intel Co-EMIB (EMIB + Foveros)

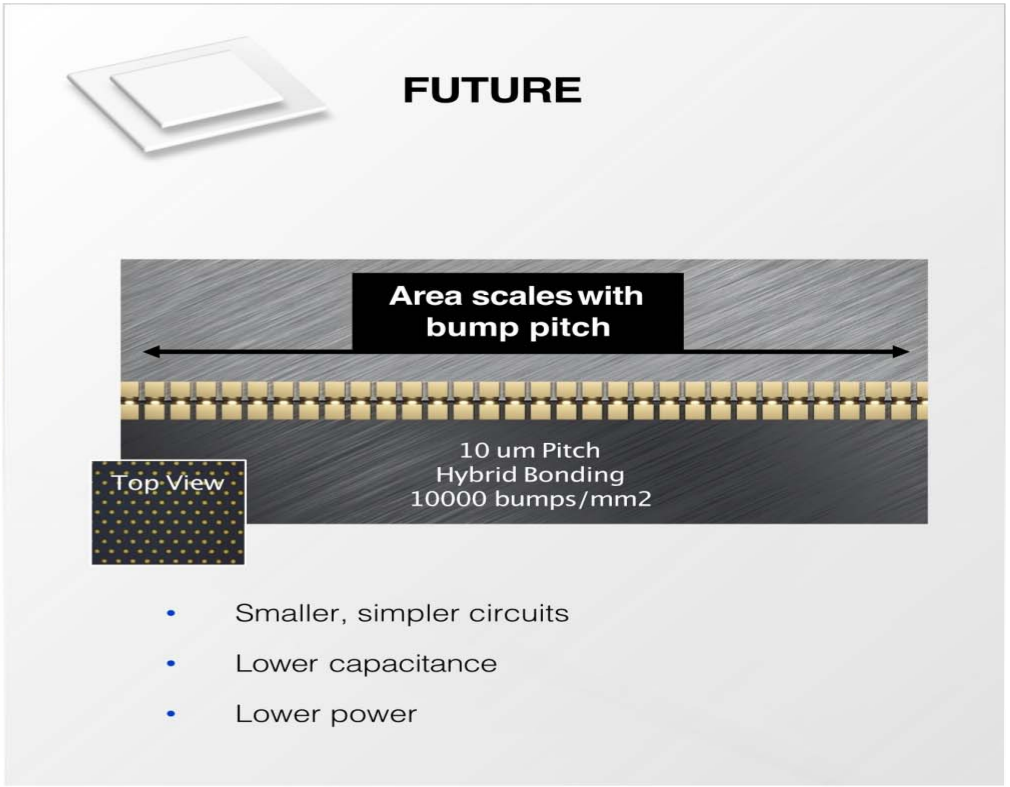


Source: Intel.

- **EMIB and Foveros can be combined to provide a high-density solution**
  - Connecting HBM and logic with silicon bridge embedded in laminate substrate
  - Foveros used to connect chiplets (Intel calls tiles)
- **Will be used for Intel's upcoming datacenter GPU**

Hybrid Bonding

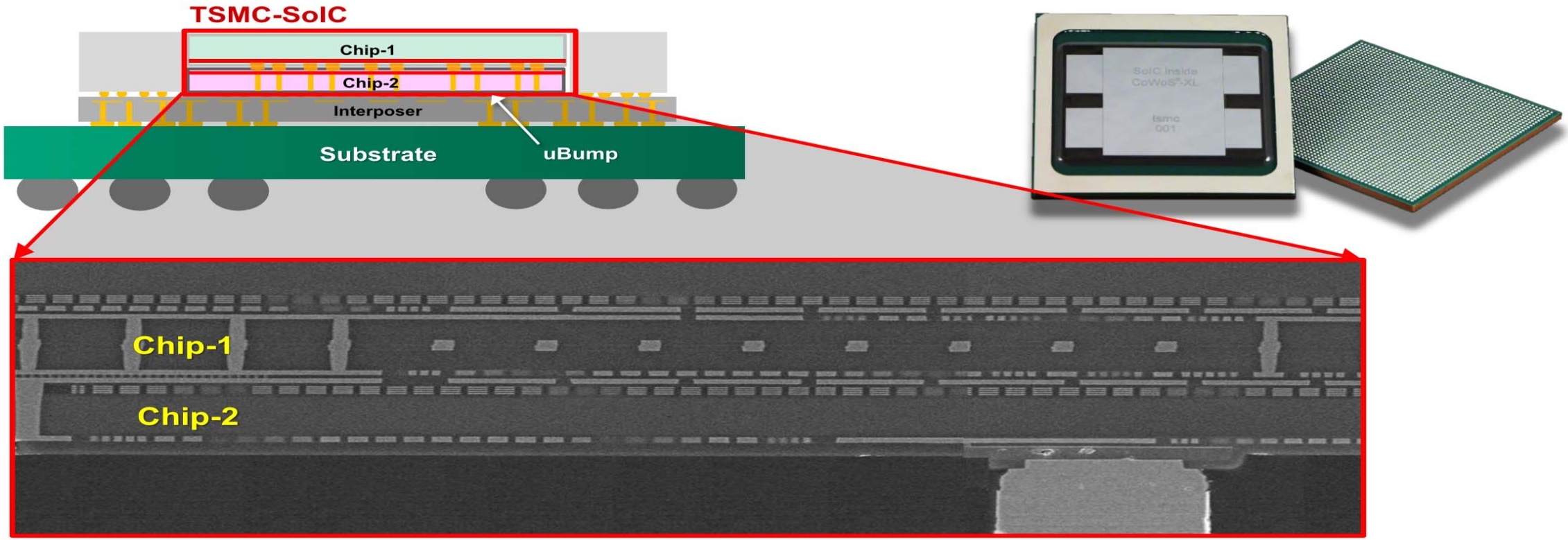




Source: Intel.

- **No solder interconnect**
- **Finer pad pitch joining is possible**
- **Requires clean surface (no particles), clean environment**

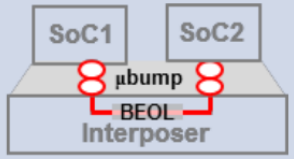
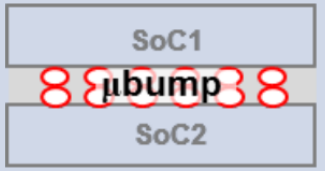
TSMC-SoIC™ + CoWoS® for HPC Applications



Source: TSMC.

- SoIC can be attached to a silicon interposer
- SoIC can be used to stack 4, 8, or 12 high chips with a total height of 600 µm

SoIC™ Compared to 2.5D and 3D IC

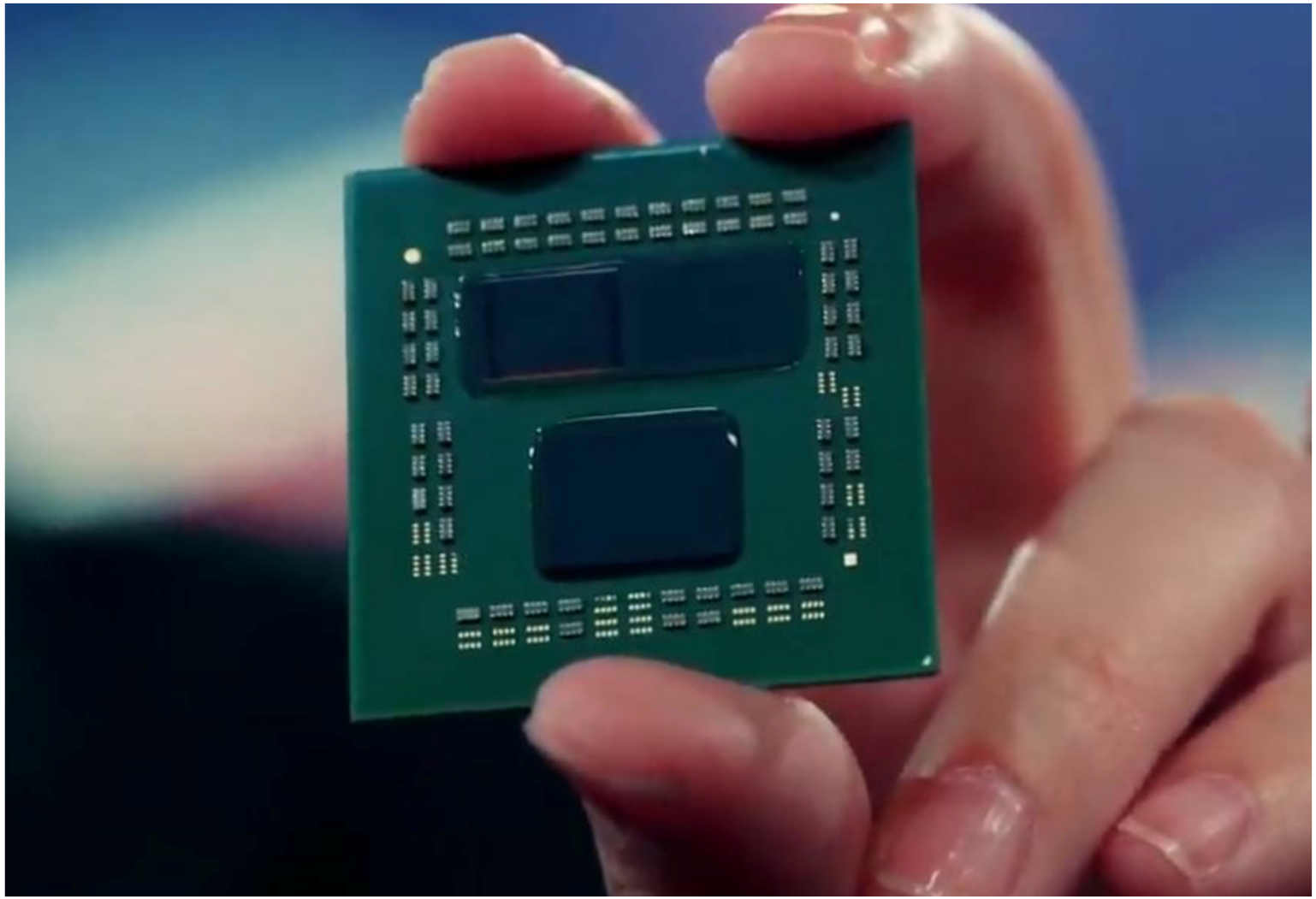
Technology	2.5D	3D-IC	SoIC
Structure cross-section			
Interconnect	µbump + BEOL	µbump	SoIC bond
Chip Distance	**~100 µm**	**~30 µm**	**0**
Bond-pad Pitch	**36µm (1.0X)**	**36µm (1.0X)**	**9µm (0.25X)**
Speed	0.01X	1.0X	**11.9X**
Bandwidth Density	0.01X	1.0X	**191.0X**
Power Efficiency (Energy/bit)	22.9X	1.0X	**0.05X**

Source: TSMC.

- **With SoIC there is virtually no distance between integrated chips, and a very small bond-pad pitch of 9 µm provides good scalability**
- **Using a bumpless bonding process is critical to improvements in performance, power, resistance, and capacitance (lower inductance and thermal resistance)**

AMD's 3D Chiplet

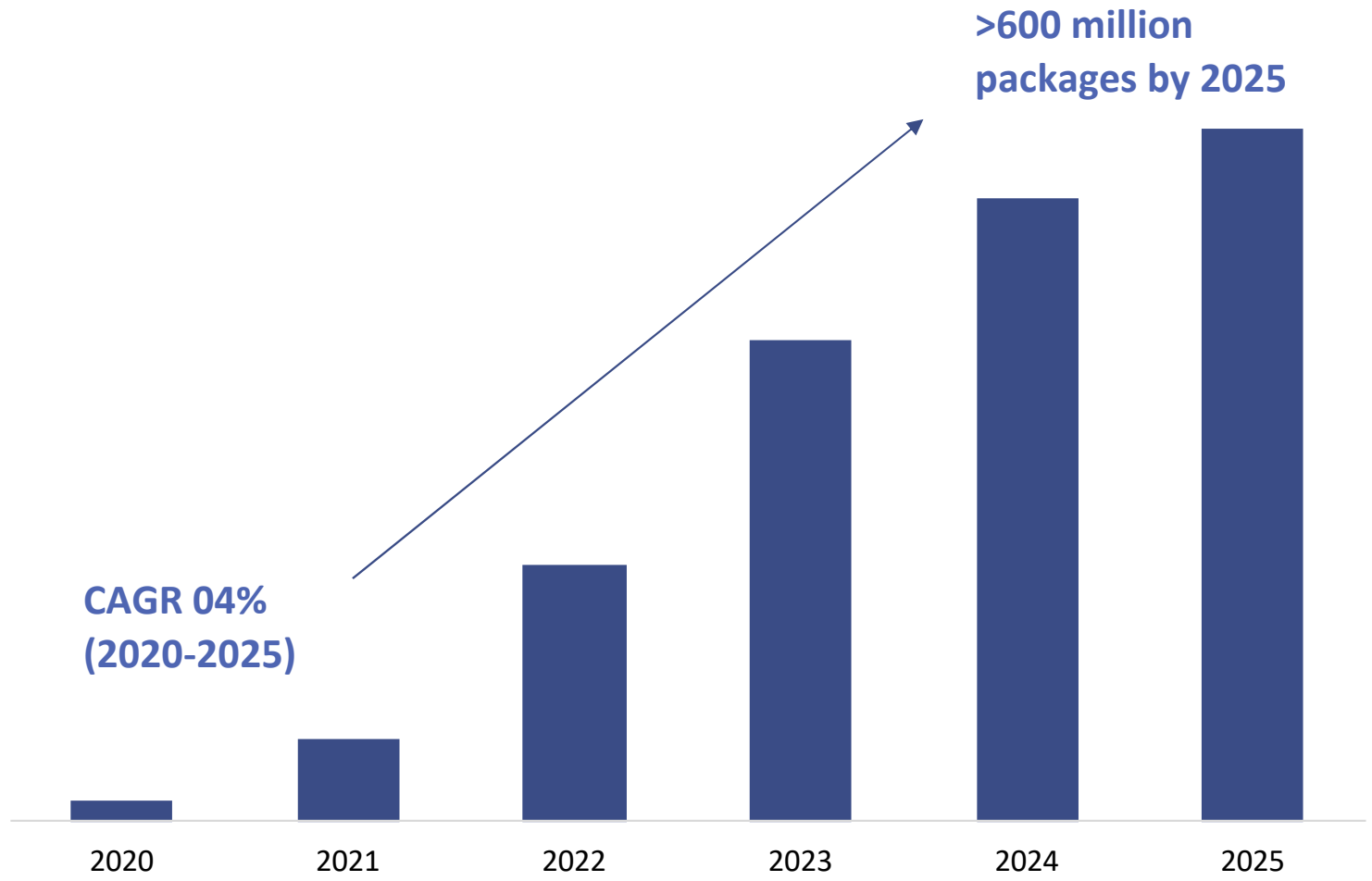
- **AMD's Prototype 9 5900X chip for gaming**
  - Gaming performance improvement
- **Same 7nm node as Ryzen, but performance gains using chiplet design and 3D copper-to-copper hybrid bond**



Source: AMD.

We Are at the Beginning of Our Journey

- Applications today include server, desktop laptop, networking, AI
- Devices such as GPU, CPU, FPGA
- Future applications expected to include tablets and smartphones
- Introduction of third party IP block providers and standard interfaces potential to broad the market



Source: TechSearch International, Inc.

Thank you!

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