Road to Chiplets: Architecture

July 13 & 14, 2021

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Chiplets: Building Blocks and Future Packaging Trends

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Agenda

1. High Level Trends
2. What is a Chiplet?
3. Chiplet Motivation
4. Packaging Technologies for Chiplet-based Products

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Market Driver and Trends

June 2021

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High Performance Product and Packaging Trends

Power

Higher memory BW
at **low power**

- Memory co-located in package or on chip (data locality)

High wafer costs
Higher I/O count

- **Chiplets:** Use N node sparingly, keep some portion in N-1 node (e.g., I/O blocks)

Better PDN required

- Ultra low ESR caps, IPDs, VRMs (Voltage Regulator Modules)

Increasing dissipated power

- Improve thermal power dissipation solution for the package

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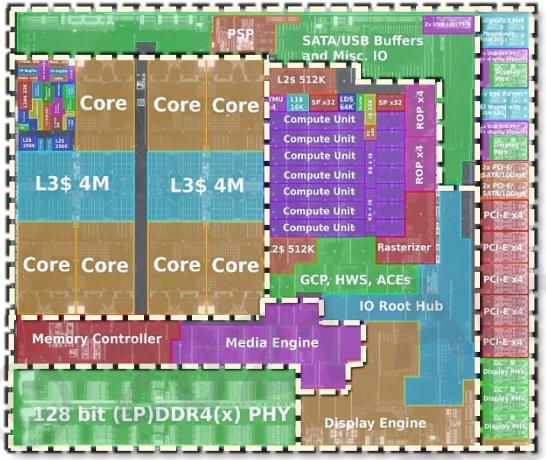
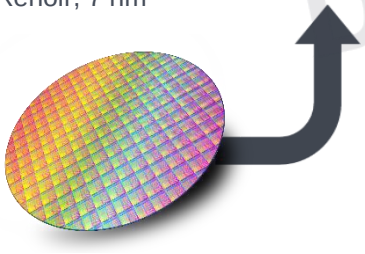
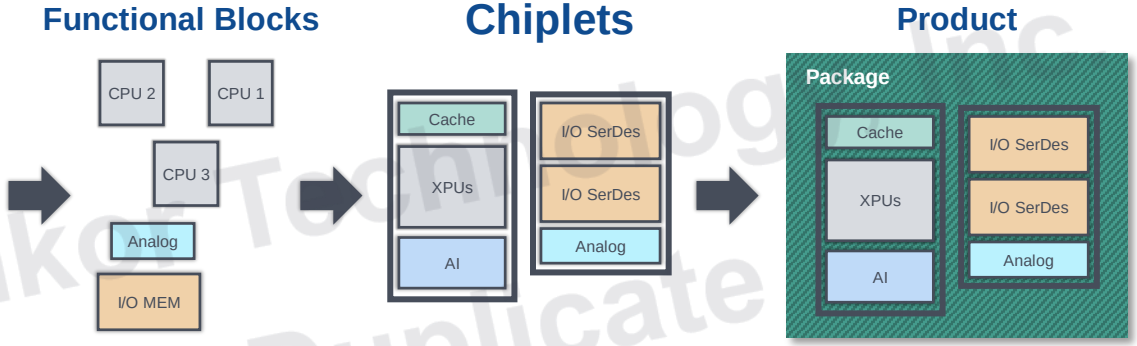
What are Chiplets?



*AMD Renoir, 7 nm





- Functional blocks are combined and partitioned into chiplets
- Chiplets are combined in the IC package to create the final product

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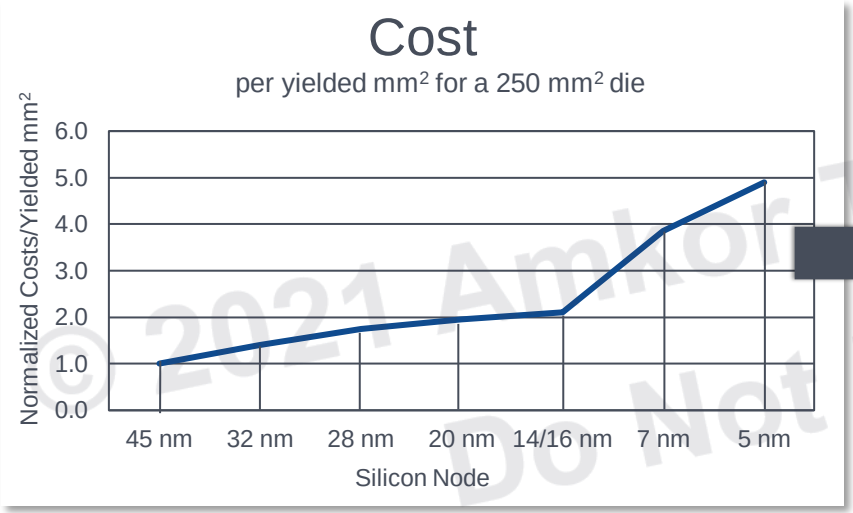
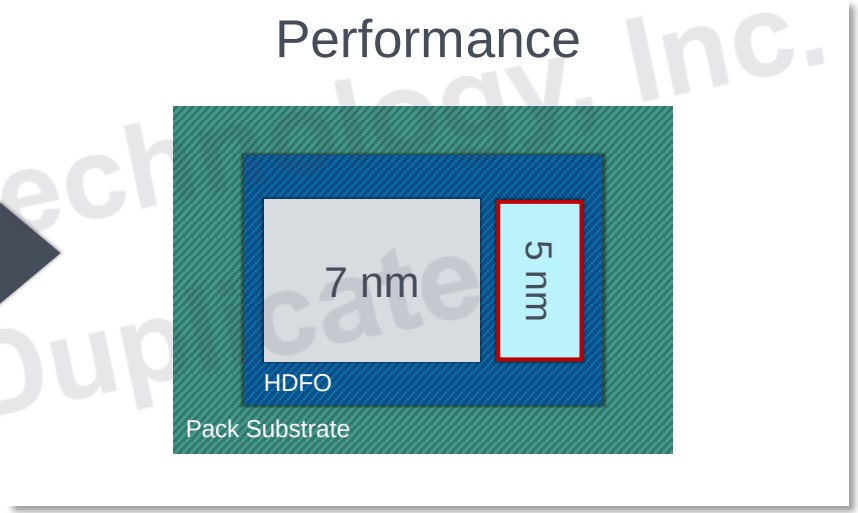
Why Chiplets?





- Lower the total silicon cost
- Use latest Si node sparingly

- IC package-level integration enables same or greater performance
- Lower total product cost than SOC

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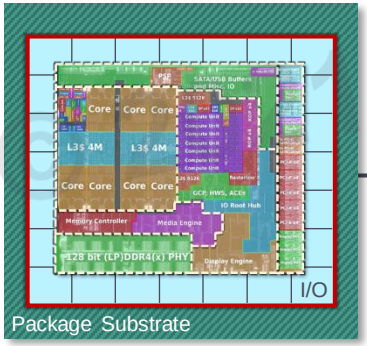
From SOC to Chiplets → Different Paths

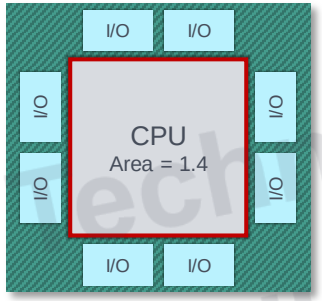
Single Die FCBGA



Data Center
CPU/Server

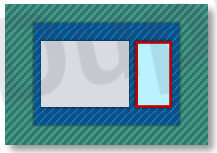
PC Notebooks
CPU

5G
Processor



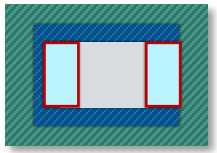
MCM

CPU + I/O Chiplets
128 I/O



HDFO

CPU + I/O Chiplets
860 I/O



HDFO

Logic + RF Chiplets
550 I/O

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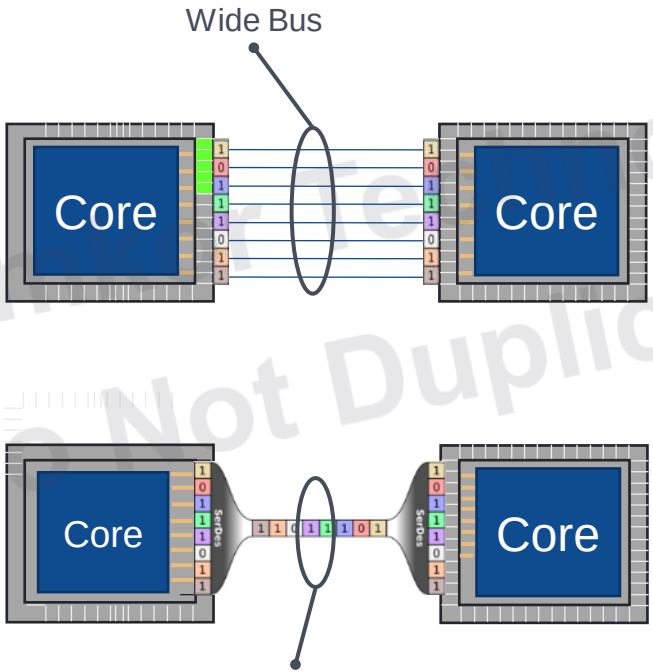
Die-to-Die Interface: Package Differentiation

- Parallel interfaces
  - More physical wires
  - **Lower latency**
  - Lower power



- Module based
  - One physical wire/bit
  - Each I/O driver is small
  - High density routing
    - HDFO
    - 2.5D TSV

- Serial interfaces
  - Fewer physical wires
  - Higher latency
  - Higher power

- MCM
  - Many bits per wire pair
  - Large I/O driver area

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Chiplets and Heterogeneous Integration

Wafer Costs

Design Costs

Power Increases

IP Reuse

TTM

Better Power Dissip.

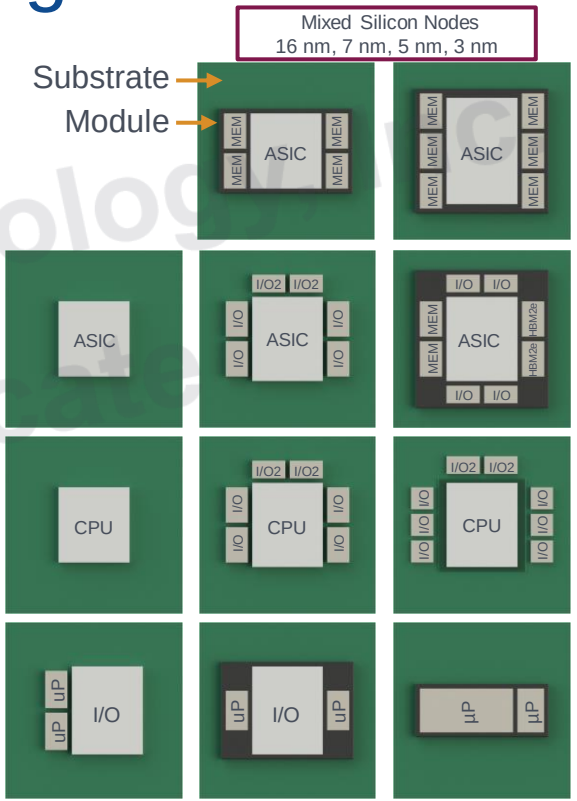
Better PDN

Deep Learning/AI Training
- Memory BW
- Lower power

NW Switch/Router
- Increase I/O count
- More gates

CPU, Server
- Address more DRAM
- Client PC

PC CPU/GPU
- Lower cost



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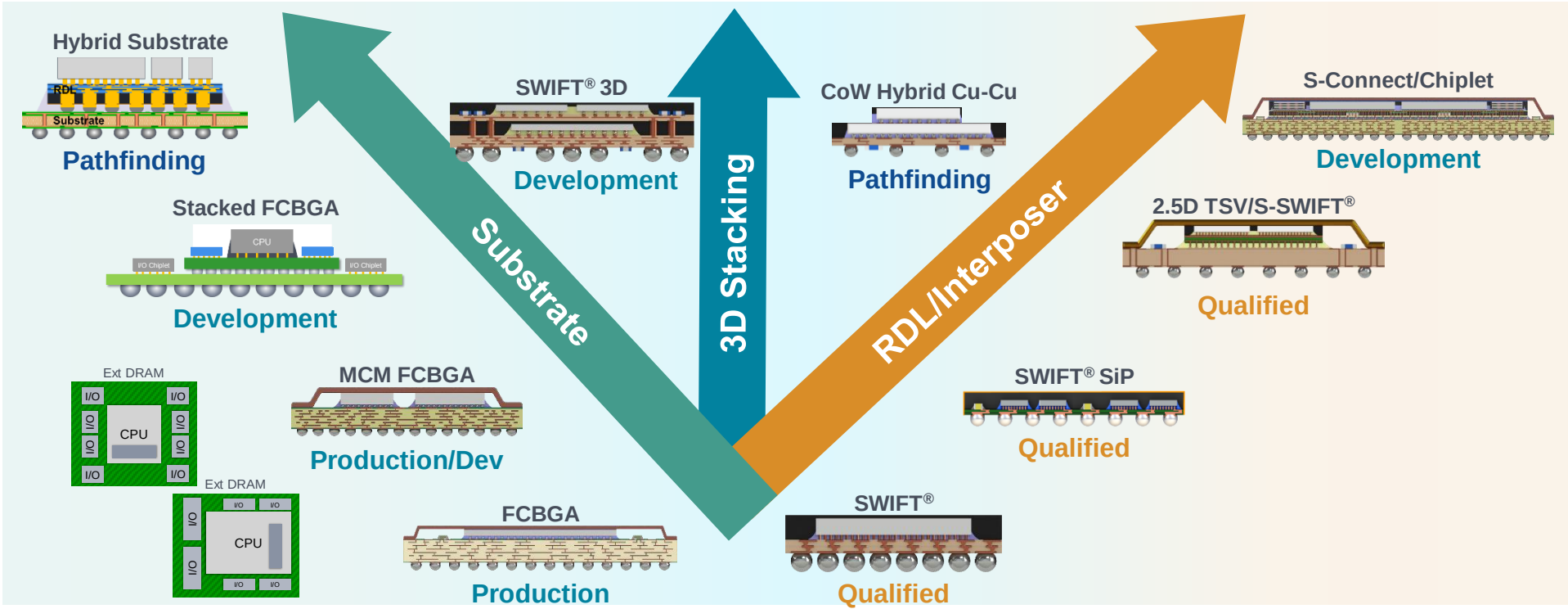
Chiplet Integration Path



High-Density MCM

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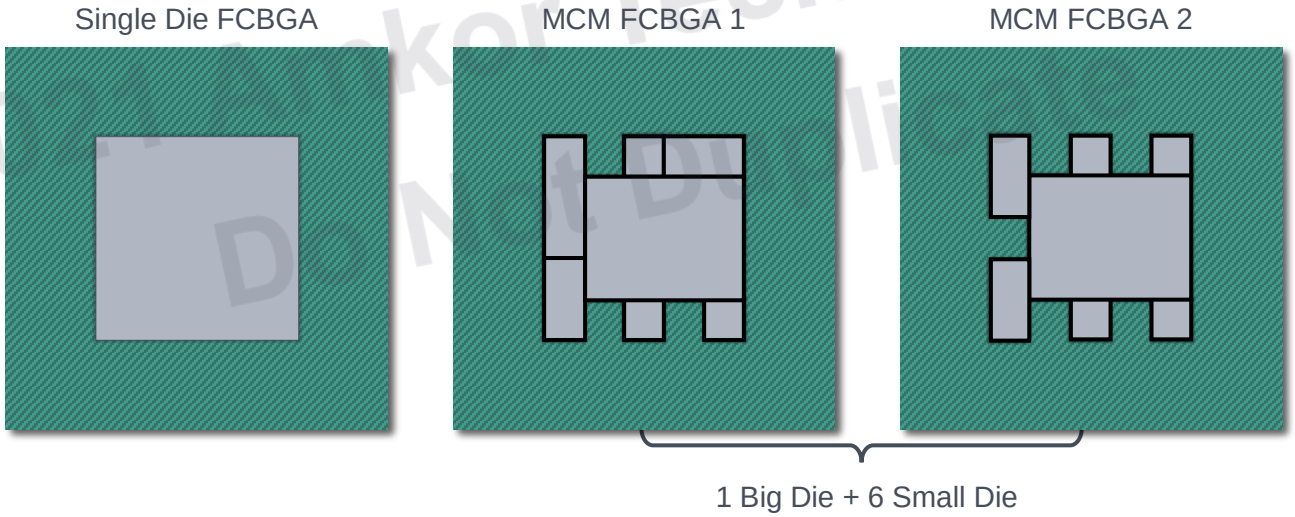
Test Vehicle

- In this device design a 32 x 32 mm die size was used with full array bumps at 165 µm pitch
- Same substrate was used for both single die & MCM study. Layout detailed below
- **70 µm die-die spacing**



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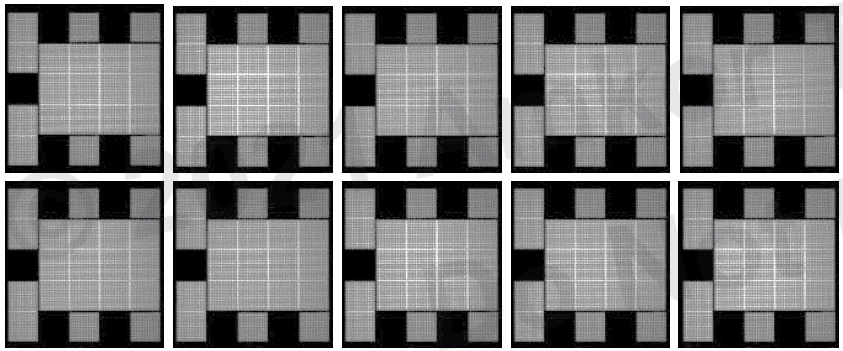
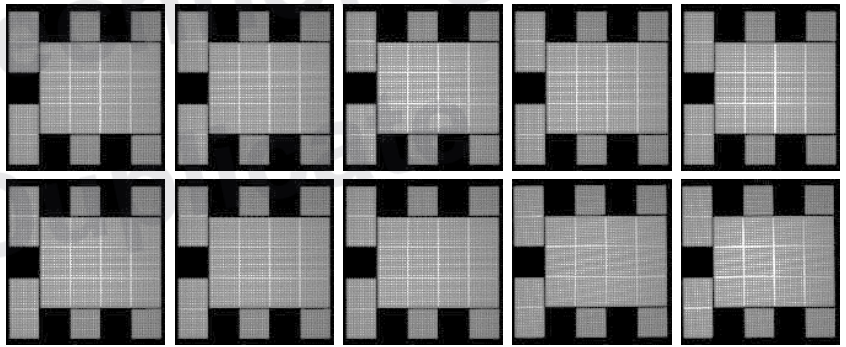
Development Results Summary: Reliability

- TCB 1,000x result
  - Found no UF abnormality



Leg 1: Individual side dispensing



Leg 2: One side dispensing

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High-Density MCM

- Engineering feasibility completed
- UF dispense and cure demonstrated: Void-free
- Reliability (TCB only) demonstrated: No abnormality on both individual and single side dispensing
- Ready for customer prototyping

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High-Density Fan-Out (HDFO) (S-SWIFT®)

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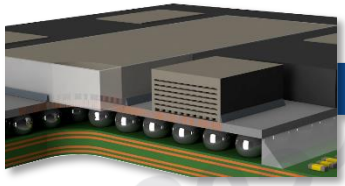
High-Density Fan-Out Evolution

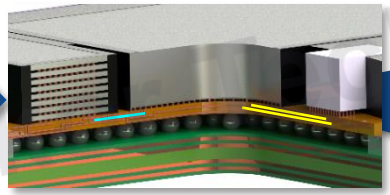
2.5D TSV



RDL Interposer

- Mostly logic + HBM2/2E

HDFO on substrate

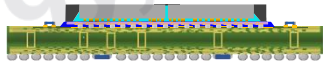


- Logic + HBM2/2E/3
- I/O die chiplets

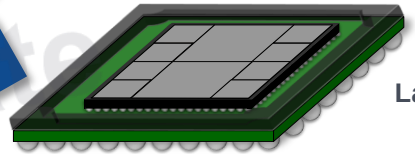
Smaller with cost emphasis
Large with more integration

Diversification

More Diversification



Small



Large

- **Cost emphasis**
  - Lower layer count
  - Die first and die last
- **Module size → 3x reticle area**
  - Better PDN solutions

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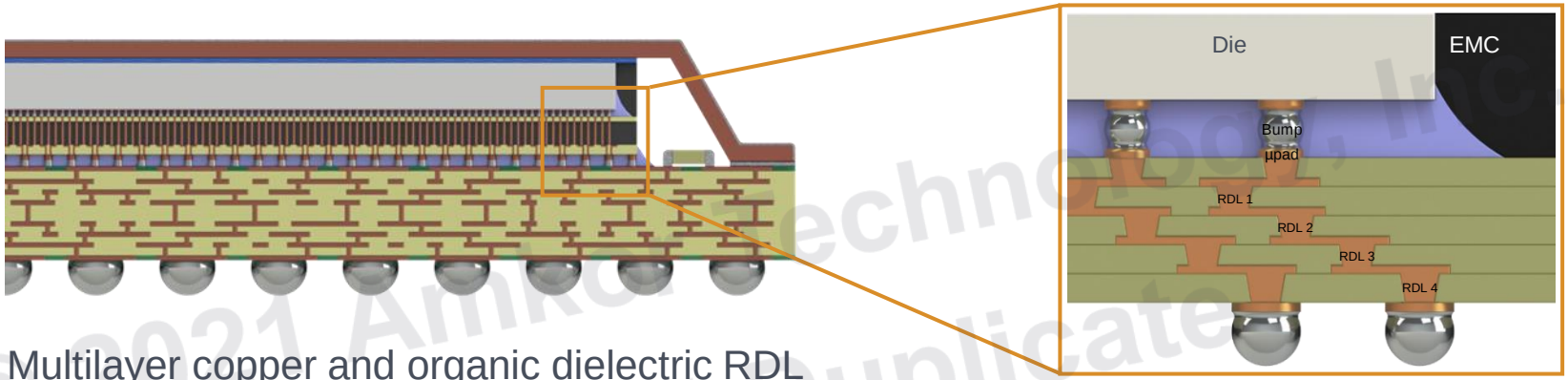
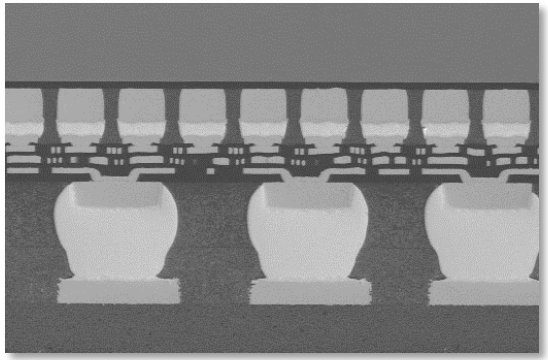
Substrate SWIFT® (S-SWIFT®)



- Multilayer copper and organic dielectric RDL
- 2 µm line/space capability, 2-**6** layers
- Excellent electrical properties
- Flexible solution
  - Fine pitch support for L1 down to 40 µm pitch
  - Plated Cu pillar or LF solder for L2 bumps



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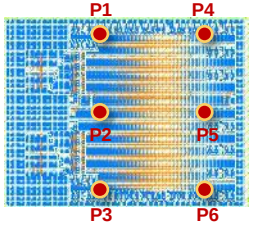
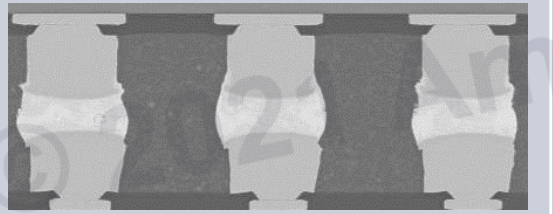
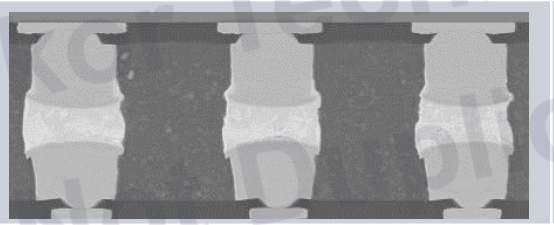
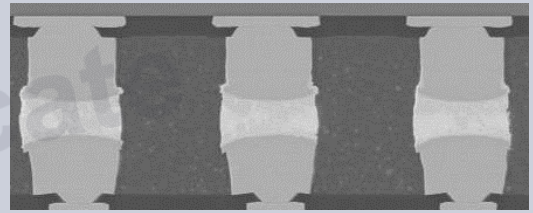
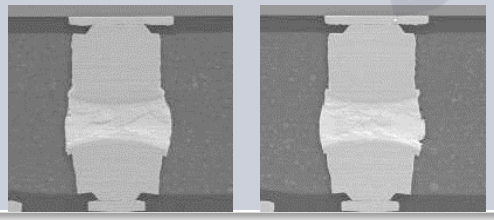
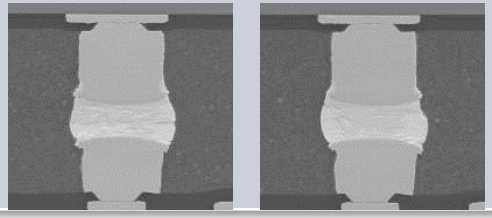
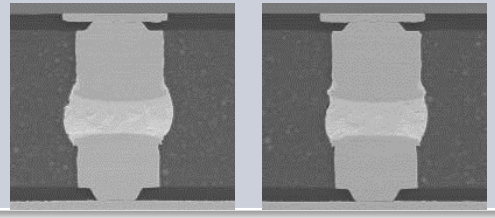
Cross Section Analysis – TCG 1000x



- HBM µbump joint analysis
  - No abnormality was observed

P1 (Left Top)	P2 (Left)	P3 (Left Bottom)
		
P4 (Right Top)	**P5 (Right)**	**P3 (Right Bottom)**
		

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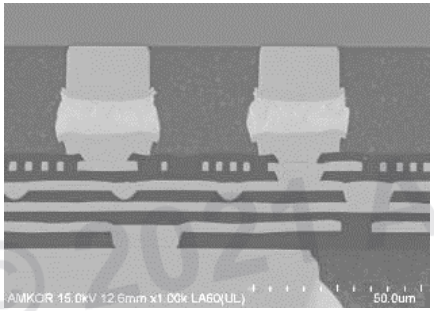
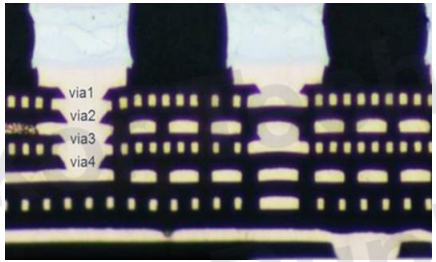
HDFO Status

2 µm L/S, 4 Layer



- ~99% RDL yield
- Stacked vias with minimized dimple
- Reliable screen through AOI and in-line test
- Internal qualification completed for 4L 2/2

2 µm L/S, 6 Layer



6L RDL for routing

- 6L development ongoing 2021
- Product quals 2022

Larger Area, 3x Reticle

- Development ongoing

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S-Connect (IPD and/or Bridge)

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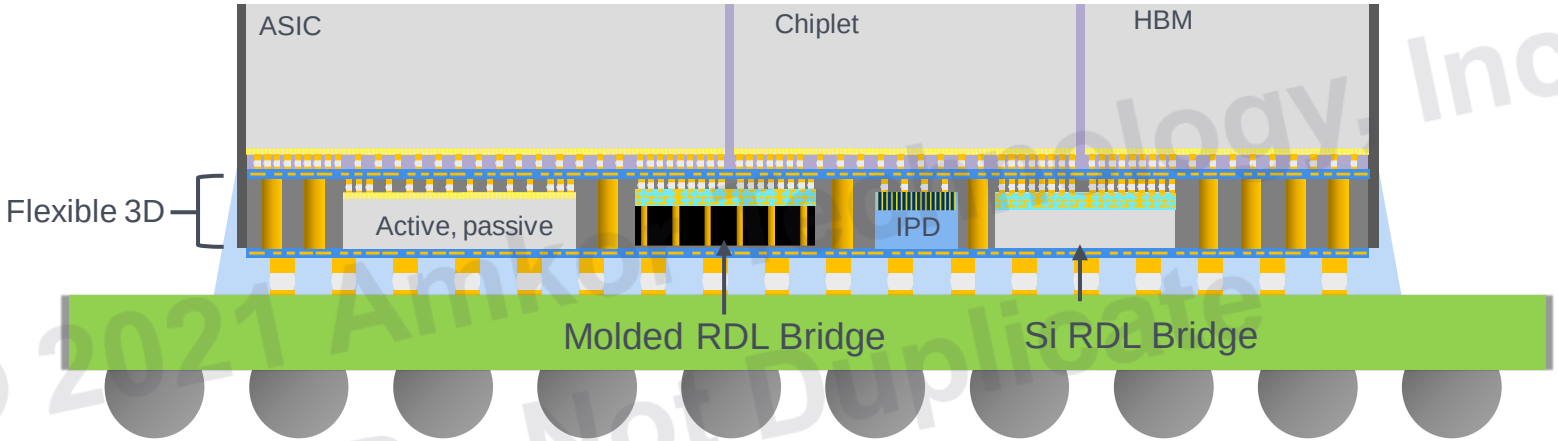
S-Connect



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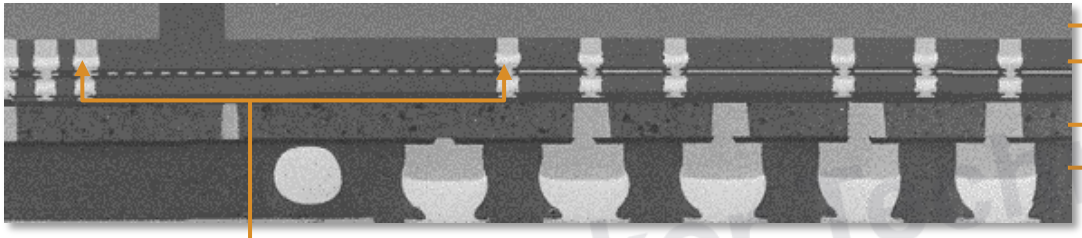
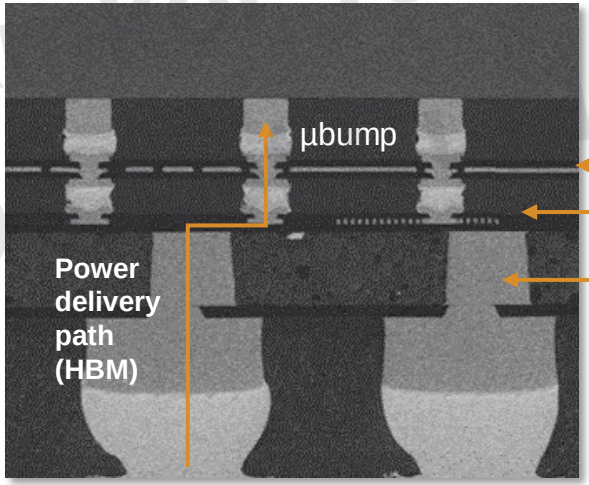
- Extended technology of SWIFT® and S-SWIFT®
- Bridge technology with embedded silicon connect dice for inter-chip connection
- IPD embedment for better power and signal integrity

S-Connect with Molded Bridge



Top die
µbump
Connect module
Cu pillar C4

Die to die connection through molded bridge



Connect module top side RDL
2/2 µm RDL for die to die connect
Through mold via in connect chip

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3D Stacking

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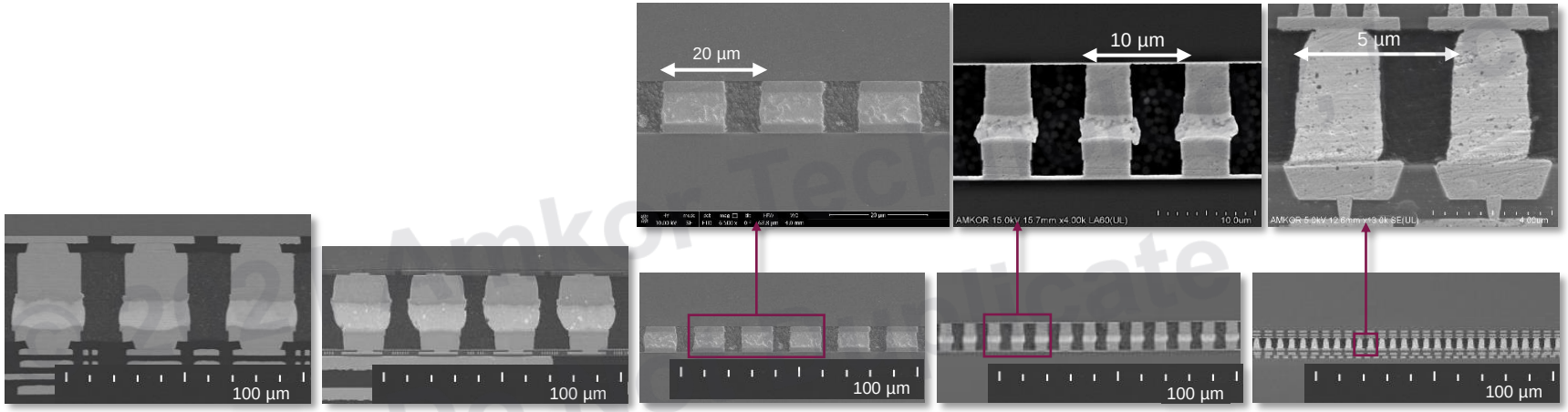
Ultra Fine Pitch Bump Interconnection



45 µm pitch | 30 µm pitch | 20 µm pitch | 10 µm pitch | <10 µm pitch

Production
MR, TC, LAB

Validated
MR

Feasibility test
MR, TC, LAB

Pathfinding
Hybrid, TLP

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Cu-Cu Hybrid Bonding

- 18 µm pitch CuP LF bump demonstrated for CoW application
- 10 µm pitch CuP LF bump demonstrated with Laser Assisted Bonding (LAB)
- Cu-Cu hybrid pathfinding ongoing
  - Amkor would like to co-develop with an alpha customer

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