Road to Chiplets: Architecture

July 13 & 14, 2021

MEPTEC
THE NEXT GENERATION

www.meptec.org

Meptec Workshop
Road to Chiplet: Architecture
July 14th 2021

Chiplets & the HIR Village

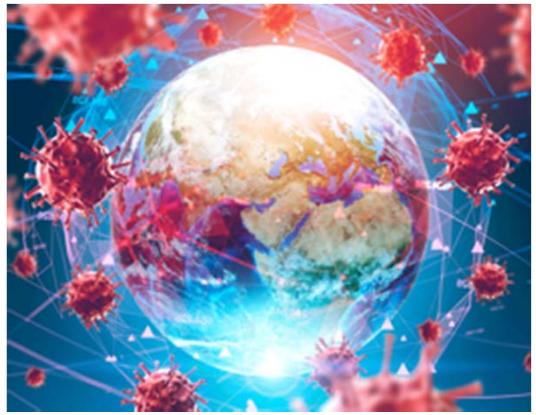
William (Bill) Chen

Ravi Mahajan & WR (Bill) Bottoms

In Collaboration with Heterogeneous Integration Roadmap Technical Working Groups Team

Agenda

- Covid 19 & Digital Transformation
- Coming to End of Technology Scaling
- Heterogeneous Integration Roadmap
- Chiplet & the HIR Village
- Innovations bubbling up everywhere
- Summary



COVID-19 Pandemic

- As we go through the pandemic, we are seeing millions of infections & staggering loss of life, but also incredible heroism, sacrifice, and resilience.
- The rapid advancement of vaccine science, and comprehensive vaccines deployment are tremendous achievements in global collaboration
- While the Delta Covid Variants are surging, we are hopeful in rapid growth of vaccination. We are optimistic to meet face to face once more not too far into the future

2006 Dec 31

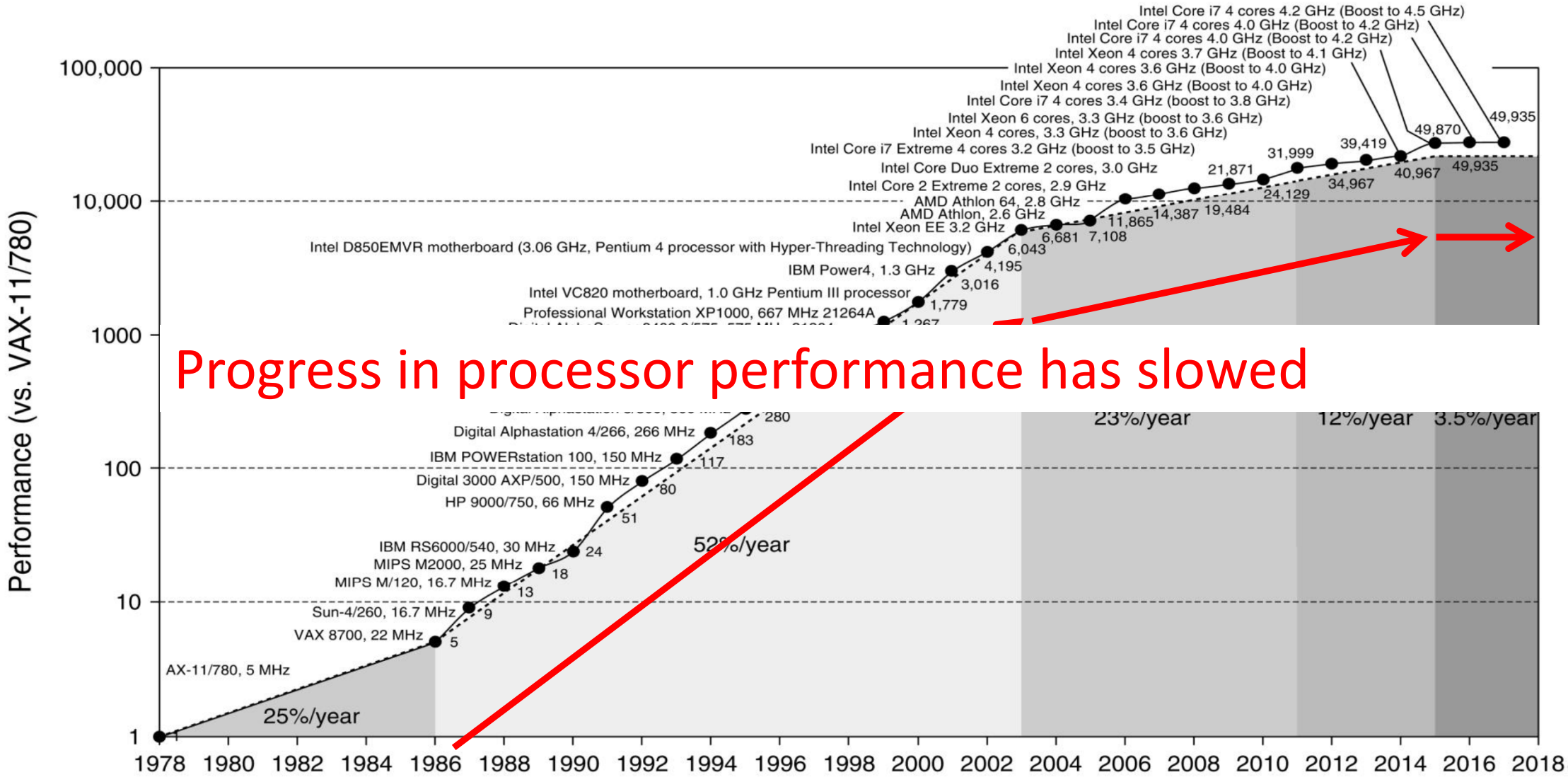
- Exxon Mobil
- General Electric
- Gazprom
- Microsoft
- Citicorp
- Bank of America
- Royal Dutch Shell
- BP
- Petro China
- HSBC

Source 2006 & 2020: Statista & FXSSI

Technology Companies are leading the digital transformation of the global economy and fueling the AI & ML revolution

40 Years Of Progress In Computing

Source: John Hennessy (Chairman Alphabet) Plenary presentation at DARPA ERI Conference July 23 2018



Progress in processor performance has slowed

Moore's Law Economics meeting Headwinds

Source : AMD Lisa Su "Delivering Future of High Performance Computing" Plenary Presentation DARPA ERI Conference July 15, 2019.

Technology Scaling Trends: Exascale in 2021… and then what?

John Shalf (LBNL) “Computing Beyond Moore’s Law” International Supercomputer Conference June 18 2019

HETEROGENEOUS INTEGRATION ROADMAP

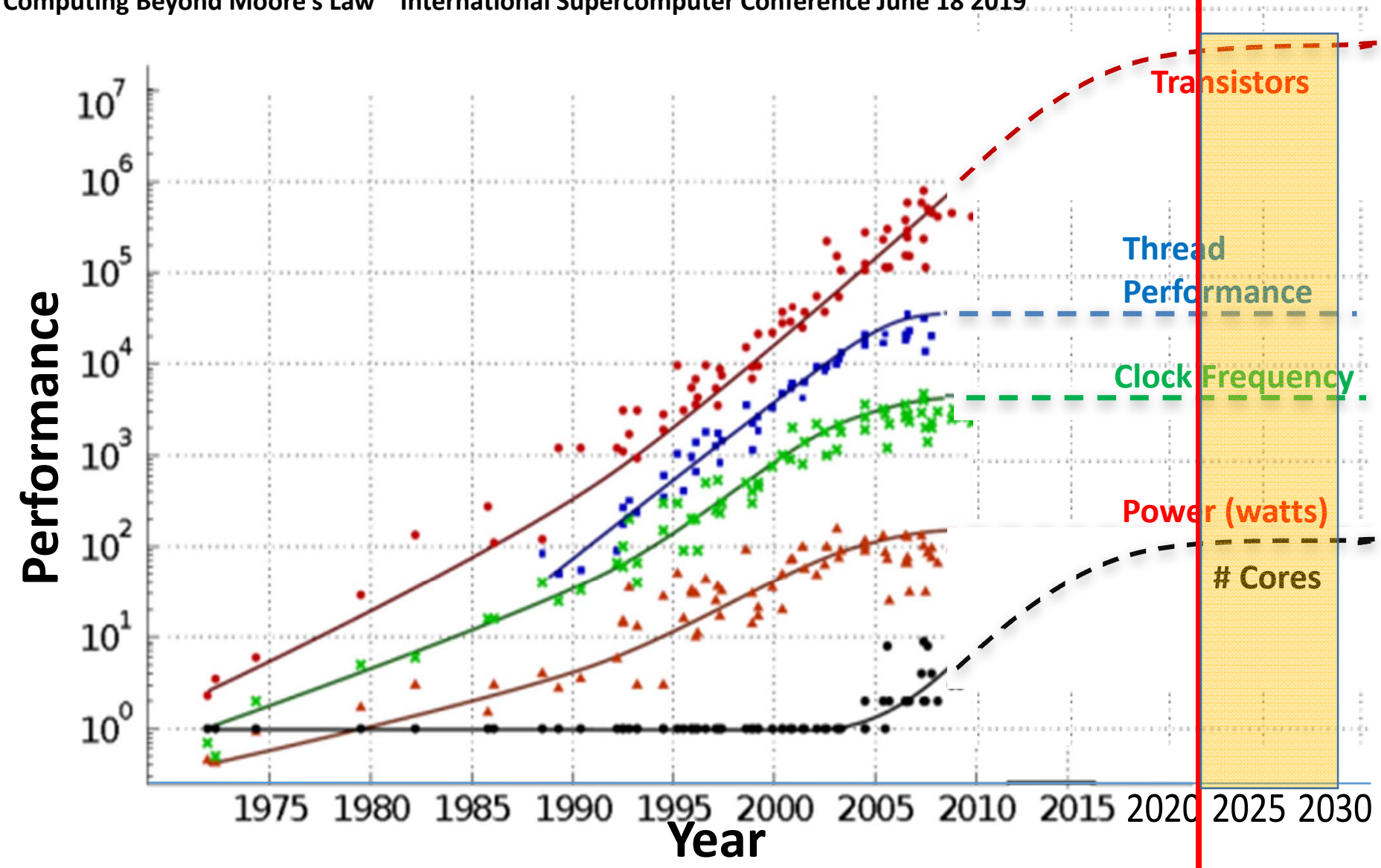


Figure courtesy of Kunle Olukotun, Lance Hammond, Herb Sutter, and Burton Smith – extended by John Shalf

Technology Roadmapping History

HETEROGENEOUS INTEGRATION ROADMAP

1991

World's first Open Source Technology Roadmap, the National Technology Roadmap for Semiconductors (NTRS) sponsored by the US Semiconductor Industry Association (SIA).

1998

NTRS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Technology Roadmap for Semiconductors (ITRS).

2014

The benefits of Moore's Law scaling diminishing and decision was made to end ITRS.

2016

The last edition of the ITRS was published July 8, 2016

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

Heterogeneous Integration Roadmap (HIR)

Launched 10-10-2019
24 chapters
590 Pages
Free download
Download Link
https://eps.ieee.org/technology/heterogeneous-integration-roadmap

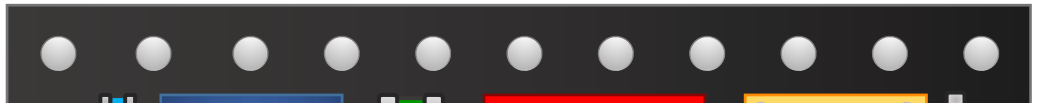
- Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division
- Comprehensively covering microelectronics technology ecosystem
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions
- HIR is the Knowledge Roadmap & Knowledge Supply Chain for the Heterogeneous Future

IEEE Press Release 10-10-2019

PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the **Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines**

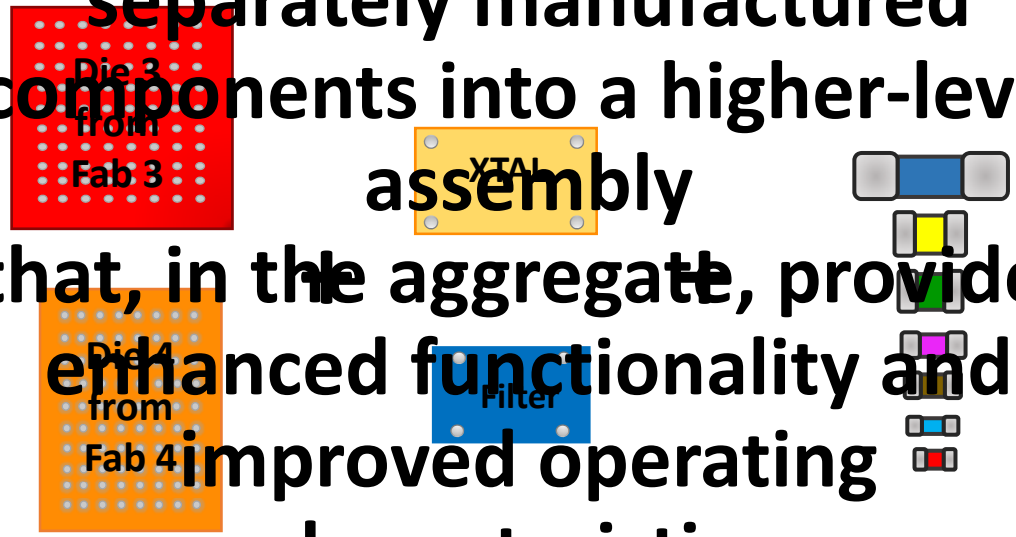
Heterogeneous Integration:

Heterogeneous by material, component type, circuit type, node and bonding/interconnect method & sources



HI is the integration of separately manufactured components into a higher-level assembly

- that, in the aggregate, provides enhanced functionality and improved operating characteristics.



“Cramming More Components onto Integrated Circuits,” *Gordon Moore, Electronics,* pp. 114–117, April 19, 1965.

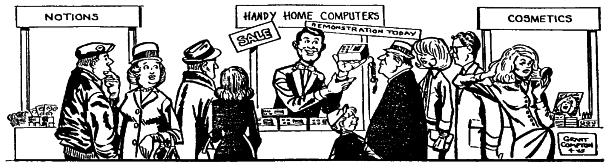


Fig. 2.

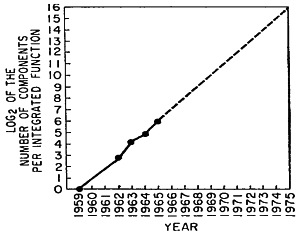


Fig. 3.

VII. Heat Problem

Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?

If we could shrink the volume of a standard high-speed digital computer to that required for the components themselves, we would expect it to glow brightly with present power dissipation. But it won't happen with integrated circuits. Since integrated electronic structures are two dimensional, they have a surface available for cooling close to each center of heat generation. In addition, power is needed primarily to drive the various lines and capacitances associated with the system. As long as a function is confi... to a small area on a wafer, the amount of capa... which must be driven is distinctly limited. In fac... dimensions on an integrated structure mak... e to operate the structure at higher speed... e power per unit area.

VIII. Day of Reckoning

Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large systems out of smaller functions, wh... separately packaged and interconnected. The availab... rge functions, combined with functional design an... n, should allow the manufacturer of large systems ... and construct a considerable variety of equipment ... and economically.

IX. Linear Circuitry

Integration will not change linear systems as radically as digital systems. Still, a considerable degree of integration will be achieved with linear circuits. The lack of large-value capacitors and inductors is the greatest fundamental limitation to integrated electronics in the line...

By their very nature, such elements ... torage of energy in a volume. For high Q it ... y that the volume be large. The incompatibi... ge volume and integrated electronics is obvio... terms themselves. Certain resonance phenom... as those in piezoelectric crystals, can be e... have some applications for tuning functions ... rs and capacitors will be with us for some ...

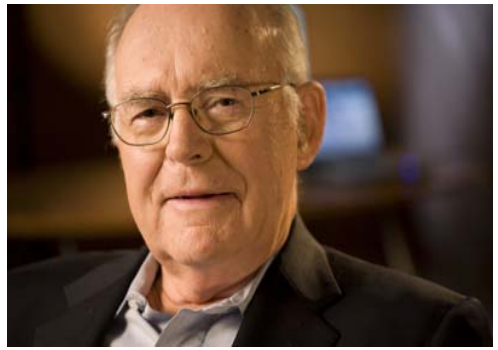
The int... amplifier of the future might well consist o... stages of gain, giving high performance a... cost, interspersed with relatively large tuning ...

...ther linear functions will be changed considerably. The matching and tracking of similar components in integrated structures will allow the design of differential amplifiers of greatly improved performance. The use of thermal feedback effects to stabilize integrated structures to a small fraction of a degree will allow the construction of oscillators with crystal stability.

Even in the microwave area, structures included in the definition of integrated electronics will become increasingly important. The ability to make and assemble components small compared with the wavelengths involved will allow the use of lumped parameter design, at least at the lower frequencies. It is difficult to predict at the present time just how extensive the invasion of the microwave area by integrated electronics will be. The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar.

“VIII. DAY OF RECKONING

----------The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array.”



Revisiting Dr Godon Moore’s words today.

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically.”

A chiplet is a part of a system functional circuit block (SoC) designed to communicate with other chiplets through specific die to die interface. The goal is to manufacture each chiplet economically for optimum cost & performance of the integrated electronics system/subsysteem.

A visionary message for Chiplets, System-in-Package & Heterogeneous Integration

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

The HIR Village

From Wikipedia:

"It takes a village to raise a child" is an African proverb that means that an entire community of people must provide for and interact positively with children for those children to grow and thrive in a safe and healthy environment.

The HIR Village is a community comprising engineers and scientists that voluntarily come together to develop the Heterogeneous Integration Roadmap. It is truly a global village of like-minded people from across diverse disciplines, who all share common vision on maintaining and progressing the Heterogeneous Future for the common good.

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communications & Beyond

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (under formation)

Integration Processes

- SiP
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Co-Design & Simulation

- Co-Design & Simulation – Tools & Practice

Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- **Single Chip and Multi Chip Integration (including Substrates)**
- **Integrated Photonics**
- **Integrated Power Electronics**
- **MEMS & Sensor integration**
- **5G Communications & Beyond**

Cross Cutting Technologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (under formation)

Integration Processes

- **SiP**
- **3D +2D & Interconnect**
- **WLP (fan in and fan out)**

Co-Design & Simulation

- **Co-Design & Simulation – Tools & Practice**

Heterogeneous Integration Roadmap

An Application Driven Roadmap

Market/System Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components

- **Single Chip and Multi Chip Integration (including Substrates)**
- **Integrated Photonics**
- **Integrated Power Electronics**
- **MEMS & Sensor integration**
- **5G Communications & Beyond**

Cross Cutting Teeechnologies

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- Reliability (under formation)

Integration Processes

- **SiP**
- **3D +2D & Interconnect**
- **WLP (fan in and fan out)**

Co-Design & Simulation

- **Co-Design & Simulation – Tools & Practice**

Beyond Miniaturization Tunnel

Photo credit: Prof. H.-S.P. Wong, Stanford

At 2020 ERI Conference the Plenary Speaker, (Prof Philip Wong, Stanford University, and TSMC Chief Scientist) gave talk “Future is System Integration. He illustrated semiconductor research near the end Moore’s Law like a person walking out of a long tunnel seeing green field & sun light.

During Moore’ s Law time the single focus is miniaturization towards the next set of nodes.

As one emerges from the miniaturization tunnel, opportunities for research outlook & innovations becomes infinitely brighter and broader.

Photo Source: S. Mitra, HIR Symposium Feb 24, 2021

Innovations bubbling up everywhere!!

Explorations of new system & package architectures, new materials & new devices, and innovative solutions to design, cost, security, time to market

Virtual Reality

AI & ML for everything

Integrated Photonics

Si Bridge & 3D

WL & PL Fan Out

Brain wave control of complex systems

Nanotube transistors

Qbits

AI + Co-Design &
Co-Simulation

Photon Computers

materials design

Implantable sensors for health care

Robotics everywhere

Plasmonic Devices

DARPA CHIPS Program

Source: “Extending Moore’s Law Through Heterogeneous Integration” Andreas Olofsson, SEMICON West July 10, 2020

HETEROGENEOUS INTEGRATION ROADMAP

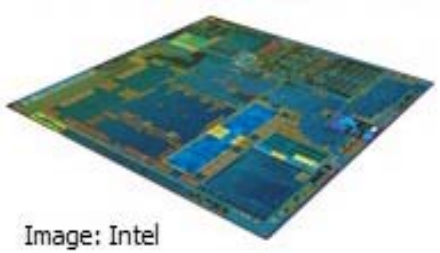
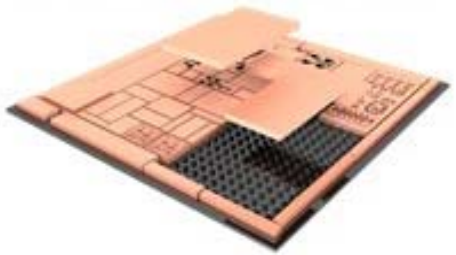
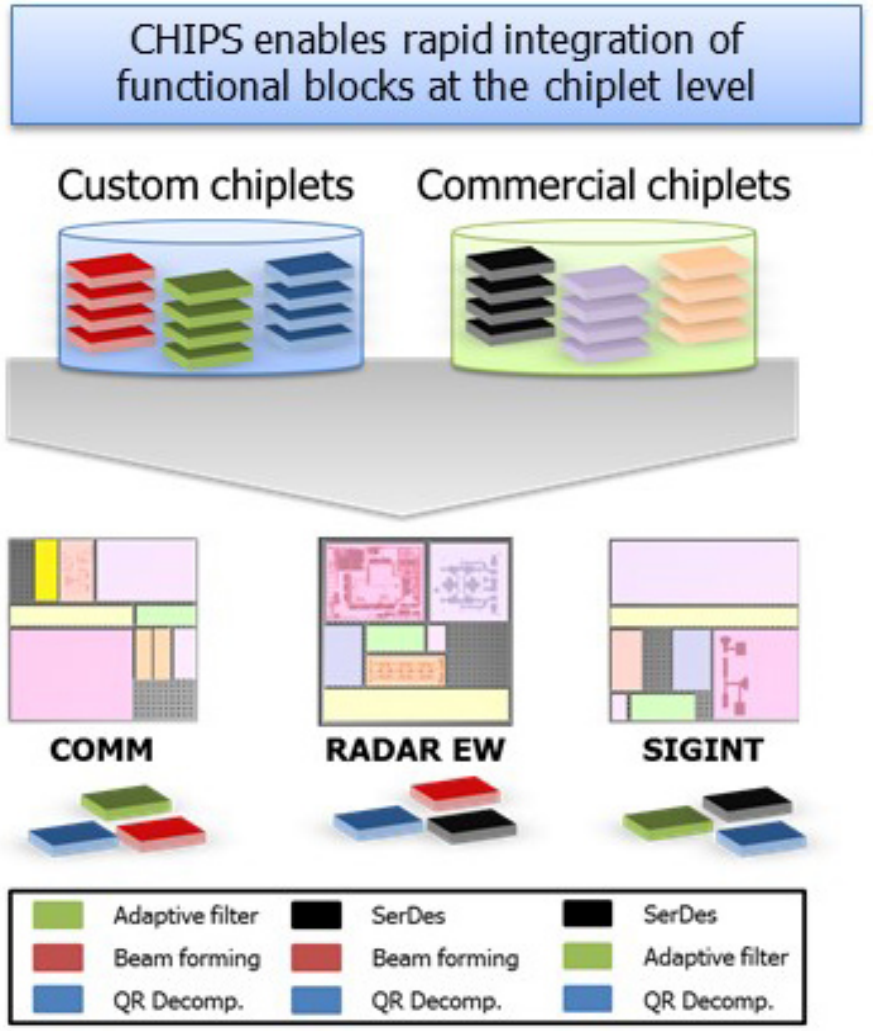


Image: Intel

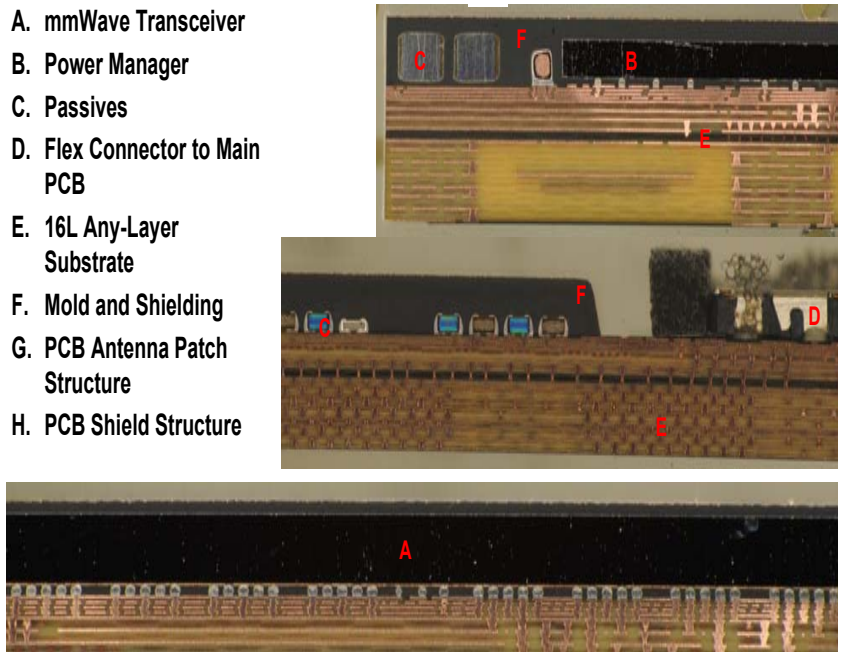




Two 5G mmWave Antenna Modules

IPHONE 11 PRO 5G mmWAVE TRANSCEIVER/ANTENNA AiP MODULE
(21X3.7X1.0 mm)

A. mmWave Transceiver
B. Power Manager
C. Passives
D. Flex Connector to Main PCB
E. 16L Any-Layer Substrate
F. Mold and Shielding
G. PCB Antenna Patch Structure
H. PCB Shield Structure



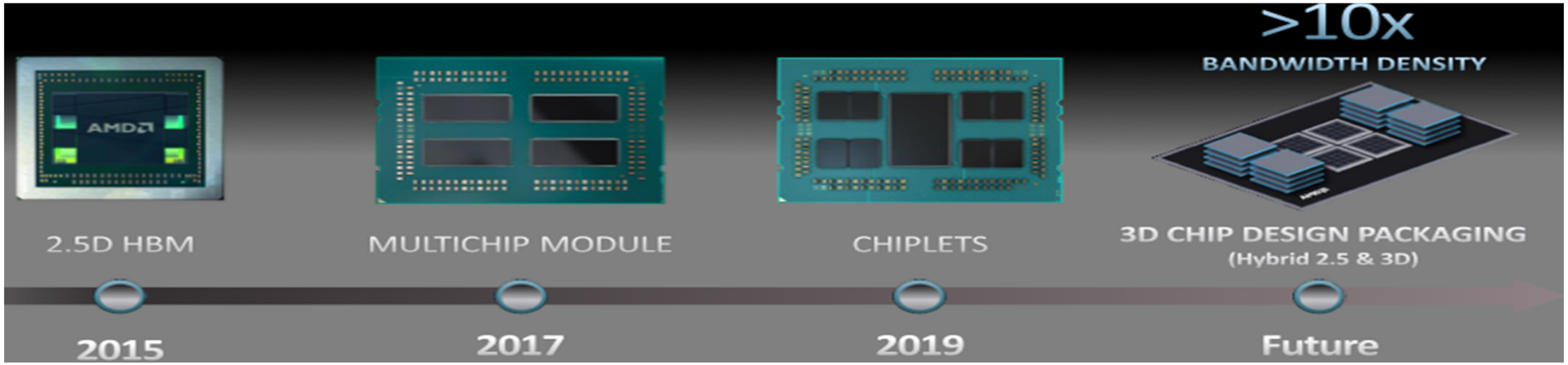
SAMSUNG GALAXY S10 mmWave 5G ANTENNA MODULES

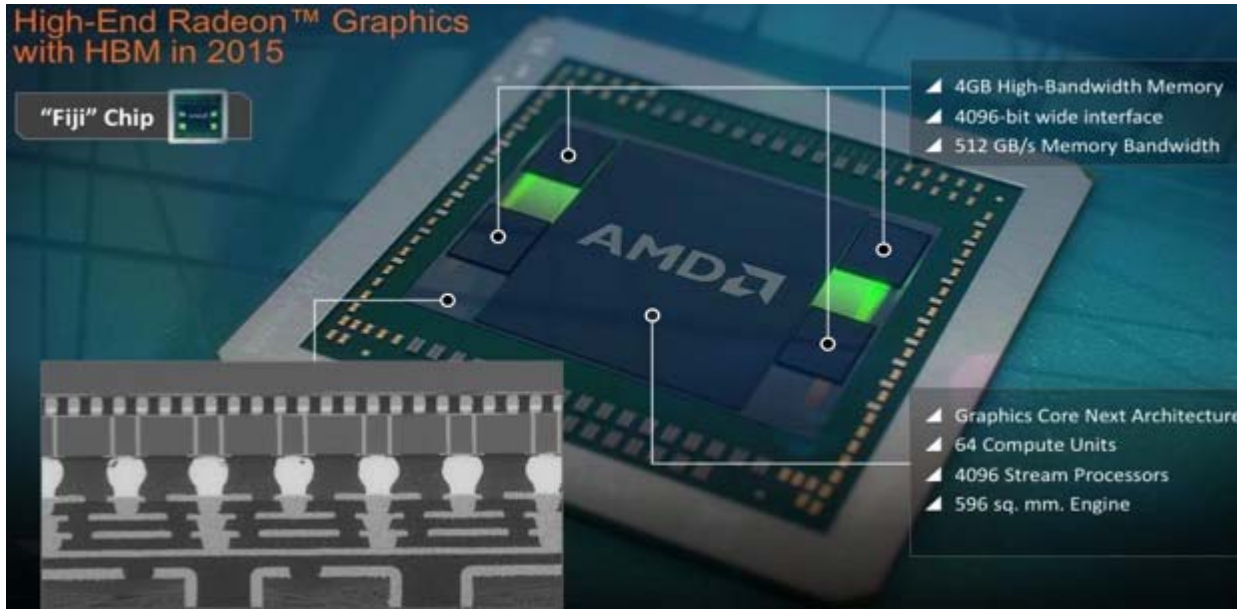
Source: Prismark Partners & Binghamton University

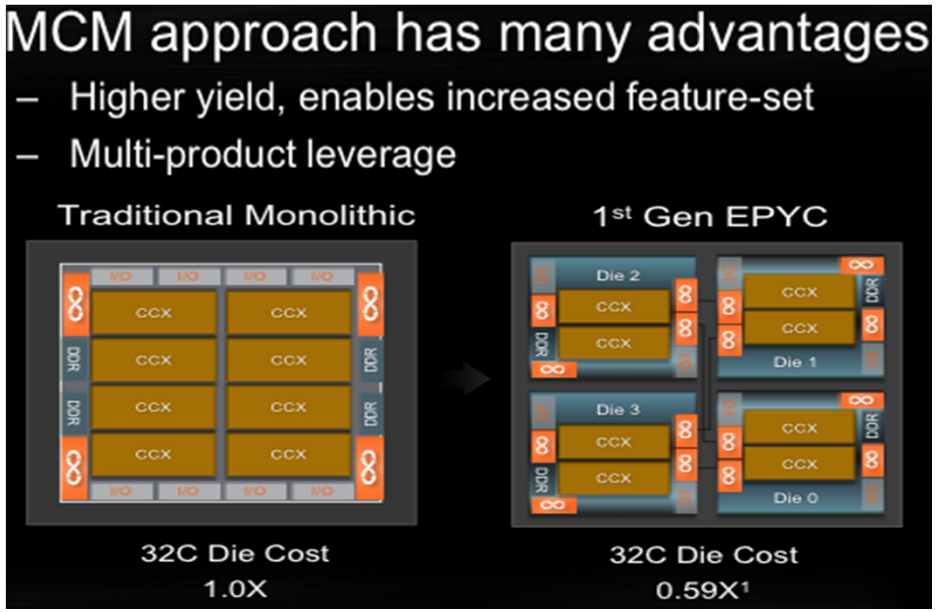
IEEE | IEEE photonics Society | semi | IEEE ELECTRONICS PACKAGING SOCIETY | ASME | ELECTRON DEVICES SOCIETY

Advance Package Integrations at AMD : 2.5D & 1st Gen EPYC MCM

Source: "Chiplets, How to utilize them, what can they do." Dr Bryan Black: IMAPS October 5-8, 2020

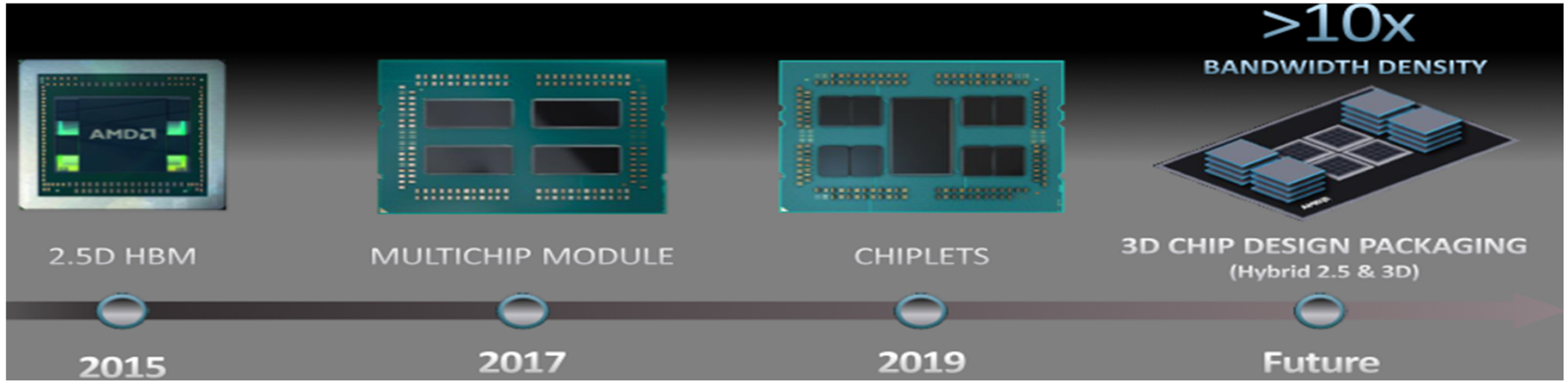


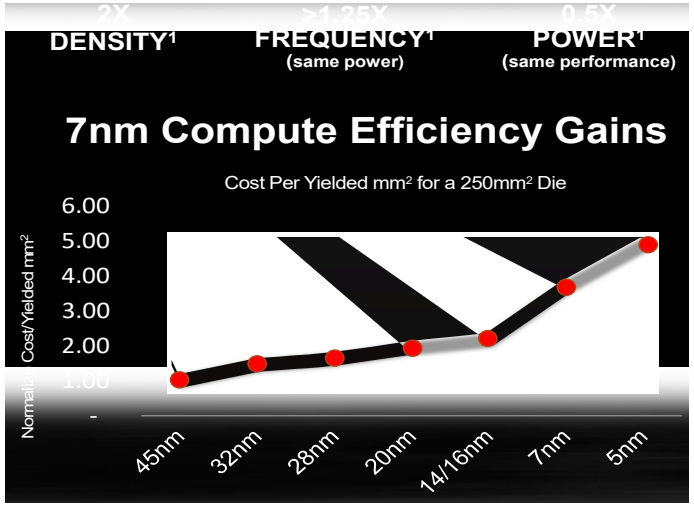


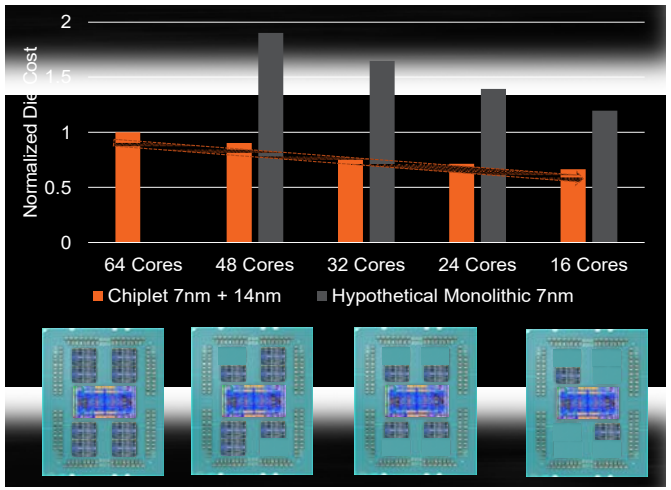


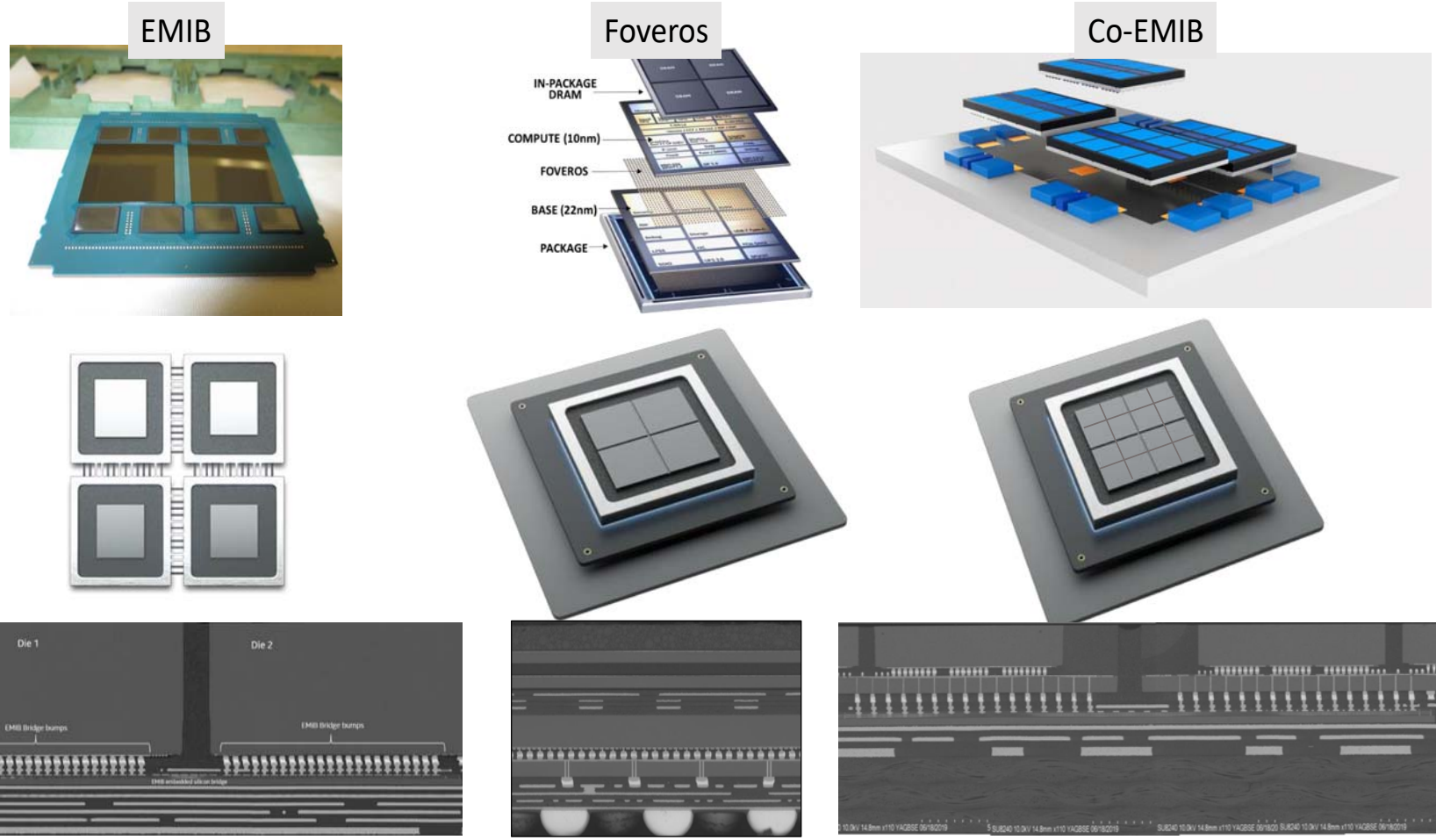
Adv Package Integrations at AMD : 2nd Gen EPYC Chiplets

Source: "Chiplets, How to utilze them, what can they do." Bryan Black: IMAPS October 5-8, 2020









Advance Package Chiplet Integration Technologies at Intel: EMIB, Foveros & Co-EMIB

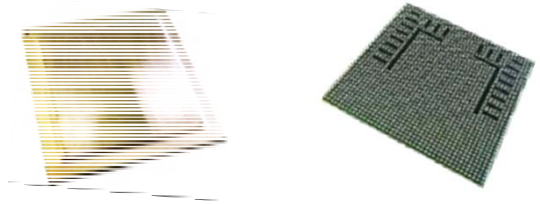
Source: "Adv Package Architecture for Heterogeneous Integration" Ravi Mahajan , Next Gen Electronic System Workshop Binghamton University October 8, 2020. Also Babak Sabi, IMAPS October 5-8 2020

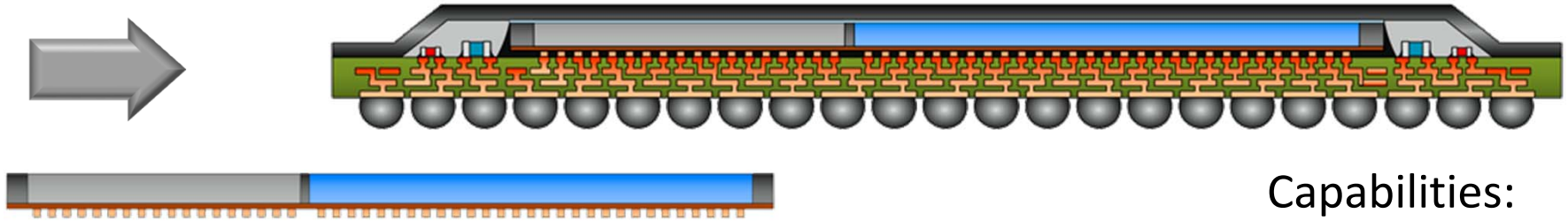
IEEE
IEEE photonics Society
semi
IEEE ELECTRONICS PACKAGING SOCIETY
ASME
ELECTRON DEVICES SOCIETY

FOCoS – Fan Out Chip on Substrate

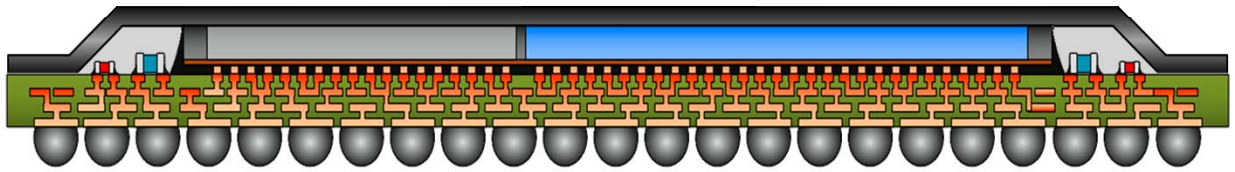
Acknowledgement: John Hunt (ASE)

APU + Memory
GPU + Memory
Networking
SiP/ Modules
AI
Chiplets





Fan Out Compound Die

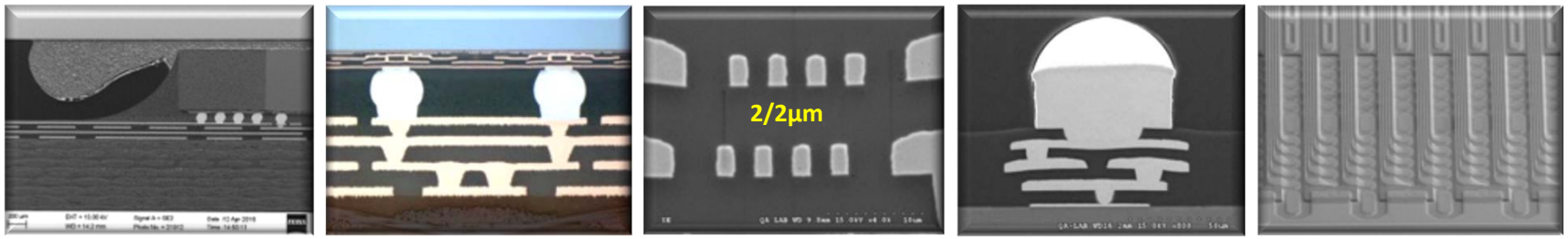


Fan Out Hybrid BGA Package

Capabilities:

- 2/2µm L/S
- 6 Metal Layers
- 33x38mm FO
- 74x74mm Pkg

- Hybrid solution: FO & BGA
- High density 2D & 3D interconnection in RDL Layers
- Advanced Fan Out & FlipChip
- Most complex Fan Out in production



Multiple products in volume production since January 2016

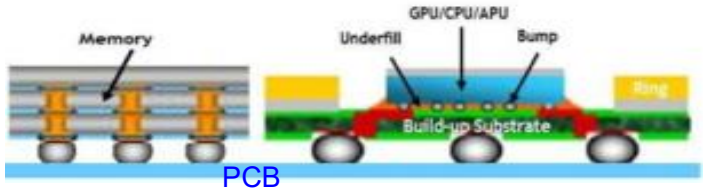
2.5D with Si Interposer

Source: ASE Group

Compare with Traditional Flip-Chip

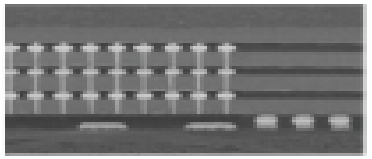
- > 20 times more bumps
- 30 times smaller Line/Space between chips

FCBGA

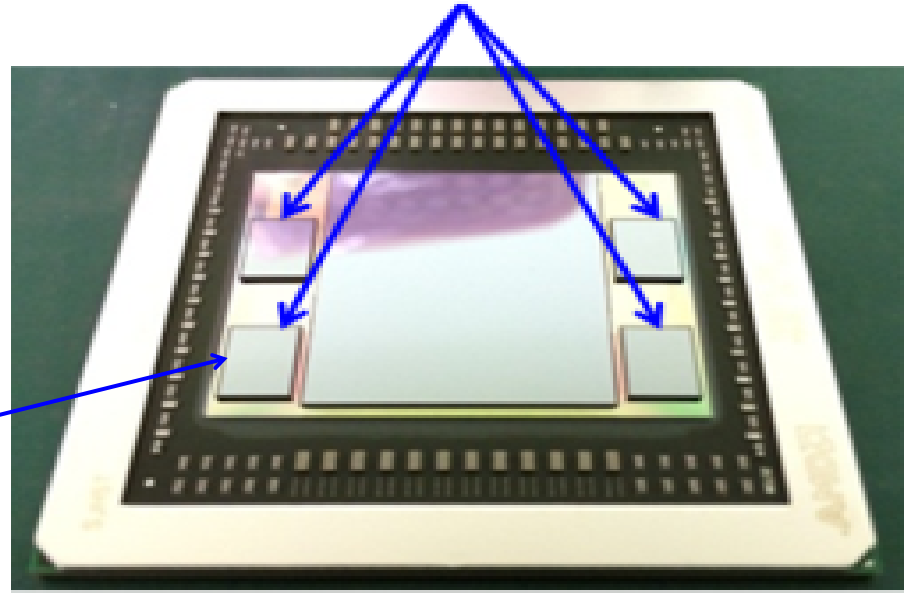


Integrating System to SiP

2.5D FCBGA (3D IC inside)

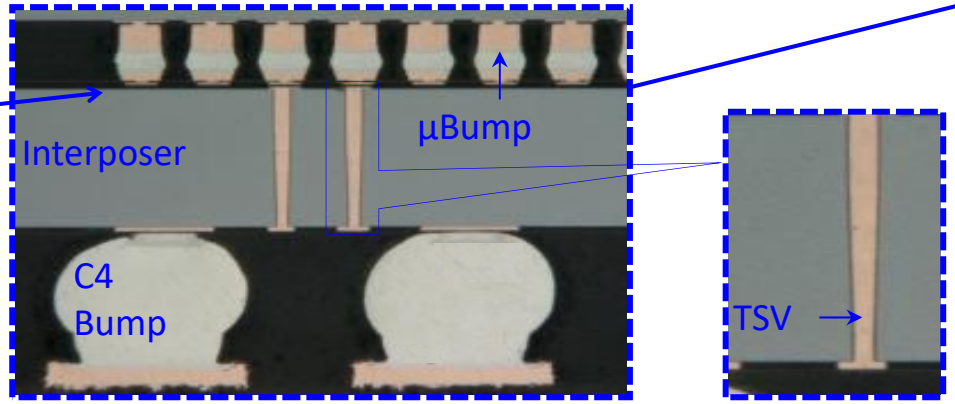


HBM (High Bandwidth Memory)

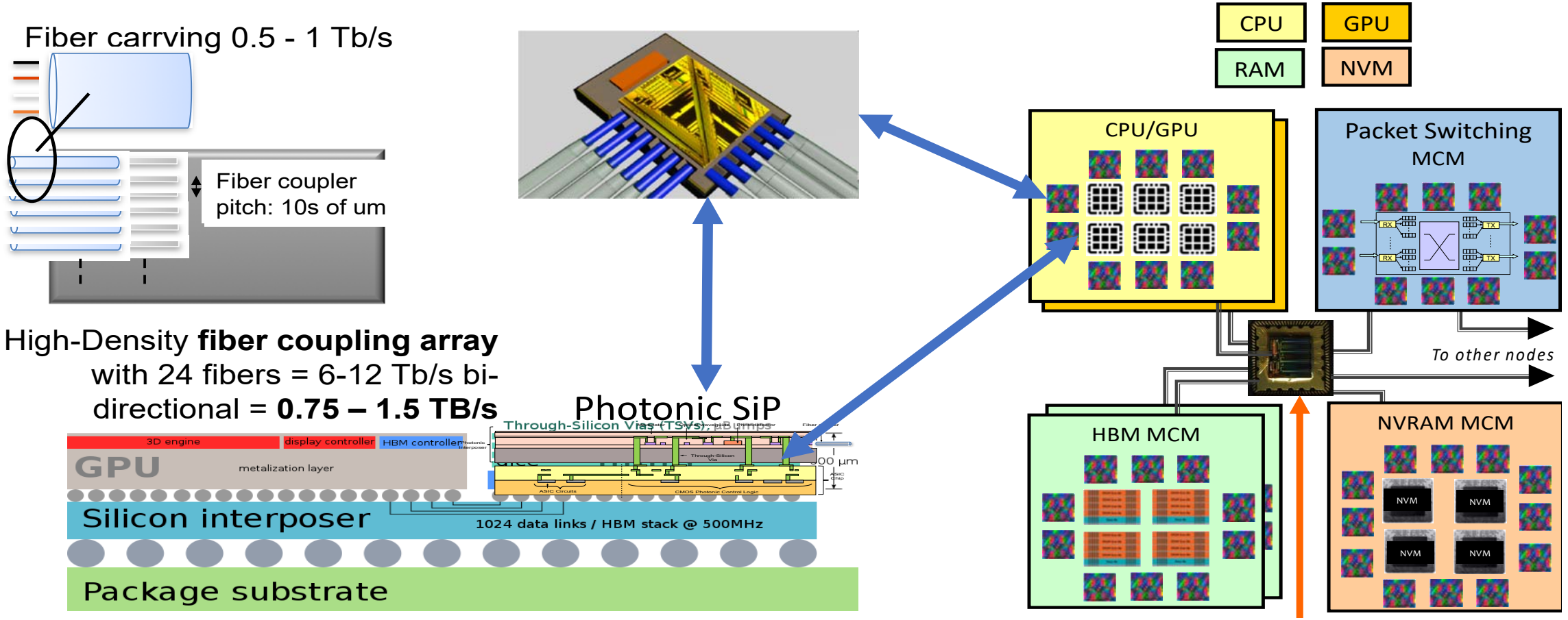


World's 1st 2.5D IC with HBMs

Fine L/S:
0.5um/0.5um



Silicon Photonics Co-Package Integration



Si Photonics Integration Concept. Source: John Shalf (LBNL) [10]

Summary

HETEROGENEOUS INTEGRATION ROADMAP

- We are at a unique period in time where the global convergence of technology chaos & business disruption are suddenly joined by the Covid 19 Pandemic still spreading around the world.
- There is immense need for a pre-competitive technology roadmap addressing future vision, difficult challenges, potential solutions.
- Chiplet is a powerful technology direction for system/subsysteem integration.
- The HIR Village is is truly a global village of like-minded people from across diverse disciplines, who all share common vision on maintaining and progressing the Heterogeneous Future for the common good.
- .

IEEE IEEE photonics Society semi IEEE ELECTRONICS PACKAGING SOCIETY ASME ELECTRON DEVICES SOCIETY

HETEROGENEOUS INTEGRATION ROADMAP

"We choose to go to the moon in this decade and do the other things, not because they are easy, but because they are hard, because that goal will serve to organize and measure the best of our energies and skills, because that challenge is one that we are willing to accept one we are unwilling to postpone, and one which we intend to win, and the others, too."

President John F Kennedy, September 12, 1962

In full acknowledgement of the spirit of dedicated collaboration of Heterogeneous Integration Roadmap Technical Working Groups

Thank you ALL for Listening

Thank you sponsors!

ADVANTEST®

Amkor Technology®

SYNOPSYS®

MEPTEC
THE NEXT GENERATION

Global Companies Rate Advantest THE BEST ATE Company 2021

Advantest receives highest ratings from customers in annual VLSIresearch Customer Satisfaction Survey for 2 consecutive years.

Global customers name Advantest THE BEST supplier of test equipment in 2020 and 2021, with highest ratings in categories of:

Technical Leadership – Partnership – Trust – Recommended Supplier – Field Service

"Year-after-year the company has delivered on its promise of technological excellence and it remains clear that Advantest keeps their customers' successes central to their strategy. Congratulations on celebrating 33 years of recognition for outstanding customer satisfaction."

— **Risto Puhakka**, President VLSIresearch

Amkor's Differentiators

Technology

Advanced Packaging Leadership
Engineering Services
Broad Portfolio

Quality

QualityFIRST Culture
Execution
Automation

Service

Design & Test Through Drop Ship
Manufacturing Footprint
Local Sales & Support

© 2021 Amkor Technology, Inc.


SYNOPSYS®
Silicon to Software™

COPYRIGHT NOTICE

This presentation in this publication was presented at the **Road to Chiplets: Architecture Workshop** (July 13 & 14, 2021). The content reflects the opinion of the author(s) and their respective companies. The inclusion of presentations in this publication does not constitute an endorsement by MEPTEC or the sponsors.

There is no copyright protection claimed by this publication. However, each presentation is the work of the authors and their respective companies and may contain copyrighted material. As such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

www.meptec.org

MEPTEC
THE NEXT GENERATION