Road to Chiplets: Architecture

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The Open Domain-Specific Architecture

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Architect, Broadcom Inc

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Outline

OPEN DOMAIN SPECIFIC ARCHITECTURE

SERVER

- Overview: Community, charter
- Review: Progress towards a fully open, practical D2D stack
- **Everything presented is the result of active and significant community collaboration.**
- How to participate

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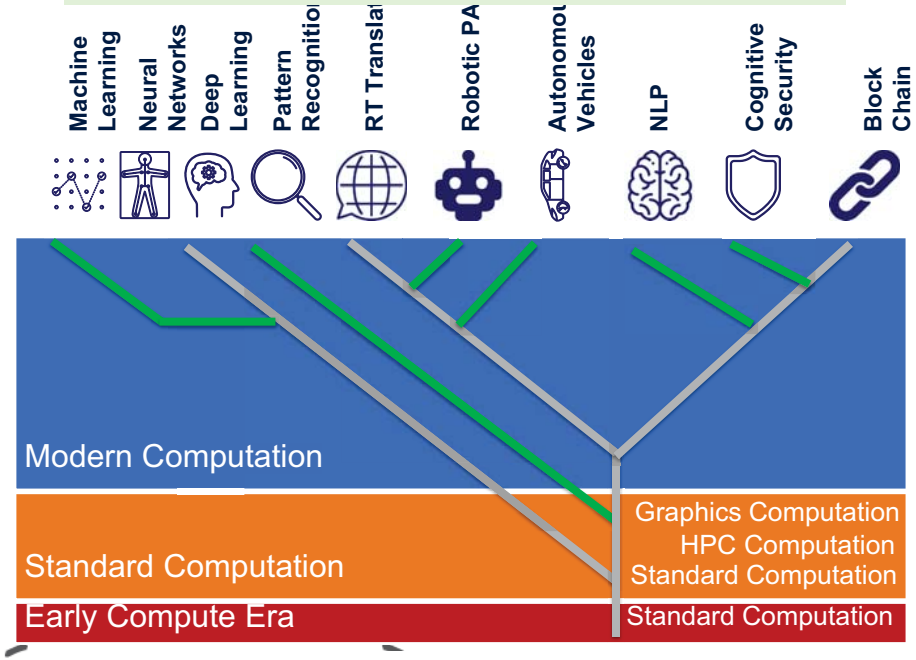
ODSA: Accelerators and Chiplets

Domain-specific architectures (DSAs) to accelerate targeted compute-intensive workloads.

Dharmesh Jani, Facebook –
ODSA Workshop, Regional Summit, Amsterdam, Sep. 2019



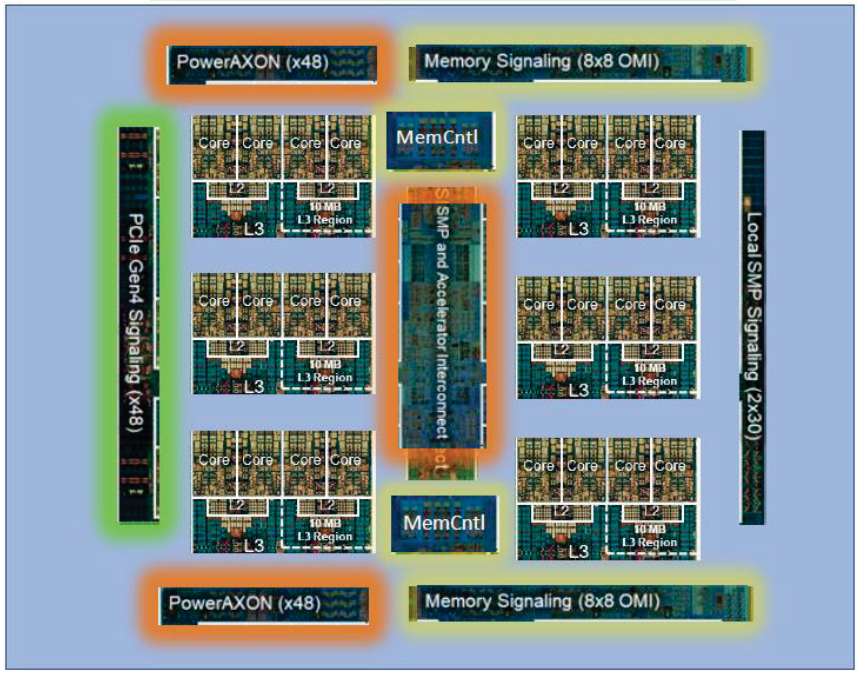
AI/ML/data workload explosion needs DSAs

OPEN DOMAIN SPECIFIC ARCHITECTURE

DSAs built using chiplets with open standard D2D interfaces

Chiplet: Die designed to be used with other die in a package, usually with proprietary interfaces.

Jeff Stuechli, Josh Friedrich, IBM –
ODSA Workshop, IBM, San Jose, Sep. 2019



IBM Power 9: potential modularity

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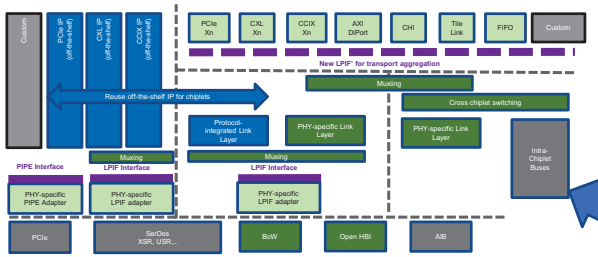
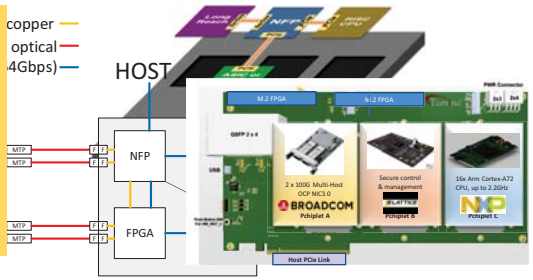
ODSA Charter

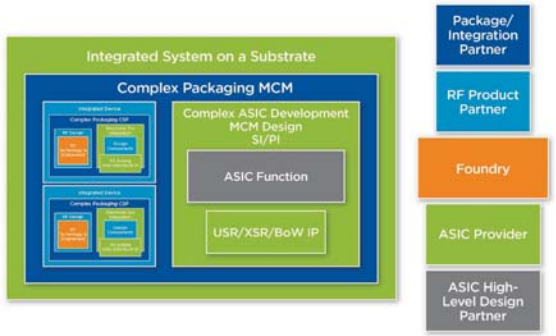
Open D2D Interface
Reduce barrier to interoperation



Reference Designs
Starting point for new designs



Reference Workflows
Reusable, open practices



ODSA Activities

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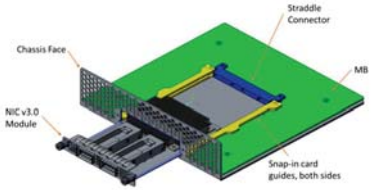
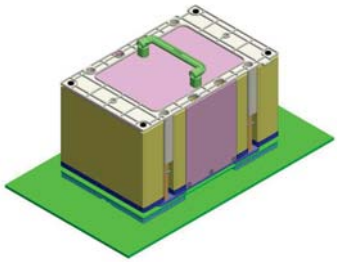
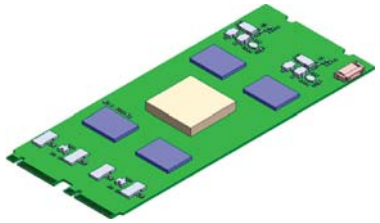
Chiplet Marketplace

Integrate best-in-class chiplets from multiple vendors through open interfaces



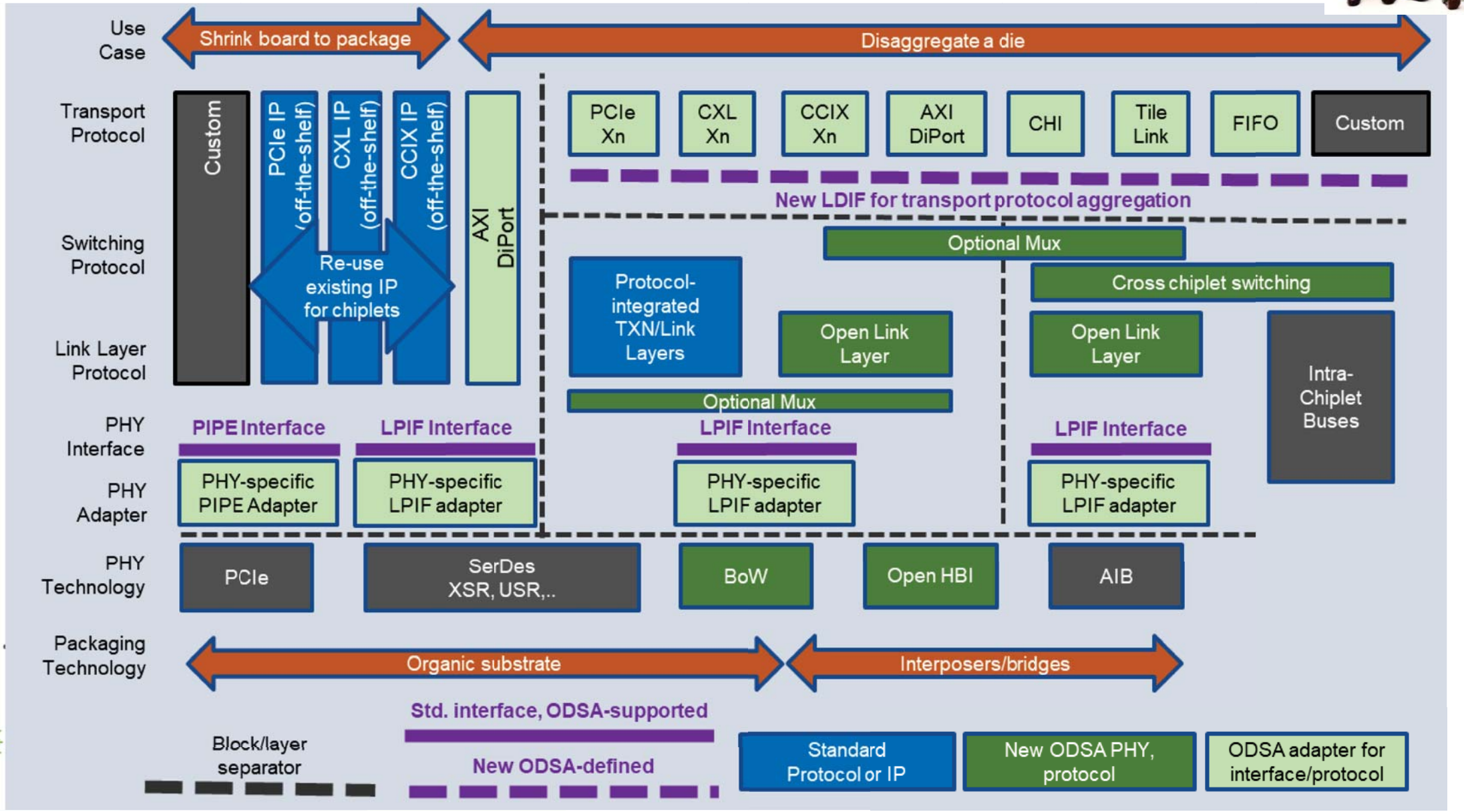




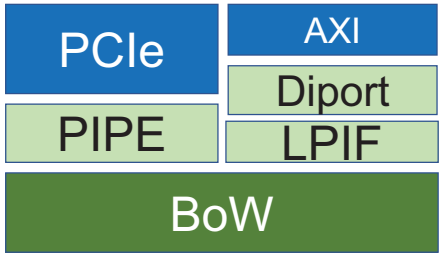
OCP modular form factors

ODSA Stack:

A stack for a marketplace to support the most popular data transaction protocols used by system designers on a wide range of packaging options

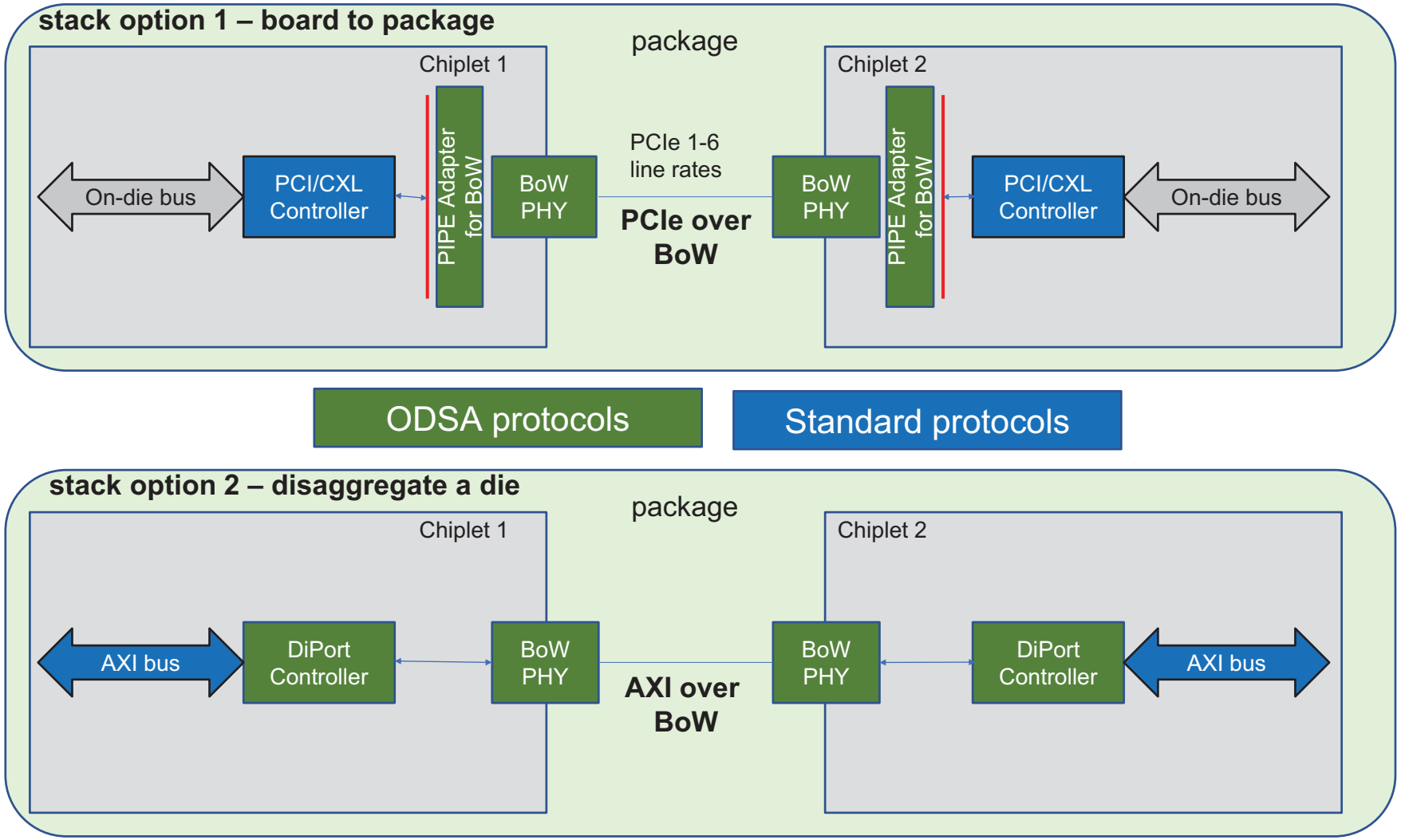


ODSA PHY/Logic D2D Interface



Port the most common system (PCIe/CXL) and SoC (AXI) transaction to chiplets.

- PCIe/CXL over BoW through standard PIPE interface
- AXI over BoW with DiPort contributed by NXP



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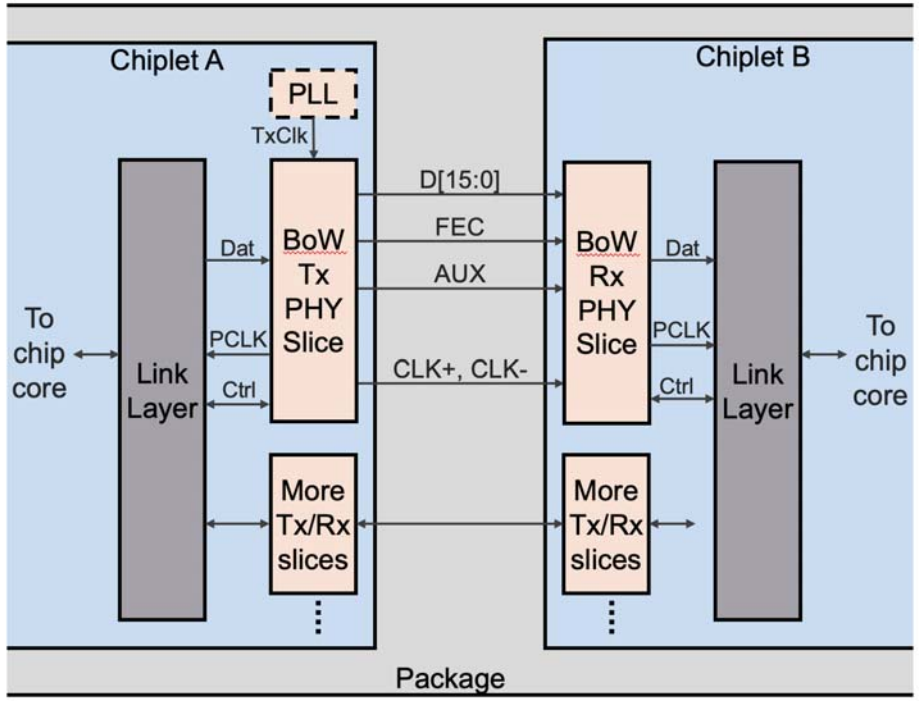
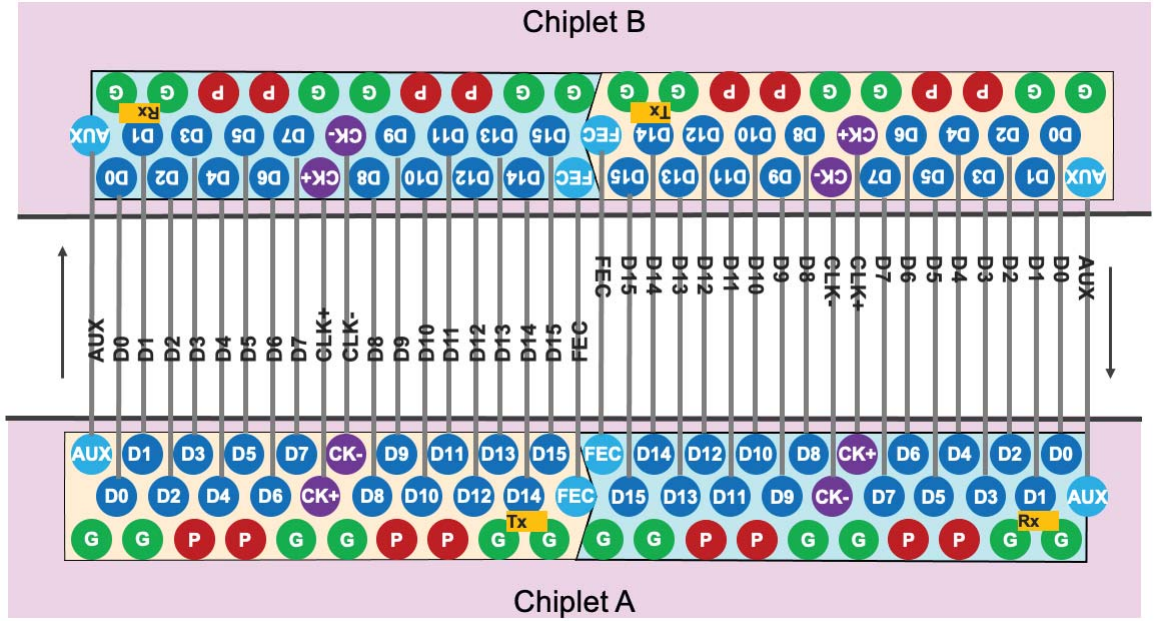
Bunch of Wires PHY

Open D2D PHY:

- Simple clock-forward base parallel PHY – 4-8 Gbps/wire, < 5 ns latency, 0.75V
- Supports process nodes from 3nm to 65nm to enable heterogeneous designs.
- Progress on: Electricals, bump maps, logic interface, initialization & control
- https://github.com/opencomputeproject/ODSA-BoW



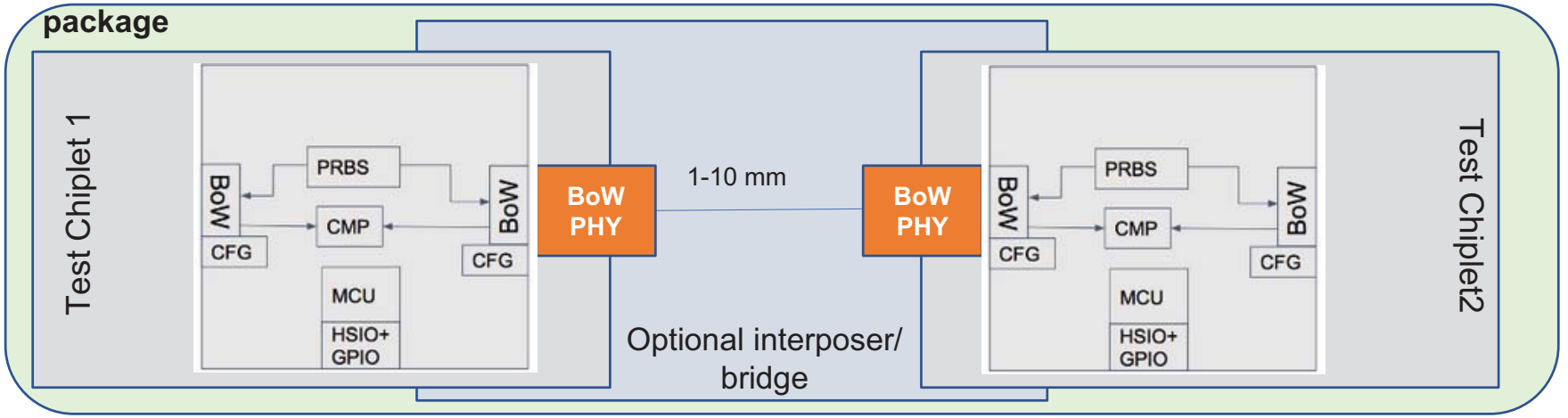


BoW PHY Modes

All BoW modes are implemented as slices with a differential Tx clock pair, 16 data wires and 2 additional optional wires for two of FEC, DBI and control.				Laminate Packaging			Advanced Packaging
				Unterminated	Source Terminated	Doubly Terminated	Unterminated
Mode	TxClk Freq Ghz	Per-wire Bit Rate Gbps	Per-Slice Bit Rate Gbps	Reach			
BoW-32	1	2	32	10	20	50	4
Bow-64	2	4	64	Not Specified	10	50	2
BoW-128	4	8	128	Not Specified	5	50	1
BoW-256	8	16	256	Not Specified	Not Specified	50	Not Specified

Only PHY to offer a graceful cost-performance trade-off

BoW Test Chiplet: Close the Data Gap



	Data	Willing to License GDS II	Free GDSII	Design Files	Royalty	Support
Open Data	**x**	**x**			**Negotiate**	**Negotiate**
Open Design	x	No License	Encrypted		None	Negotiate
Open Schematic	x	No License	x	x	None	Negotiate

Gold, Silver and Bronze participation options. Please – get involved!

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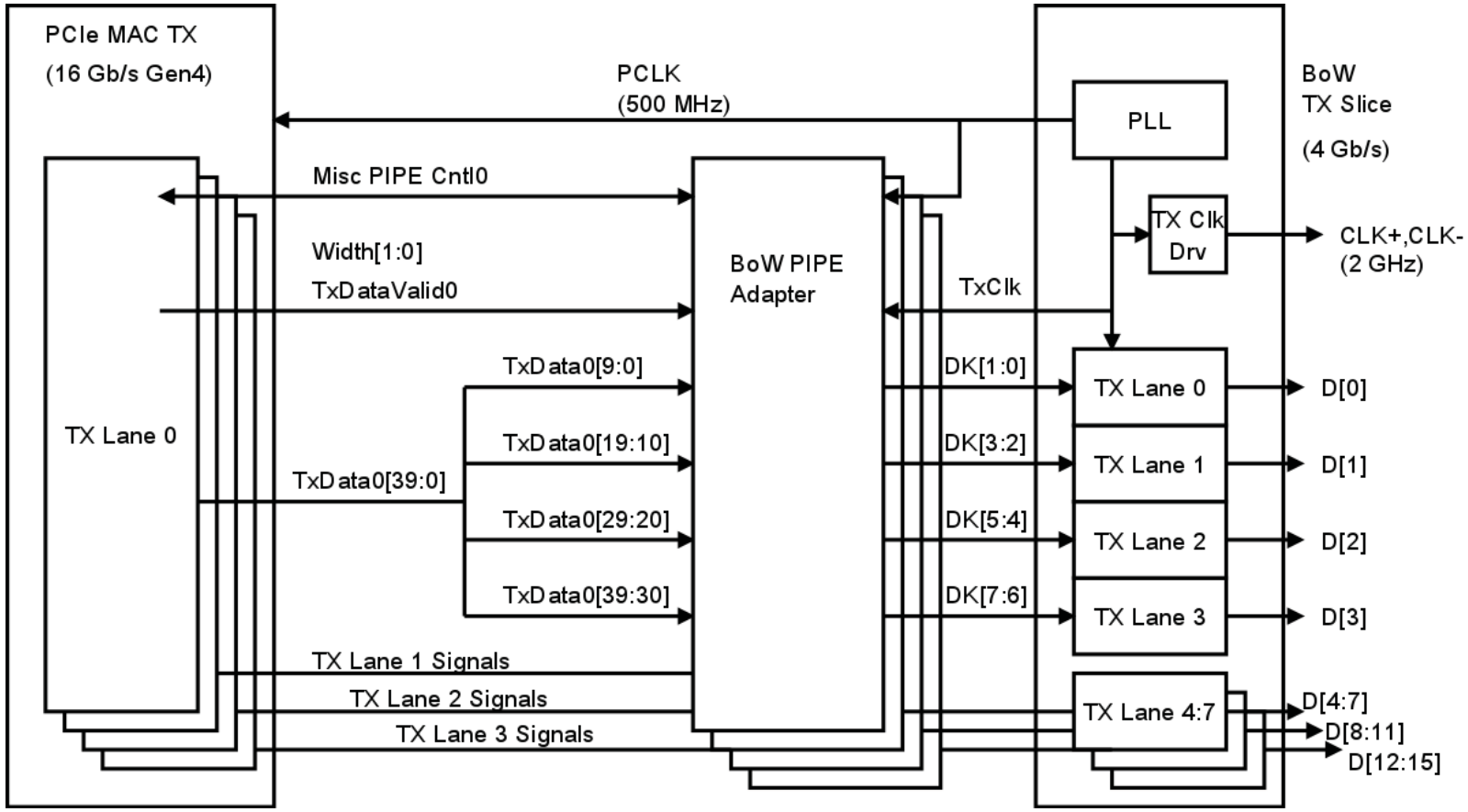
PIPE Adapter

Underlay for PCIe transactions over a D2D interface

Adapter emulates a PCIe PHY to a controller



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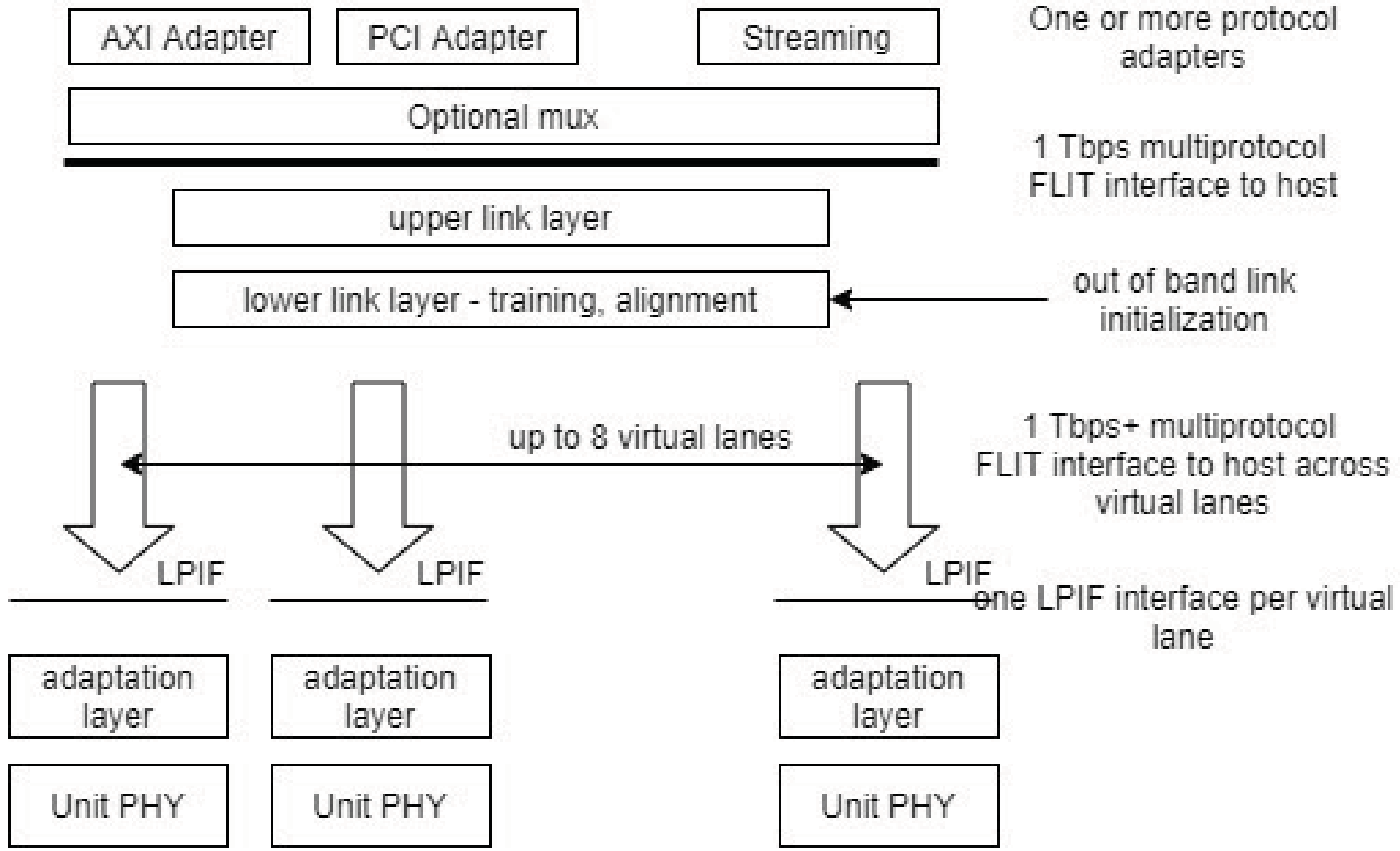
Open Link Layer

Requirements based on survey of end users, semi vendors

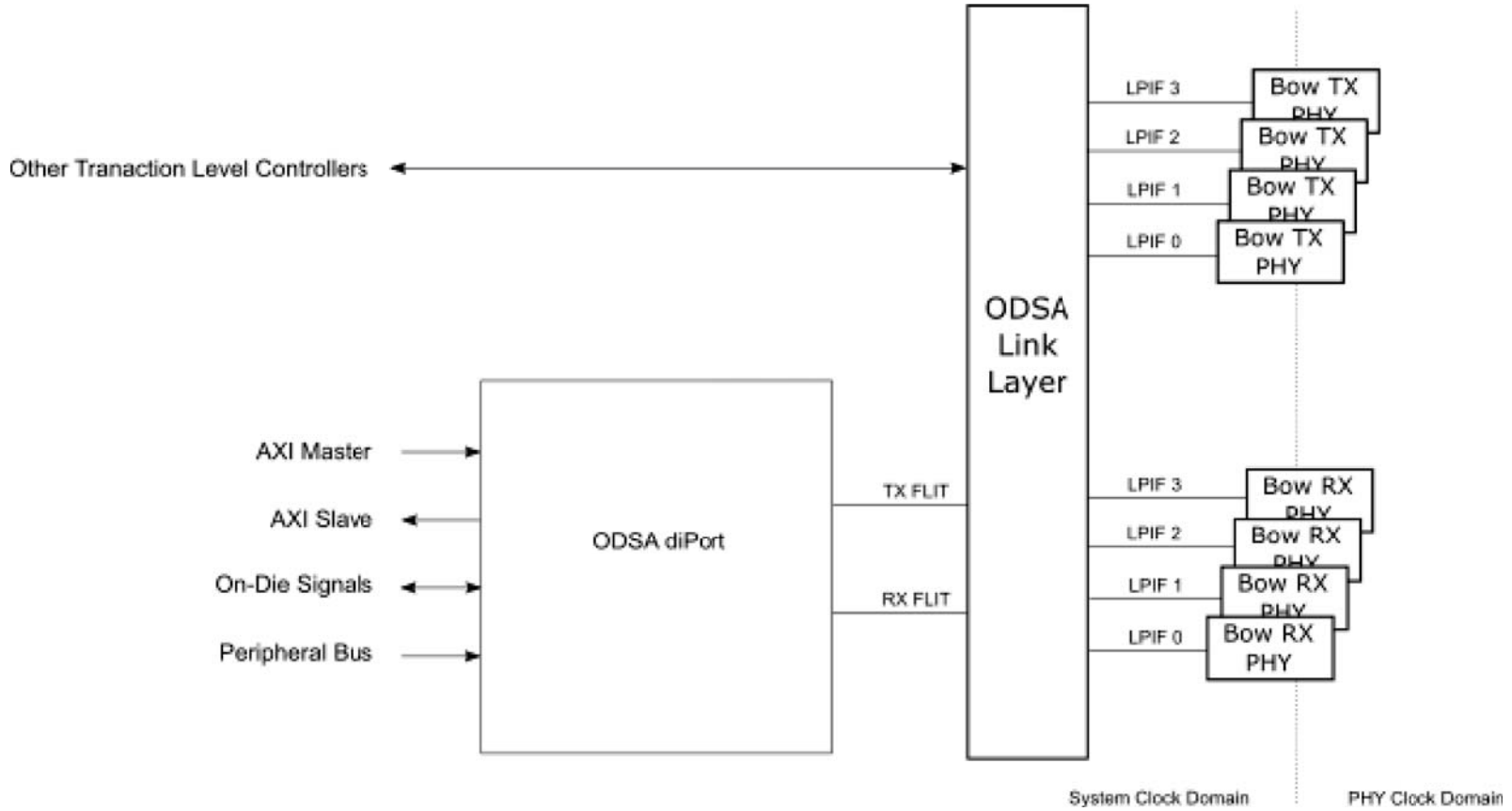
Gathering participants for spec development



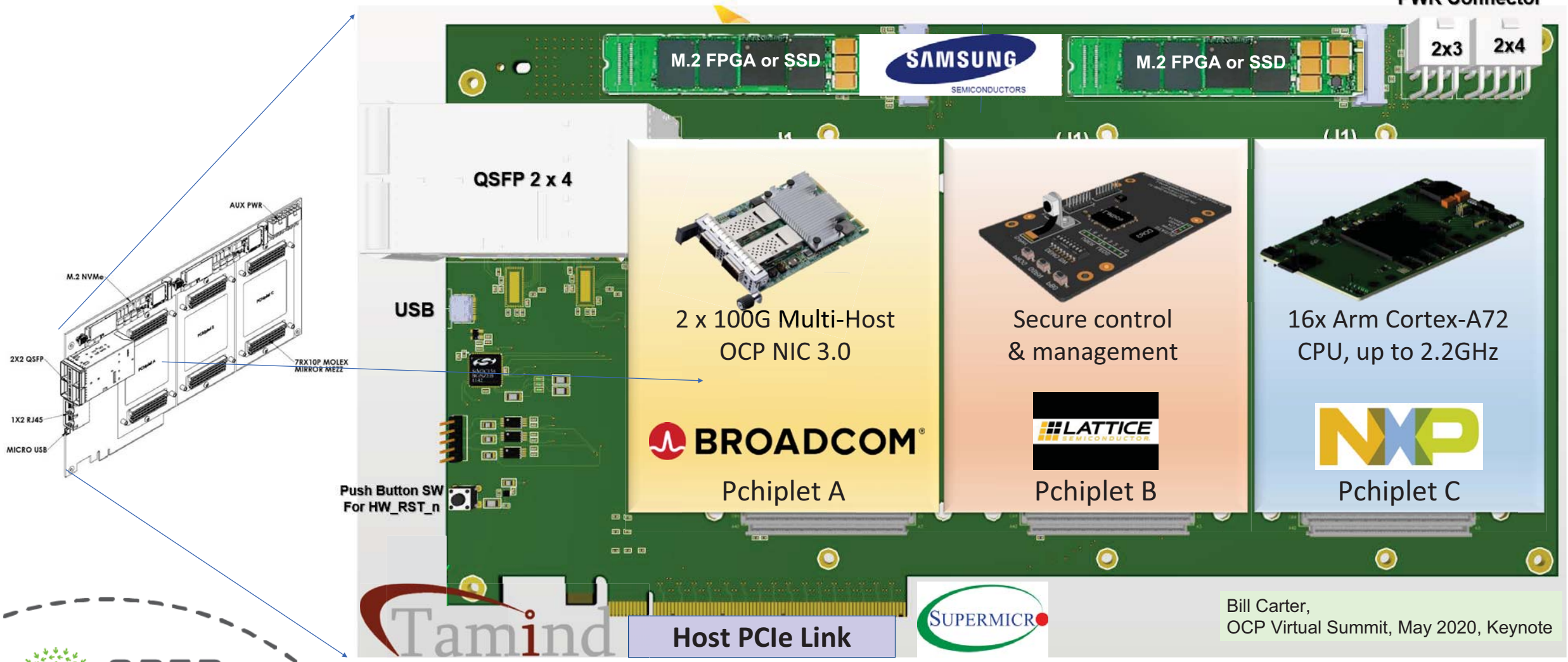
DiPort

Packetize AXI transactions over BoW

Contribution from NXP

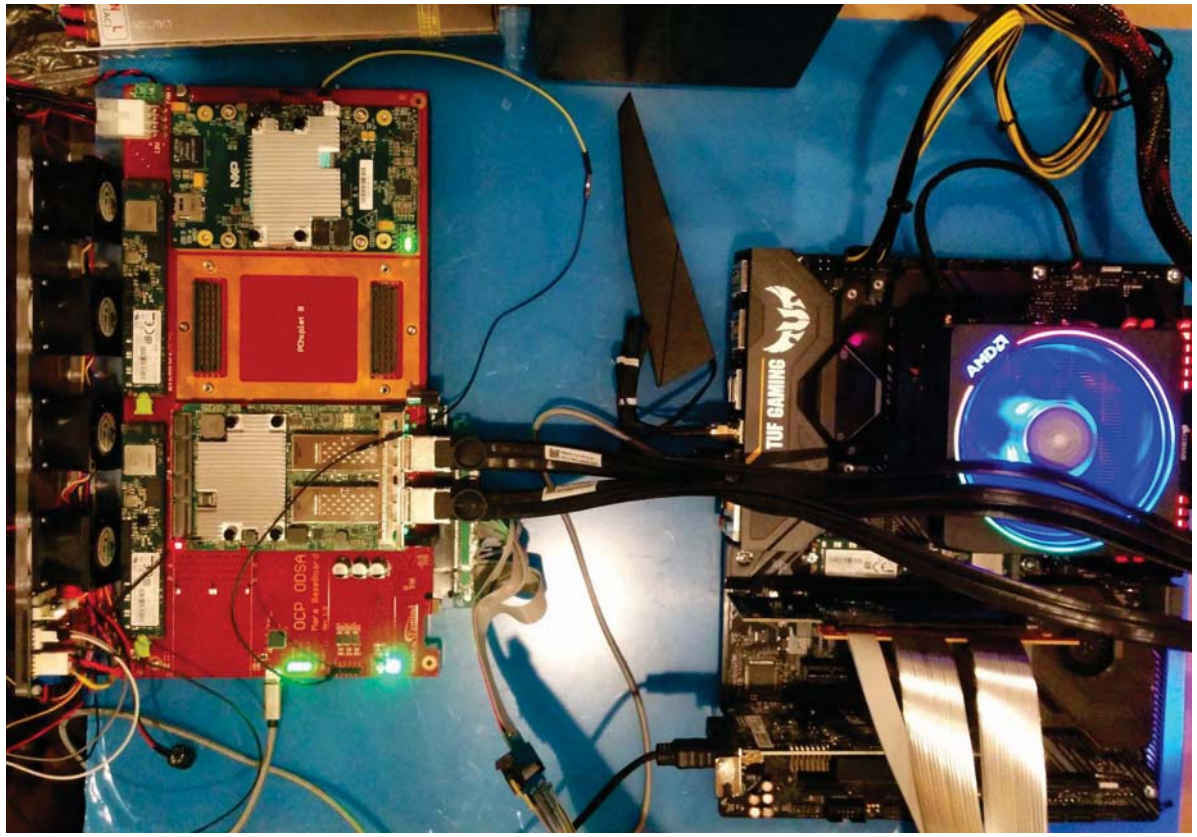


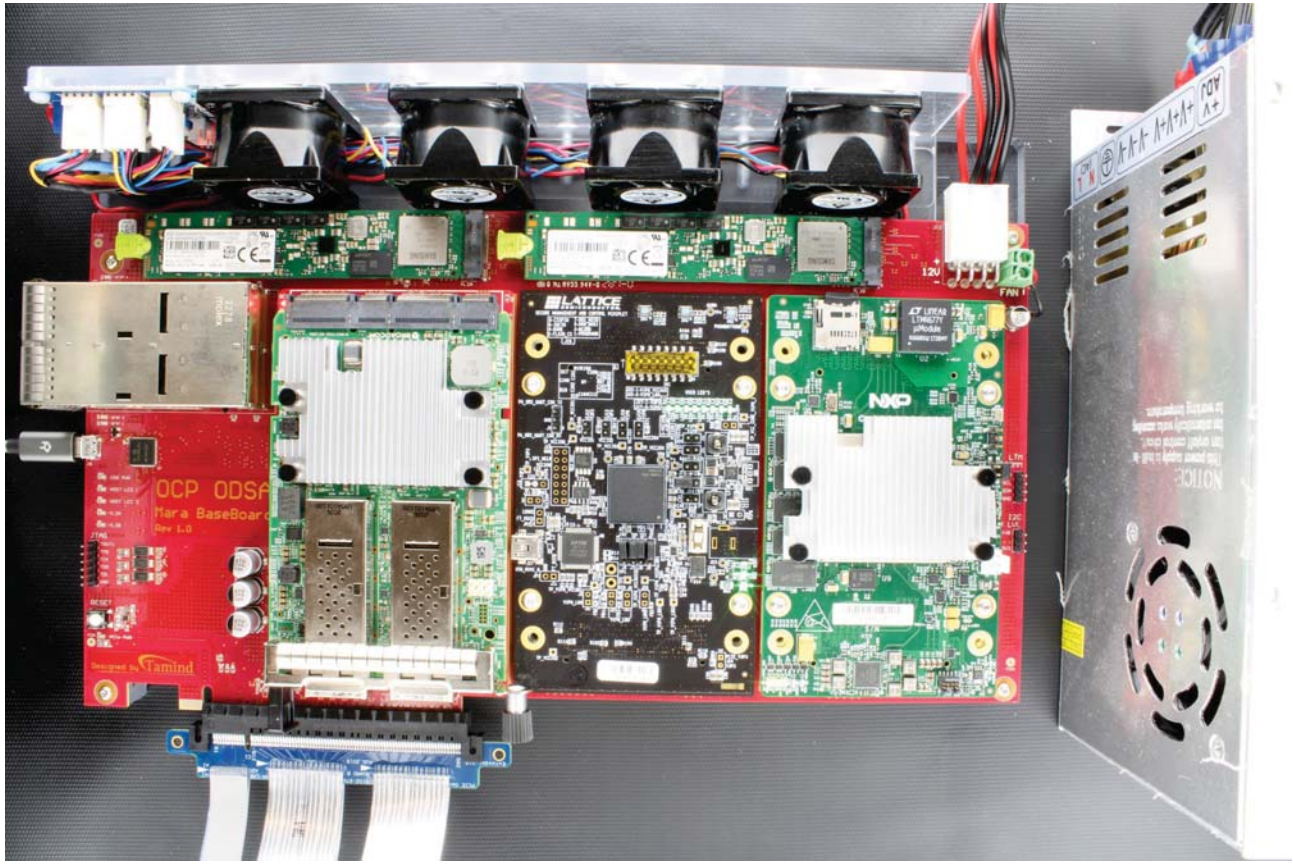
ODSA Accelerator PoC Kit



Design your own Pchiplet, develop an application

ODSA PoC





Storage Acceleration Workshop in August

Tamind

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ODSA Workstreams

Friday General Meeting (8 AM Pacific)

BoW PHY (9 AM Wed) and **Test Chip** (10 AM Wed)

Business Workstream (9 AM Fri)

Chiplet Design Exchange (1:30 PM Thu)

End User Group

Link Layer (9:00 AM Thu)

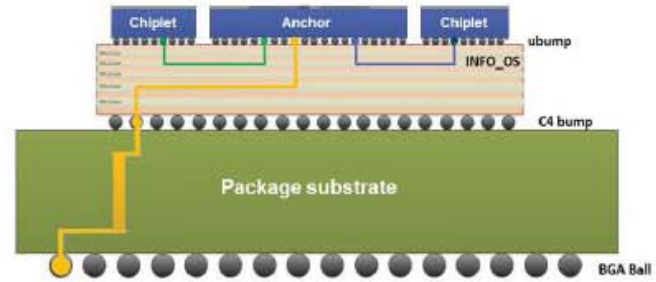
Open HBI

PoC HW and SWI (Tue 8 AM)

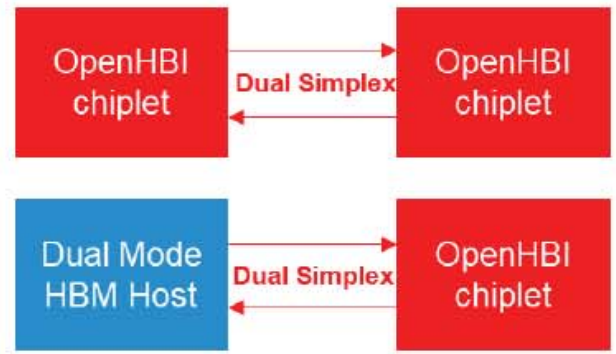
OpenHBI Key Features and Characteristics

OPEN DOMAIN SPECIFIC ARCHITECTURE

- Multi-Tbps chip-to-chip interconnect supporting wafer-level integrated fanout, Si-interposer or similar packaging technologies
- Symmetric, Multi-channel, Scalable C2C interface
- Basic building block is OpenHBI DWORD (Data Word)
  - Up to 42 data signals. With DBI (data bus inversion), Parity, Lane Repair support
  - Configurable Tx / Rx at boot time. Optionally configurable at run time.
- Optimized derivatives and electrically interoperable with JEDEC HBM3 IO with enhanced PPA and FoMs.
  - 8GT/s, up to 3mm reach, < 0.4 pJ/bit
  - Bandwidth density > 1.5 Tbps/mm
  - Raw BER 1e-15. Optional Data Integrity enhancement.
- Multi-layer architecture ease adaption to upper protocol layer
  - E.g,. Protocol adapter (PCIe/CCIX/CXL), ODSA Open Link layer
- Optional Dual-mode OHBI/HBM Host can support OpenHBI chiplet as well as HBM3 memory chiplet



E.g., Anchor & Chiplets on WLFO



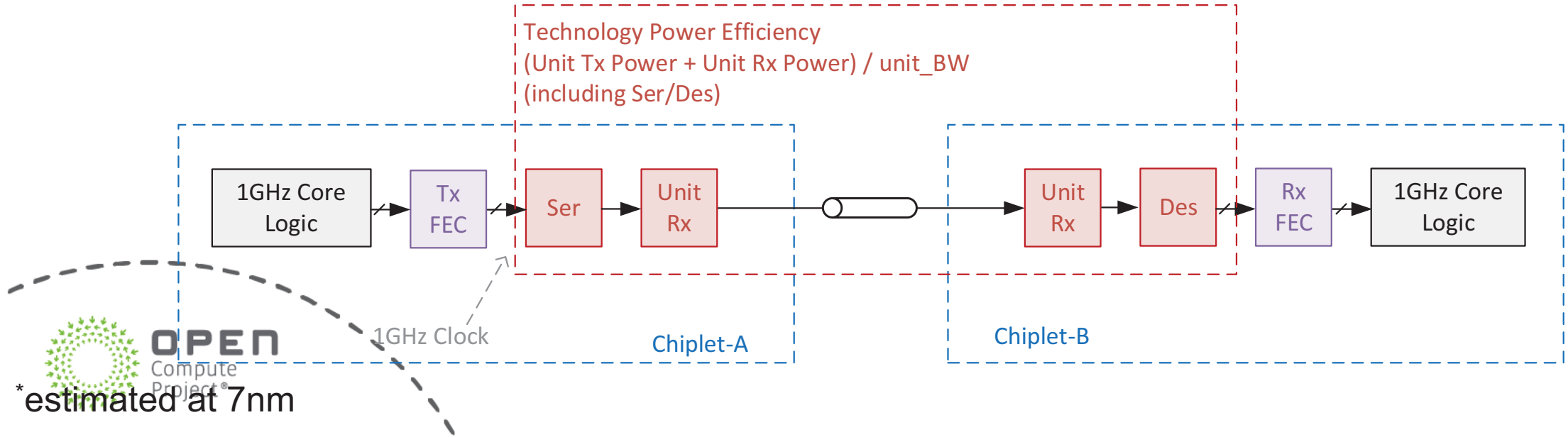
2020 Revision of D2D PHY Comparison

Metric	Impact	2019 Components	2020 Adds
Piece Cost per Unit	Manufacturing cost/complexity	Pad-limited area Substrate	
Operating Cost	Power-performance at rated throughput	Figure of Merit (Tb/mm)/(pJ/bit)	FOM2 = FOM/reach Latency at 1GHz logic at 1E-15 BER
~~Product Risk~~ Design Impact	Chiplet/product design NRE/schedule risk	Routing Freedom ~~Low power states~~ Process Node Diversity IP Integration Complexity Production test/assembly	
~~Interface Risk~~ Product Integration	Interface technology NRE/schedule risk	Licensing Fee ~~Multi-sourcing~~ Interface test, assembly IP dev/port complexity	Open standard

Section 2b: On-die parameters*

Performance:

Unit bandwidth (unit_bw) in each direction	Gbps	(speed_per_data_lane) *(num_data_bits) Examples: BoW: 16*5 = 80Gbps XSR: 112 X 1 = 112Gbps
Unit Power (Tx+Rx+Clock)	mW	Tx, Rx and Clocking power [mW/Gbps X unit_BW in Gbps] Example BoW: 80Gbps X 0.5mW/Gbps = 40mW XSR: 112Gbps X 1mW/Gbps = 112mW

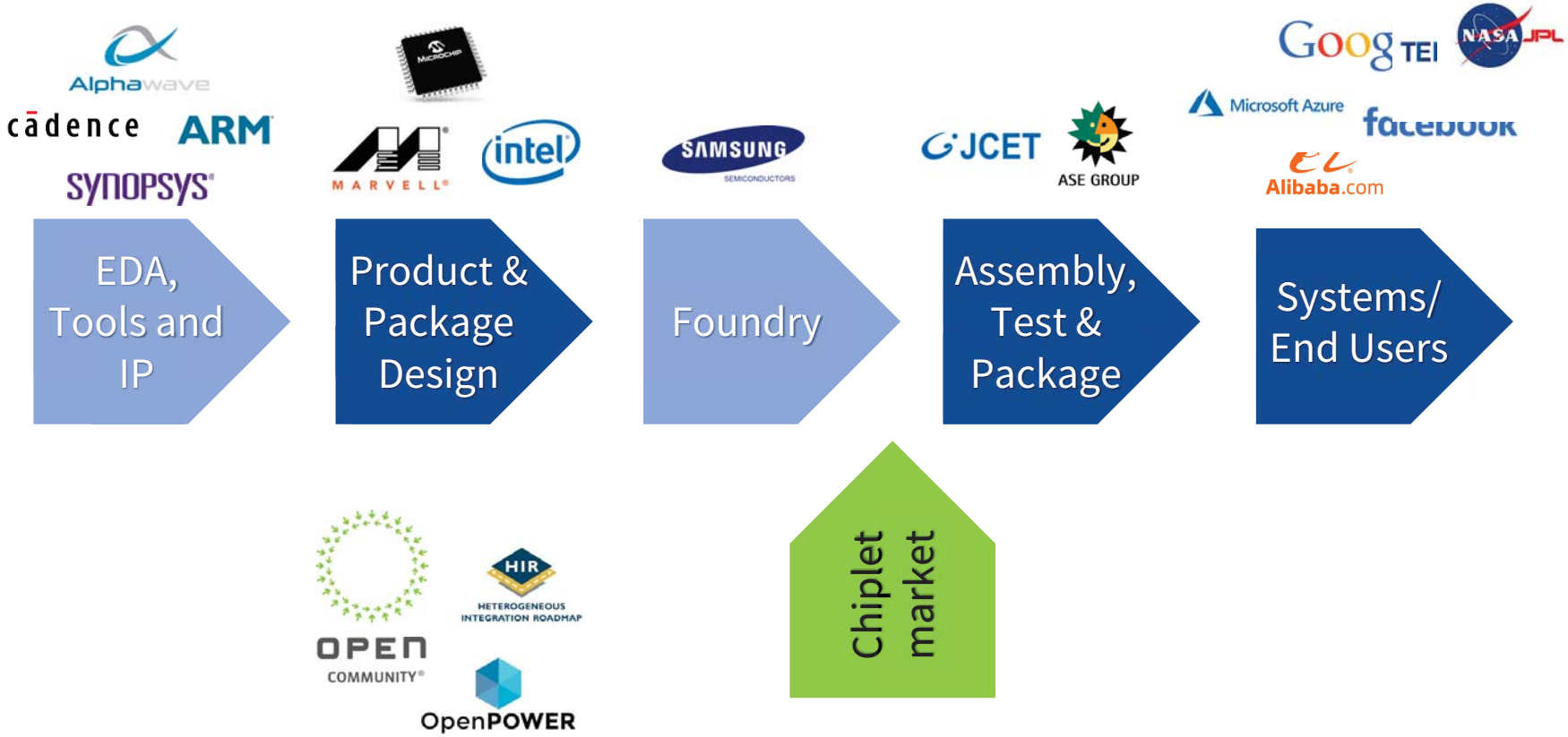


*estimated at 7nm

Performance Comparison

	Pump Space [um]	Power Efficiency [pJ/bit]	Edge Density [Tbps/mm]	Area Density [Tbps/mm^2]	FOM-1: Edge_Density/Power_Eff. [Tbps/mm / pJ/bit] Larger is better	FOM-2: Power Efficiency per Reach [pJ/bit / mm] Smaller is better
AIB 2.0	55	0.5	1.64	-	3.28	0.1
Open HBI 1.0	40	0.4	2.29	2.04	5.71	0.1
Open HBI 1.1	40	0.5	3.34	3.06	6.86	0.06
BoW- Basic / C4	130	0.5	0.27	0.22	0.55	0.05
BoW- Fast	130	0.55	0.88	0.69	1.59	0.01
BoW- Basic / Micro	40	0.5	1.78	1.07	3.56	0.1
AQ LinkP	130	0.55	1.91	1.46	4.48	0.01
AQ LinkB	40	0.5	3.56	2.13	7.11	0.01
AX-C2C	130	1.5	1.09	0.27	0.73	0.01
AX-DieIO	130	0.8	2.19	0.4	2.74	0.01
Kandou / CNRZ-5	130	1	1.33	0.67	1.33	0.02
XSR /Alphawave	130	1	3.98	0.51	3.98	0.02
PCIe Gen5	150	7	0.22	0.1	0.03	0.05

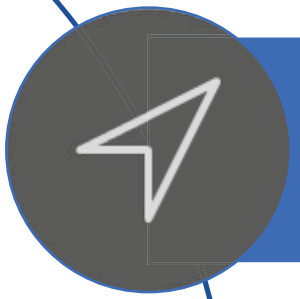
Chiplets Business Workshop



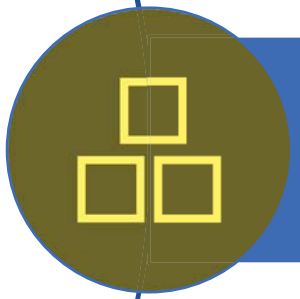
How do we make a marketplace:

- Impact of chiplets
- Many participants from the value chain
- Panels + talks
- Centered around building a reference product from a marketplace

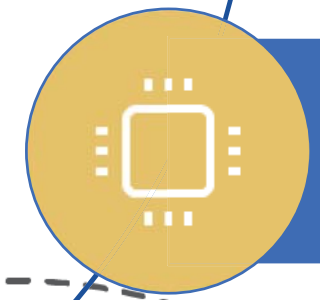
End User WG: Create Consumable Innovation



Drive requirements in a unified manner



Support development efforts



Consume chiplets and SIPs

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Microsoft

facebook

Alibaba Cloud

Google

Please Help, Join Us!

OPEN DOMAIN SPECIFIC ARCHITECTURE

- A full D2D stack + software platform available
- Join a work stream, each meets weekly
- Help with the PoC, software, use case dev
- Review, help complete documents in flight
- Need packaging and test definition and work streams
- Make chiplets with, IP for, the open ODSA stack
- https://www.opencompute.org/wiki/Server/ODSA
- Join us at the OCP Fall Summit

SERVER

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