Road to Chiplets: Architecture

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HETEROGENEOUS INTEGRATION ROADMAP

Making Chiplet-based Systems Reliable:

Approaches to Support Heterogeneous Integration

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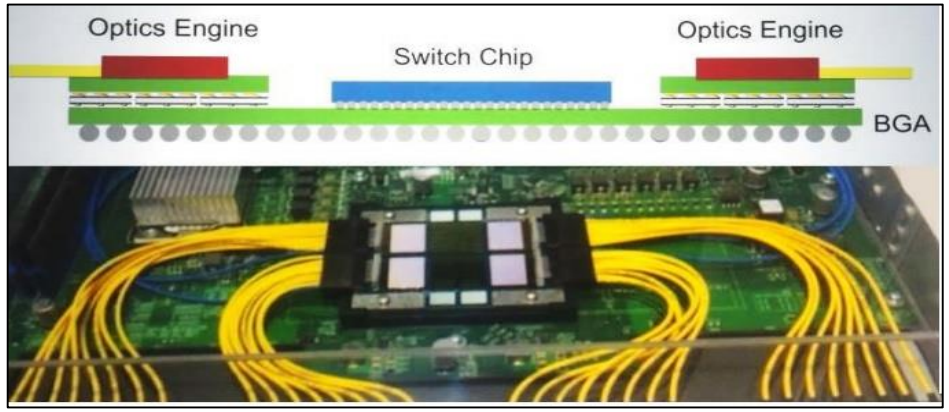
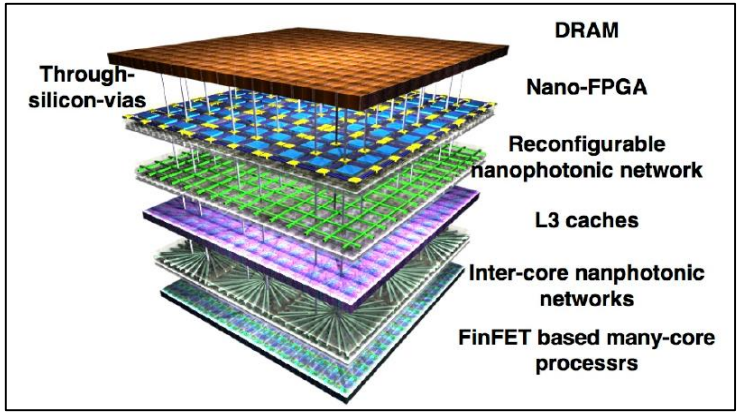
Acknowledgment:
Richard Rao (Marvell Corporation), Shubhada Sahasrabudhe (Intel)

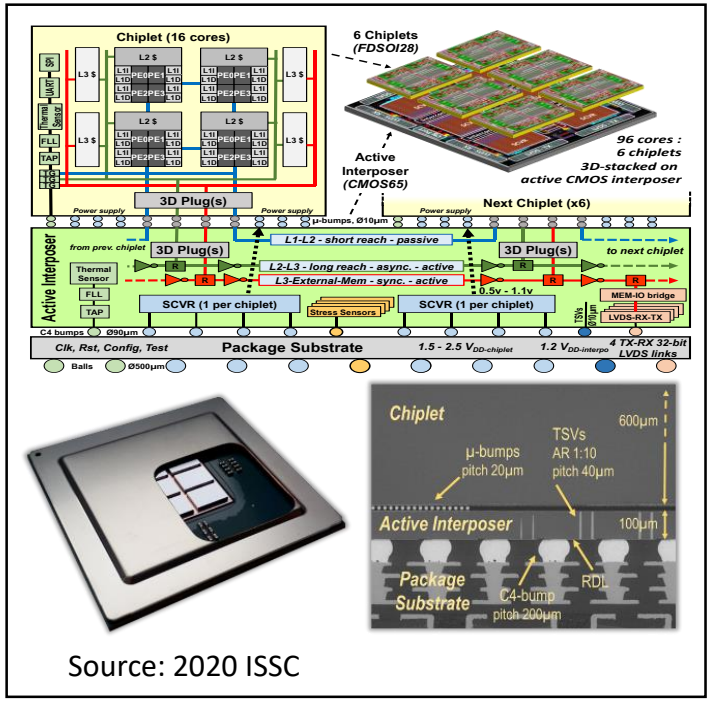
Chiplets are a critical building block in heterogenous integration:

HETEROGENEOUS INTEGRATION ROADMAP

- Electronic (Passive/Active)/photonic/MEMS/Sensor devices
- Digital; Analog; Logic; Memory; Power; RF
- System, Package (Chiplets) and Wafer levels, including Interconnects and Substrates
- 2.5D and 3D Packaging technologies





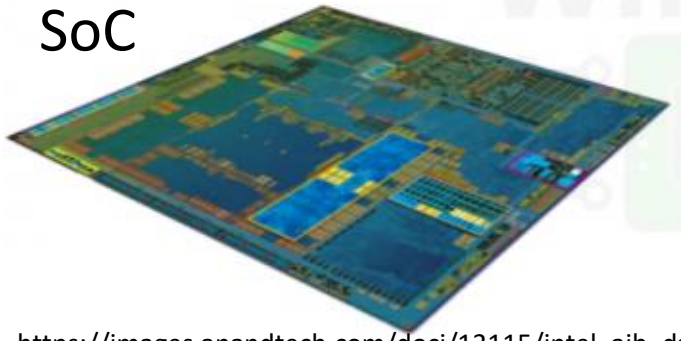


Source: 2020 ISSC

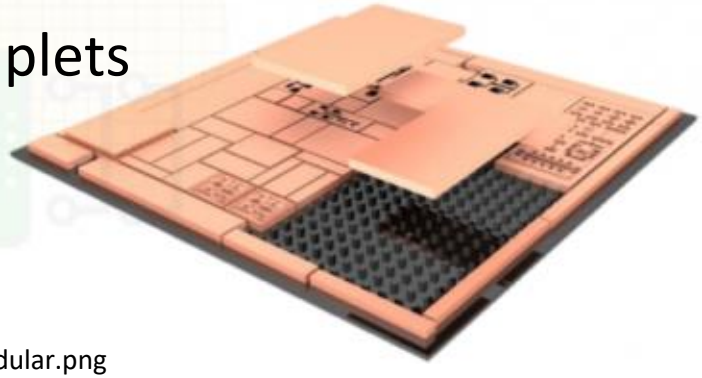
Chiplet architectures bring unique reliability issues

HETEROGENEOUS INTEGRATION ROADMAP

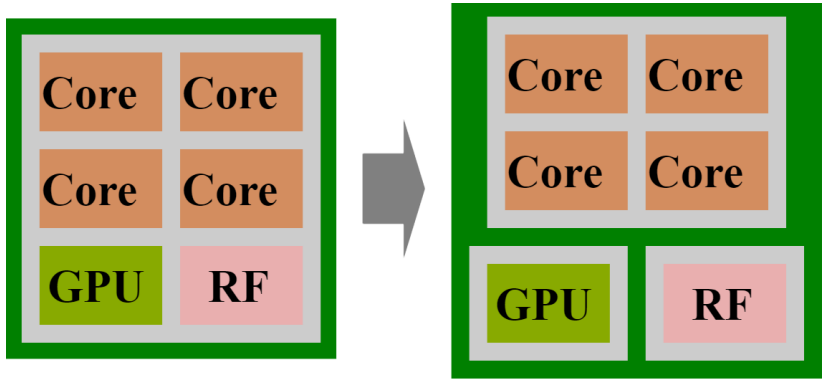
Monolithic SoC

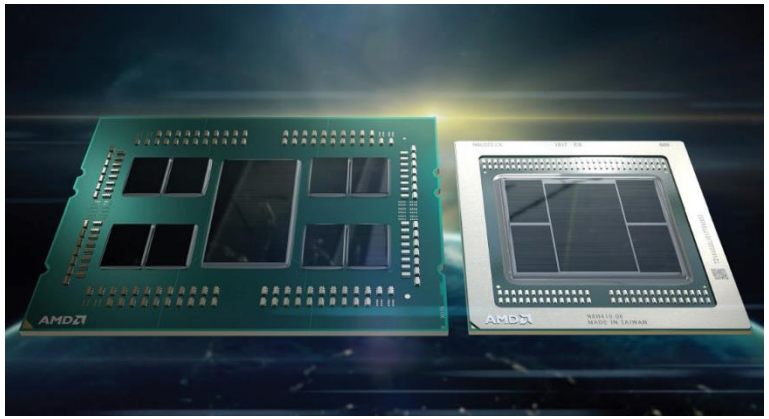


Modular Chiplets

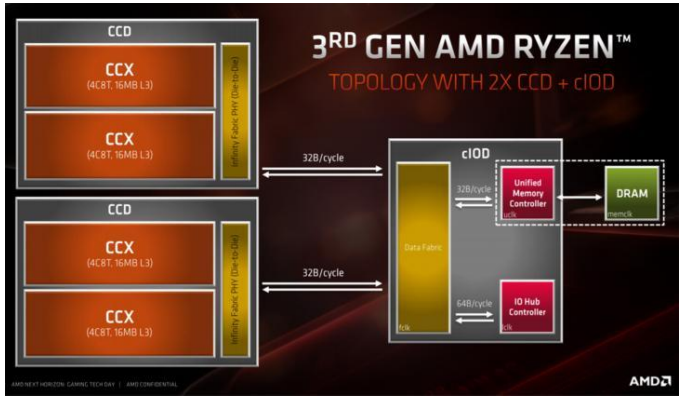


https://images.anandtech.com/doci/13115/intel_aib_darpa_modular.png



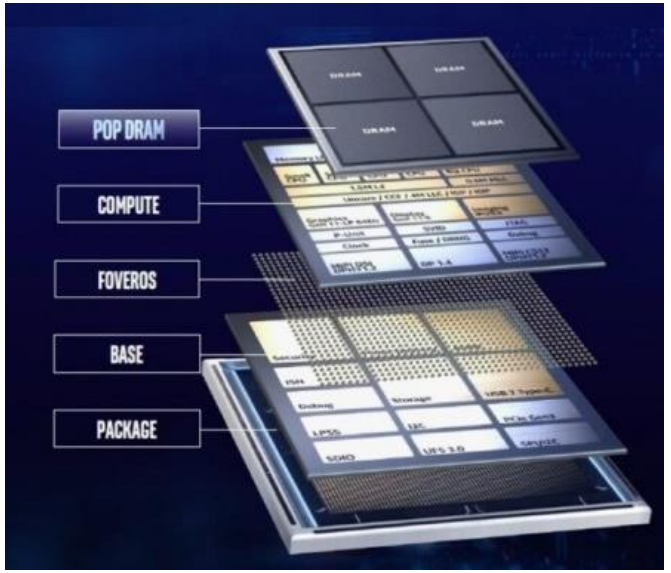


AMD



https://www.hardwaretimes.com/difference-between-intel-and-amd-ryzen-processors-chiplet-vs-monolithic/

Intel

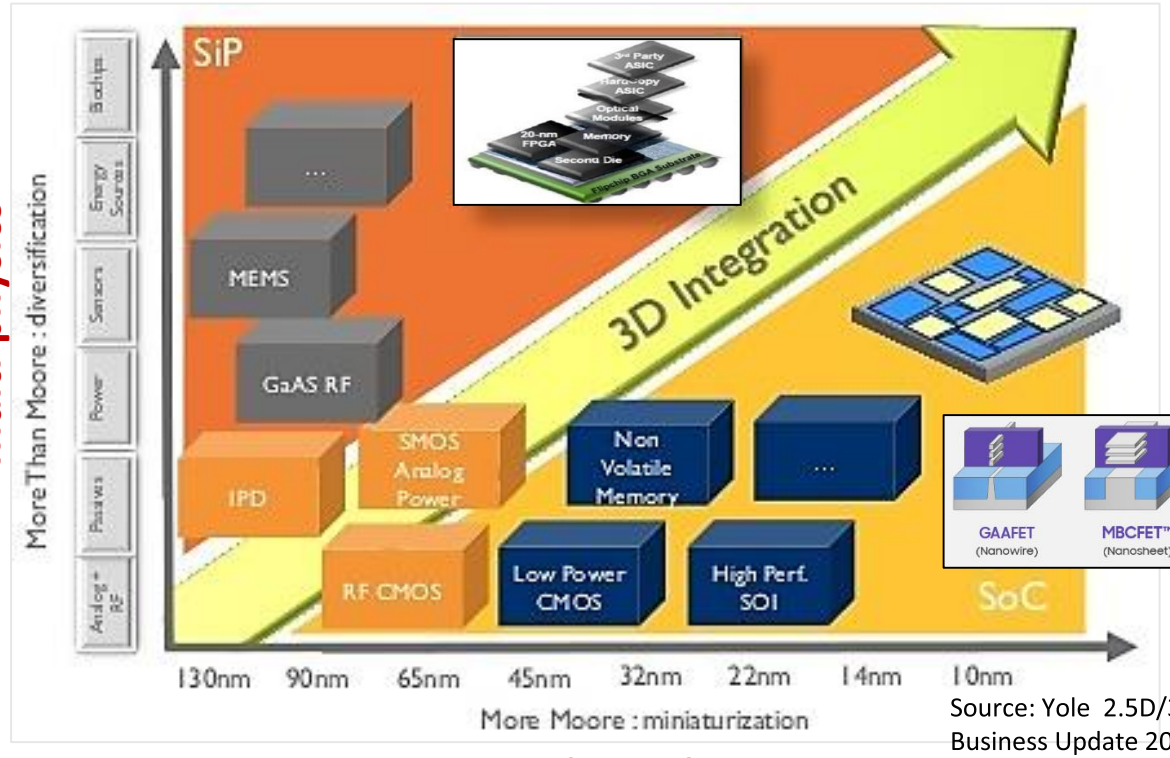


Chiplet-Based Systems: Convergence of Semiconductor & Packaging (Disaggregation and Re-aggregation)

Approach for reliable chiplet architectures

HETEROGENEOUS INTEGRATION ROADMAP

Multi-physics



Source: Yole 2.5D/3D Business Update 2015

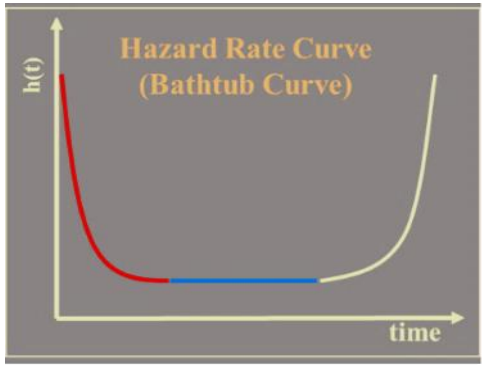
Multi-scale

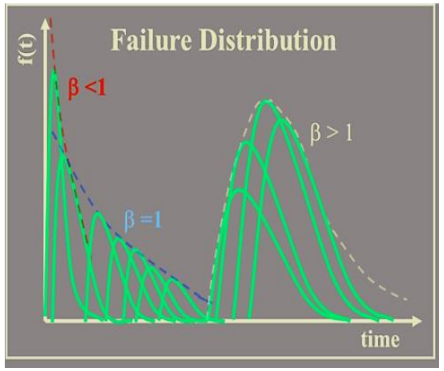
Convergence of Semiconductor and Packaging Industries

Heterogeneous chiplets:

- **technology** (IC-node, photonics, MEMS, sensors)
- **circuit type** (DRAM, Serdes and logic, photonics, power, RF)
- **packaging** (substrate, interposer and interconnect method)

Reliability Assurance Activities





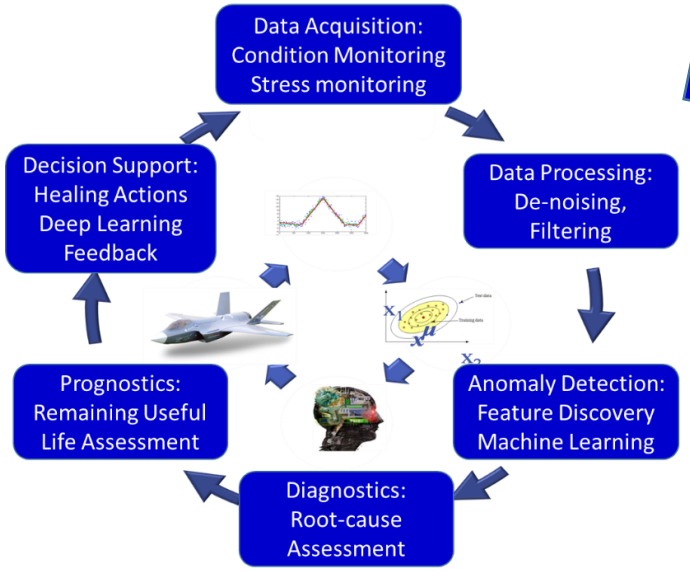
Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability
Knowledge based Testing for Qualification	Product Health Management	Supply chain Integration	

Reliability of multi-physics/multi-scale HI systems requires holistic cradle-to-grave methodology

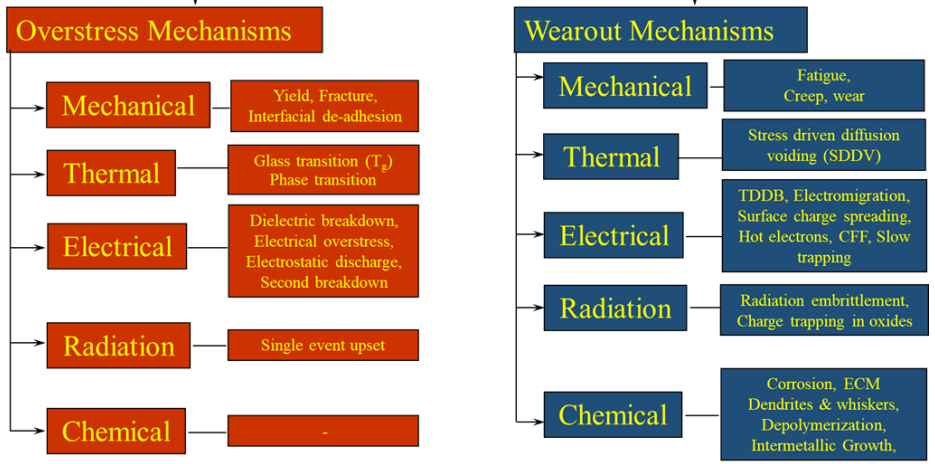
Chiplet reliability

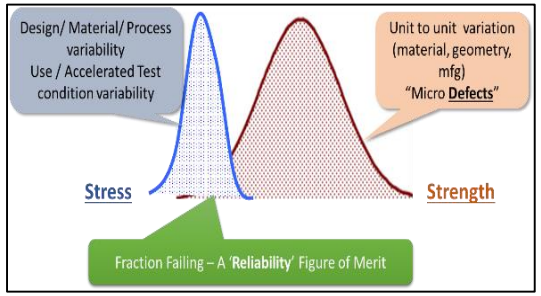
HETEROGENEOUS INTEGRATION ROADMAP

Prognostics and Health Management



Degradation and Failure Mechanisms





Fusion of bottom-up physics and top-down AI approaches

Machine Learning & Artificial Intelligence

Condition Monitoring
Sensors
Data-analytics

AI-based Degradation Analysis
Machine Learning, Deep Learning
Feature Extraction
Anomaly Detection
Neural Net Diagnostics

Reliability 'Digital Twins'

Fusion Prognostics
Remaining Useful Life (RUL)

Life Consumption Monitoring
Usage sensors
Canaries

Reliability Physics (RP) Models + Expected Future Use Conditions

RP-based Damage Accumulation Estimation

Reliability Physics

Reliability Functions in Product Lifecycle

Proof of Concept

- New Si and Packaging Technology Understanding
- Feature/performance
- Reliability data collection
- **Anticipate new failure modes/mechanisms**
- Identify Reliability Risks/FMEA

Technical Feasibility

- Usage stress conditions
- Reliability targets
- Customer engagement
- Reliability/CPI/BLR Risks Evaluation
- Test Vehicle Design and Corners
- Eng Verification DOE
- Deliver Reliability Design Rule and aging model
- IP Reliability
- Soft errors

Development/ Design

- **Design Verification**
- **Implement reliability solutions in the design flow**
- Review and assess any violations/trade offs

Design for Reliability

Product Qual

- Optimize assembly process and materials
- Reliability hardware/dynamic vector/models
- Stress based Qualification
- Knowledge based qualification

HV Production

- Early failure rate
- Reliability monitoring
- Solve field reliability fails
- Track field failure rate

PHM

- Monitor the health of products in field
- Adapt voltage to compensate aging
- Replace failed interconnect

Designing for reliability: Reliability-physics process

HETEROGENEOUS INTEGRATION ROADMAP

INPUTS

Hardware configuration
materials, geometry, architecture

Life Cycle Loading

Operational Loads
Power dissipation, voltage, current, frequency, duty cycle

Environmental Loads
Temperature, relative humidity, pressure, shock. The life cycle includes transportation, storage, handling and Application environments

ANALYSIS

Multiphysics "Stress" Analysis
Estimate stresses at failure sites under life-cycle loading:
- Thermal
- Thermo-mechanical
- Vibration-shock
- Hygro-mechanical
- Diffusion
- Electromagnetic

Reliability Margins
Estimate design margins for each relevant failure mechanism due to stresses at each failure site:
- stress margin for overstress mechanisms
- life margin for wearout mechanisms

Aggregation to the System Level
Develop reliability block diagrams
Use Monte Carlo simulations
Use Bayesian updates with field/test data (if any)

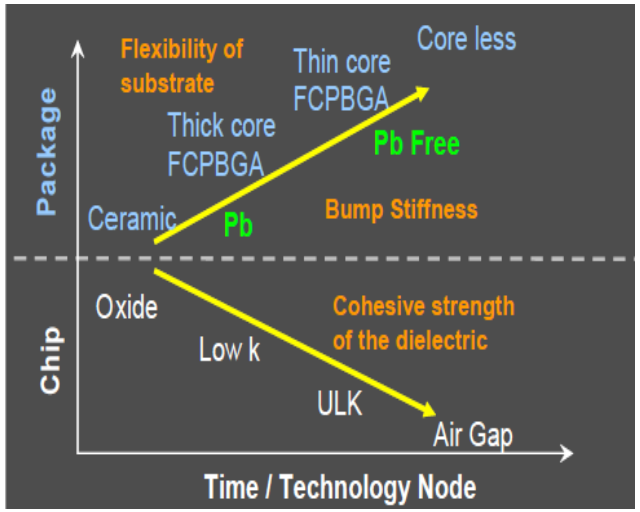
Sensitivity Analysis
Evaluate sensitivity of the product durability to changes in: application, design, manufacturing window, life-cycle support methodologies

OUTPUTS

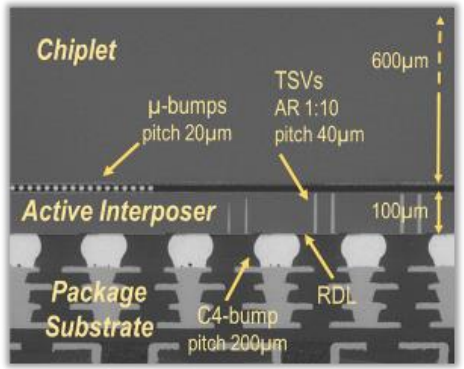
- Ranking of potential failure mechanisms and sites
- Design tradeoffs
- Risk mitigation solutions
- Accelerated test conditions
- Reliability Assessment
- Health Prognostics

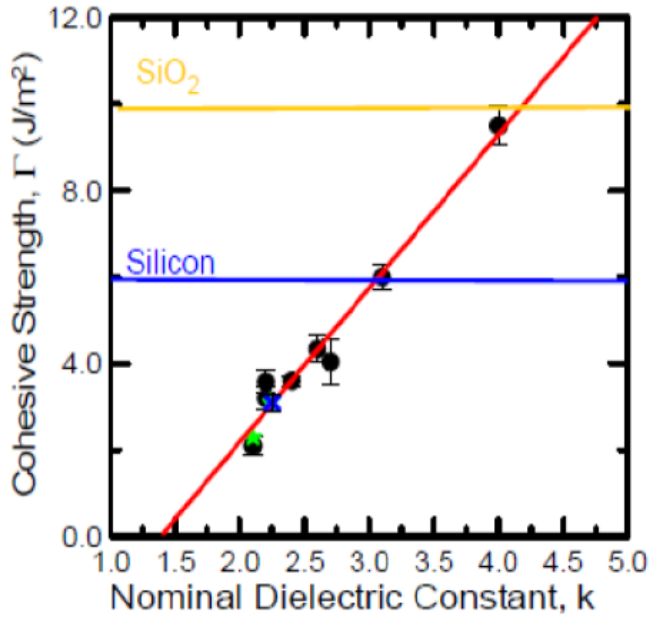
Advanced chiplets: CPI challenges

- CPI issues are increasing with newer Si nodes
  - Device and packaging reliability were treated separately in old nodes
  - Advanced Si with low k, CPI requires co-development of device and package
- Low k and Ultra low k introduction
  - Fragile and poor adhesion
- Build up substrate
  - High CTE and warpage
- Pb free or Cu pillar interconnect
  - Higher modulus
- Complex die
  - Big die size
  - Higher power
- Bump on trace
- More advanced packaging induced board-chip-package interaction
  - WLP
  - 2.5D/3D
  - Big FCBGA



HETEROGENEOUS INTEGRATION ROADMAP



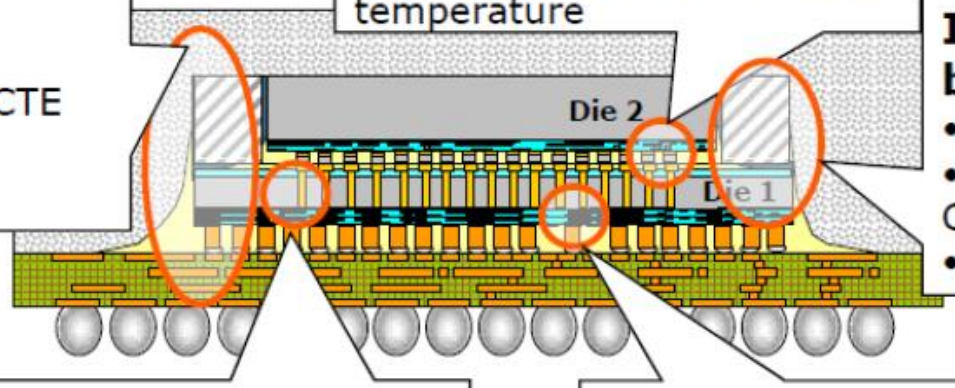


Chiplets: An overview of 3D IC stresses and reliability

HETEROGENEOUS INTEGRATION ROADMAP

Impact of Flip Chip Package on 3D chip-stack (CPI)
- Stress induced by Cu-pillars on low-K
- Stress induced by overmold, laminates CTE mismatch
- …

Impact of TSV/uBump on top die
- Built-in stress
- Stress varies as function of temperature

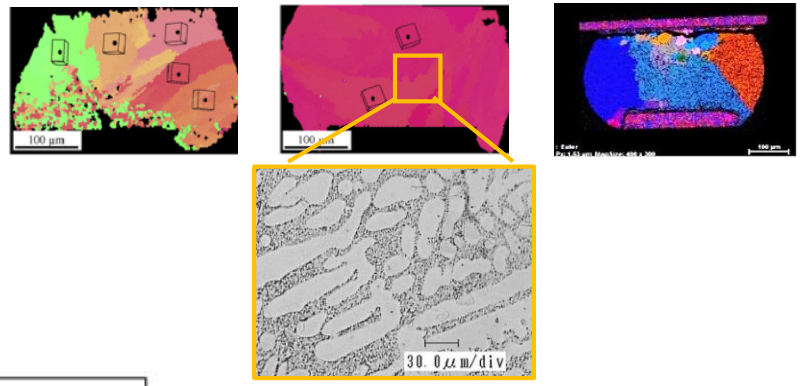


Impact of 3D-SIC bonding on dies
- Stress during bonding
- Stress due to underfill CTE mismatch
- …

Impact of die thinning
- Releases stress
- Strength of die
- …

Impact of TSV on bottom die
- Built-in stress
- Stress varies as function of temperature
- …

Microbumps:
- Material anisotropy
- Length-scale effects



Stress/strain can lead to
- mechanical failures due to delamination, peel, fatigue, …
- electrical impact due to parameter shifts, increased variability, EM,…

Multi-scale

Source: IMEC

SHE-induced FEOL failure modes

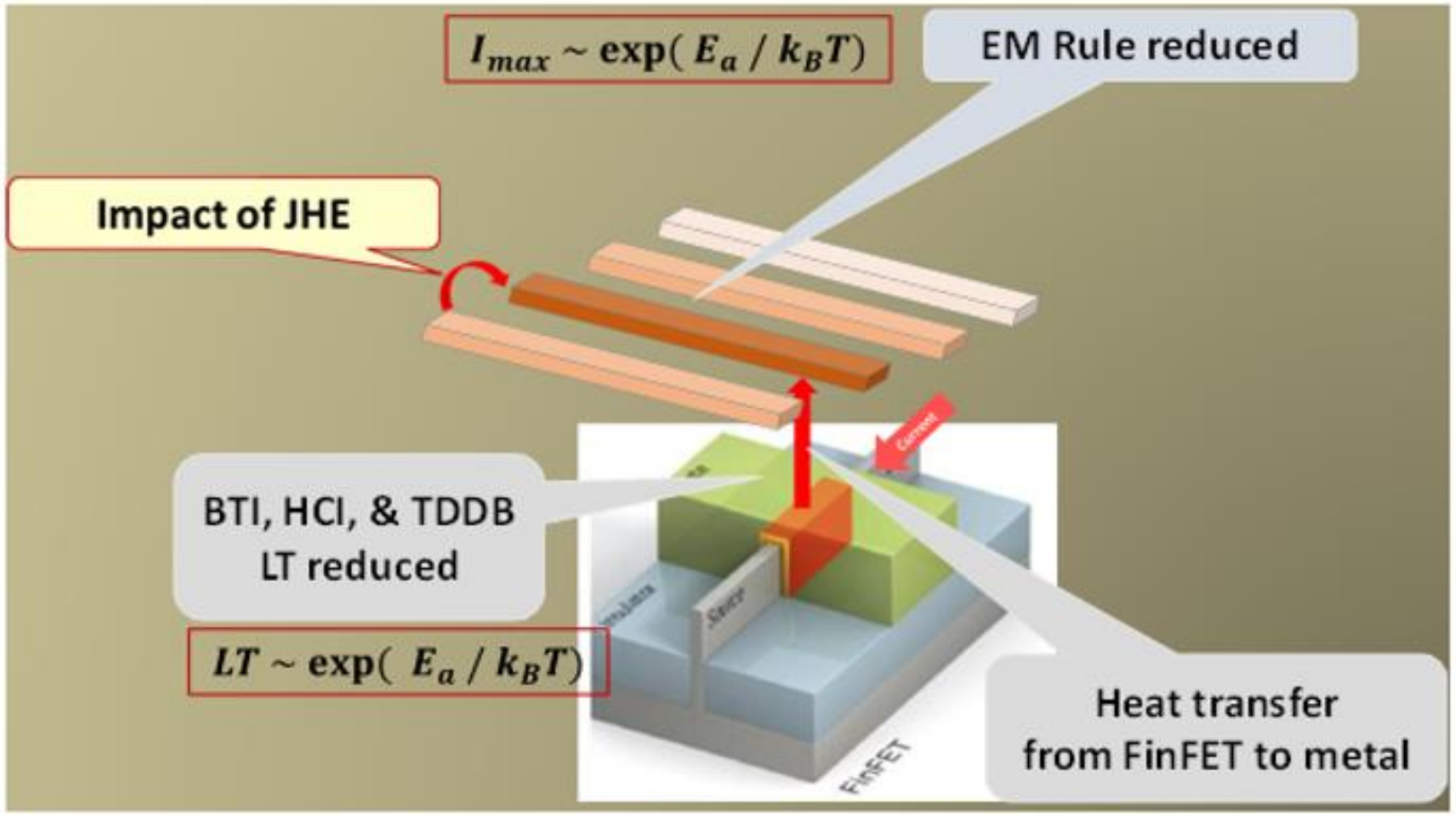
HETEROGENEOUS INTEGRATION ROADMAP

Electromigration

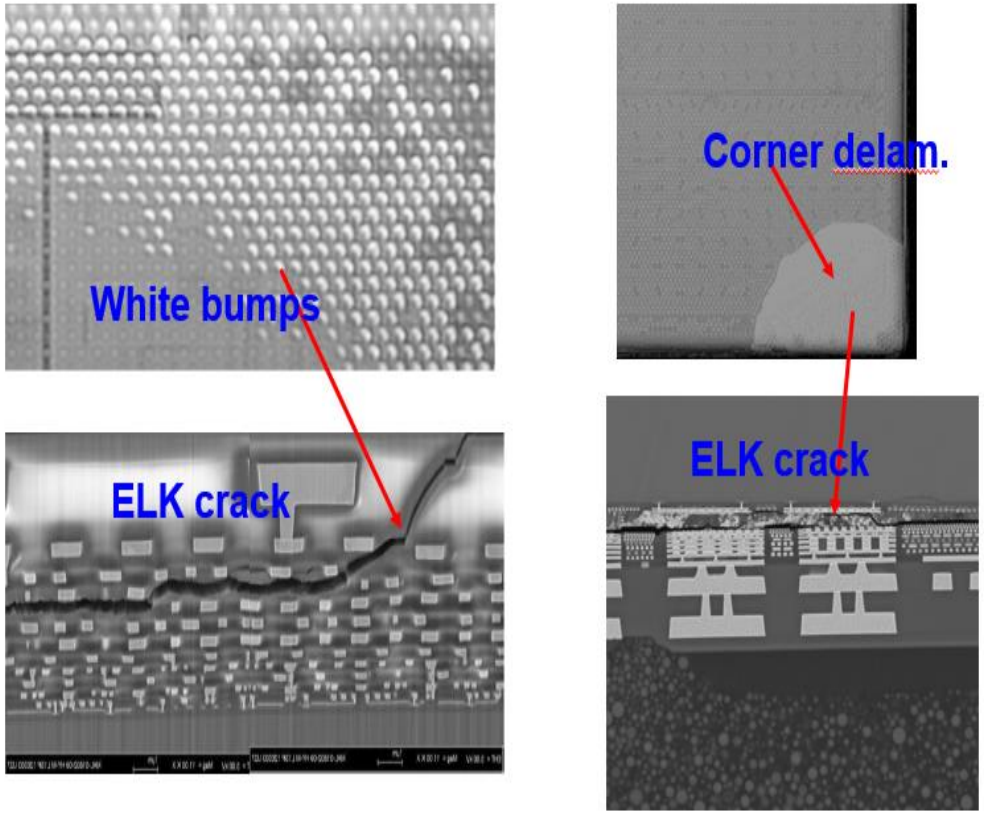
Bias Temperature Instability

Hot carrier Injection

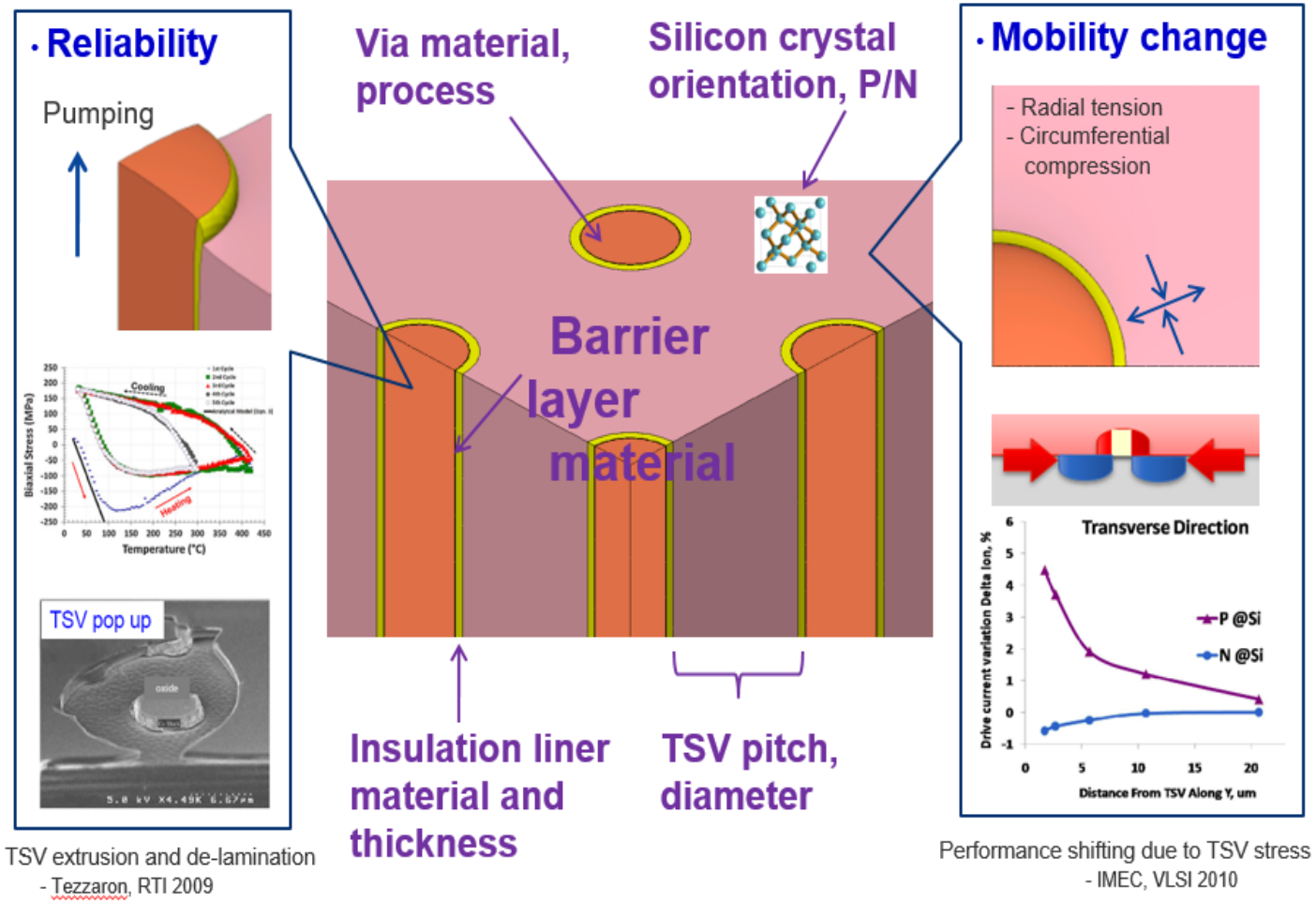
Time-Dependent Dielectric Breakdown



Typical CPI-induced MEOL/BEOL failure modes



Source: IBM

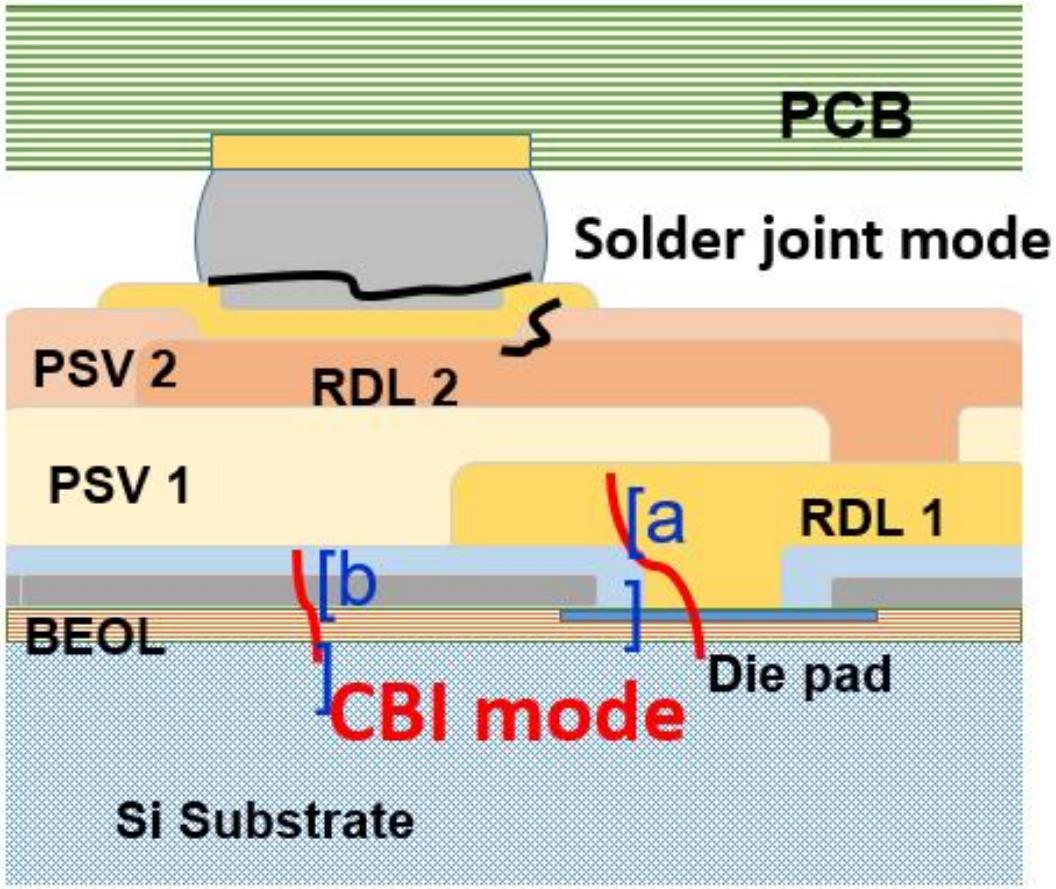


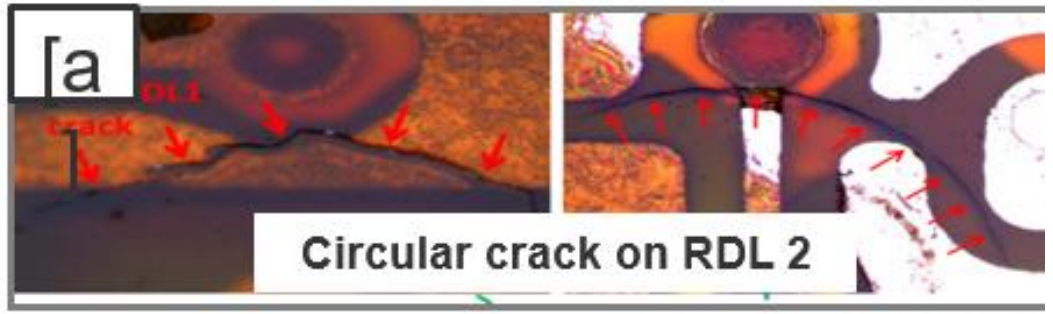
TSV extrusion and de-lamination
- Tezzaron, RTI 2009

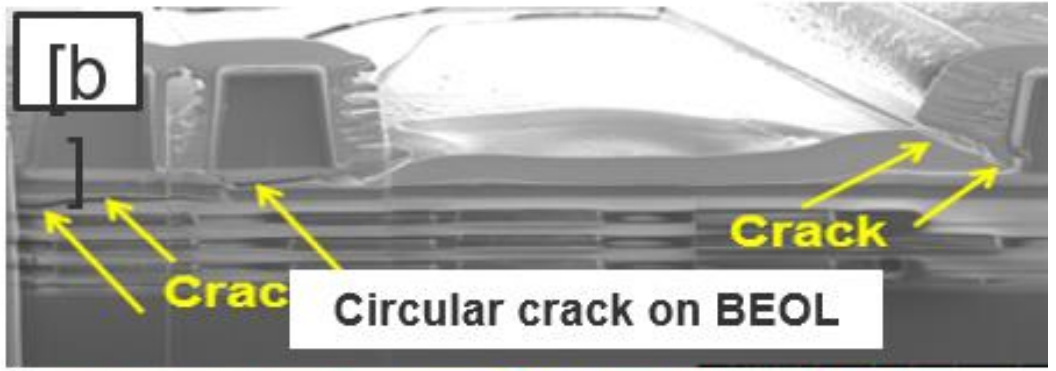
Performance shifting due to TSV stress
- IMEC, VLSI 2010

Source: Synopsys

CBPI-induced failure modes



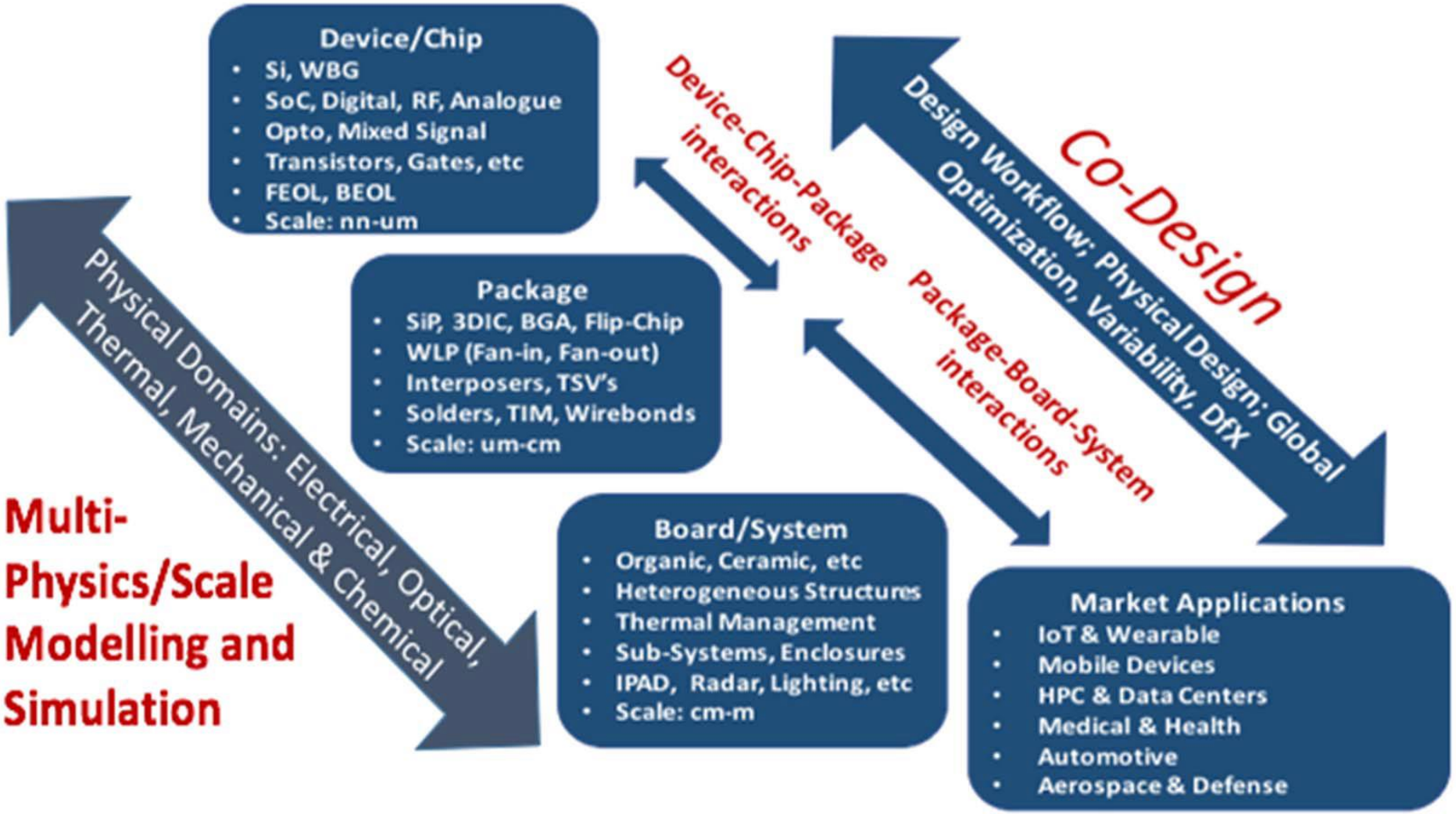




Meditek, 2017 IRPS

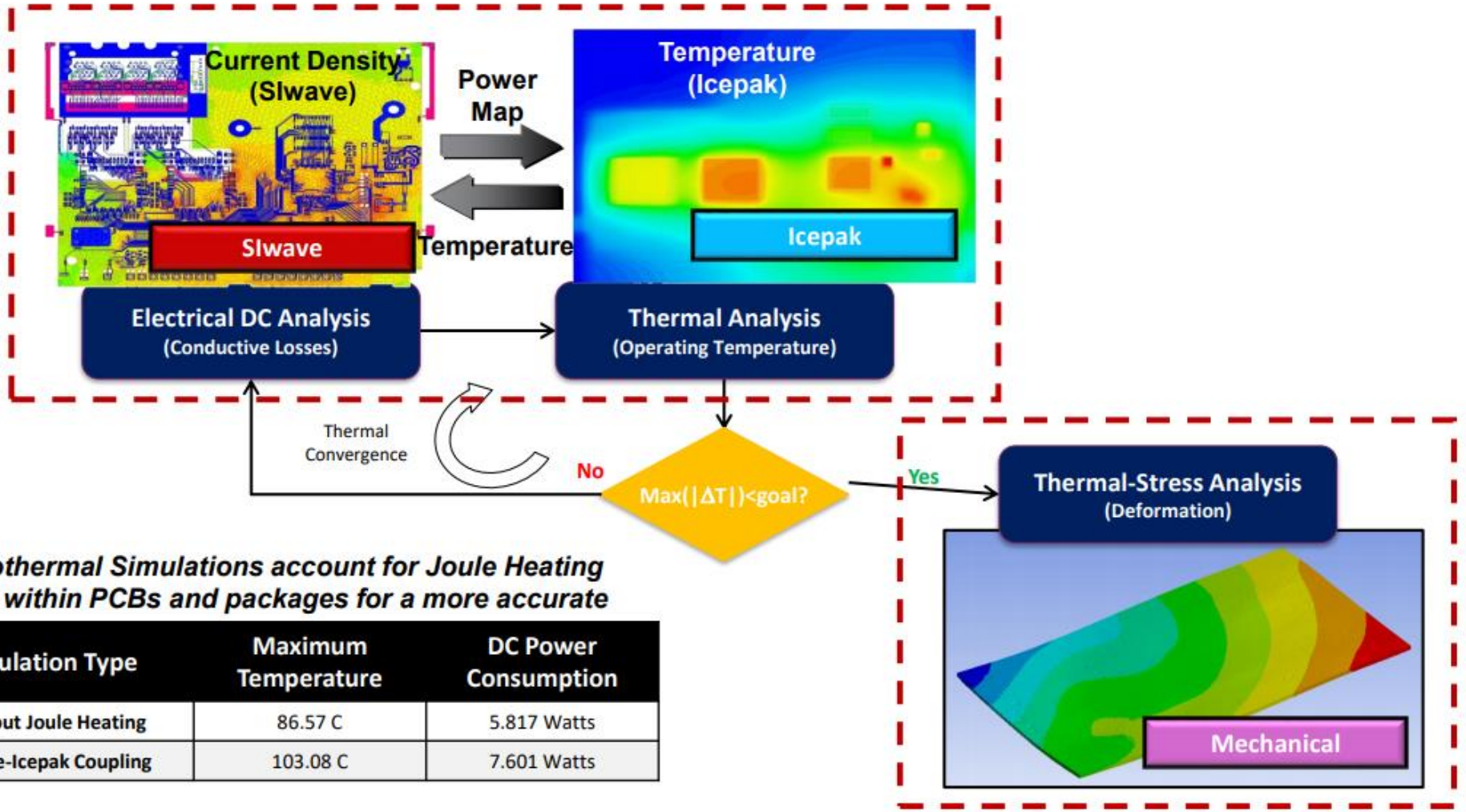
Chiplets: Physics-based modeling simulation and co-design

HETEROGENEOUS INTEGRATION ROADMAP



Source: HIR; Modelling and Simulation TWG

System-level multiphysics simulations



Electrothermal Simulations account for Joule Heating losses within PCBs and packages for a more accurate

Simulation Type	Maximum Temperature	DC Power Consumption
Without Joule Heating	86.57 C	5.817 Watts
SIwave-Icepak Coupling	103.08 C	7.601 Watts

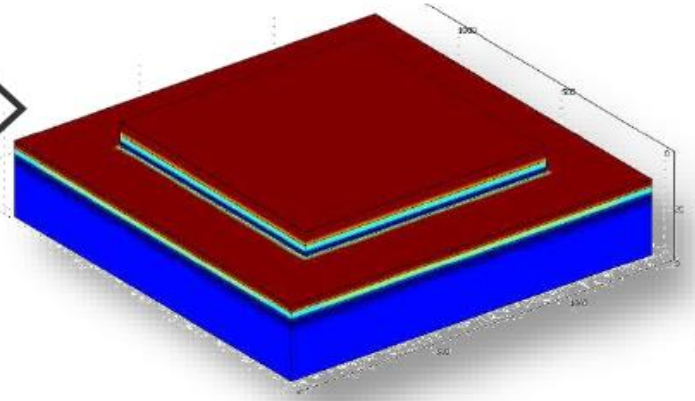
Source: ANSYS

Multi-scale and multi-physics CPI flow

Package-scale simulation (FEA)

Input: geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

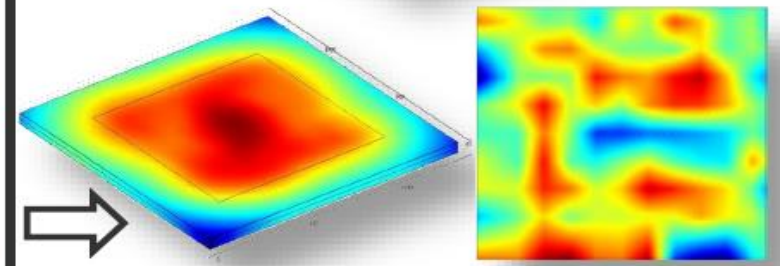
Output: field of displacement components on the die faces.



Die-scale simulation (FEA)

Input: geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

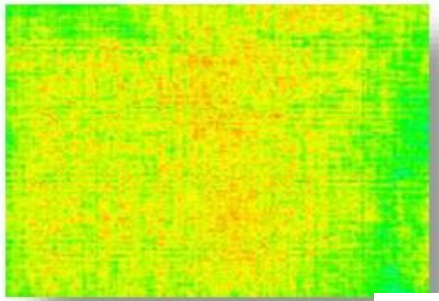
Output: Distribution of the strain components across device layer.

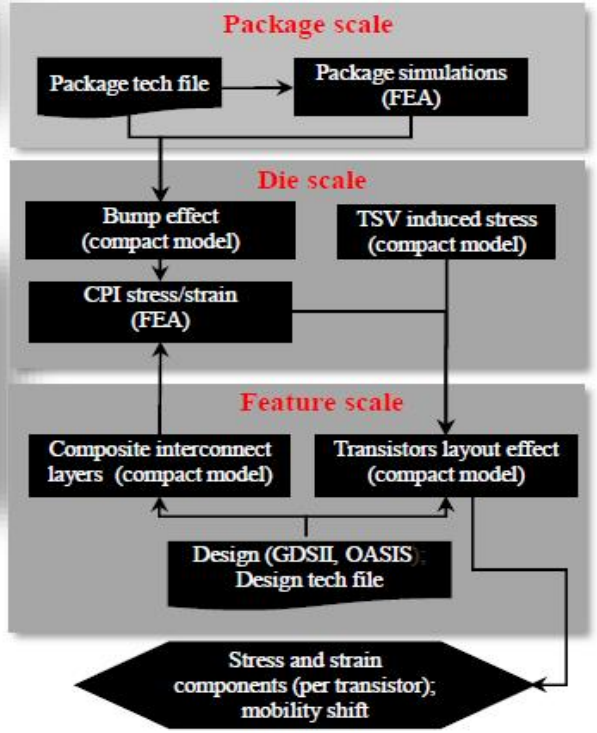


Layout-scale w/feature-scale resolution (compact model):

Input: GDS; distribution of the strain components across device layer.

Output: Transistor-to-transistor variation in stress components





Source: Mentor Graphics

Modes/Mechanisms/Models for Degradation & Failure

HETEROGENEOUS INTEGRATION ROADMAP

Electrical Thermal Moisture Thermo-mechanical Mechanical DfR Methods MfR Methods

Multiphysics

Multiscale

Devices

Interconnects

Packaging/ System

Module/System

Multiscale Integration	Multi Physics	Electrical Stress		SI/PI (Electrical Performance)	Thermal Analysis	Moisture		Thermal Mechanical Stress		Mechanical Stress		Thermal Interaction with SI/PI	Stress Interaction with SI/PI	Simulation/Modeling and Co-Design Flows		PDK/ADK	Manufacturing Variability	Material Property and Variability
		Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models	Failure Modes	Failure Mechanism and Reliability Models			Failure Modes	EDA flows			
Transistor	FinFET and GAA	Leakage current, ripple currents, unstabel performance and ESD	N/PBTI models with recovery; HCI model; TDDB Weibull model; Oxide & junction breakdown model	Transistor SPICE	FinFET SHE	No known failures	None	FinFET SHE channel stress; µBump/C4 bump/TSV; system level stresses	FinFET SHE Models; CPI Model; Piezo-electrical models	No known failures	None	SHE effect on SPICE parameters	Influence of SI stress on SPICE parameters	Effects of degradation mechanisms and process variabilities on electrical functionality	Cadence; Reixpert; Mentor Graphics	Integrate of degradation models into Device SPICE Model		
Interconnects	MEOL/BEOL Metal/Via /ELK	Electromigration; Inter Layer Dielectric ELK Breakdown; MEOL Oxide Breakdown; EOS	Electromigration model; Dielectric breakdown model	Extraction of RLC Model	Joule Heating simulation; SHE effects on MEOL/BEOL	Pad and underline metal corrosion; Cu/ELK delamination 3. Cu loss/diffusion	Electrochemical corrosion; Interface degradation due to moisture absorption; Barrier metal oxidation	SHE failure in Cu/ELK, MEOL, BEOL, µBump, TSV; RDL failures from package stress, Cu fatigue; Low K/ELK layer cracking & delamination	Creep induced voiding; CTE mismatch; SHE induced localized thermal cycling	Low K/ELK layer cracking & delamination	Fatige by bending	Joule/SHE temp effects on RLC	Effect of Cu/ELK stress on RLC	CPI Induced Cu/ELK cracking; JHE/SHE stresses; stress from bumps/TSV/RDL & Packaging	Ansys Mentor			
	FBEOL RDL/Dielectric	RDL/UBM Electromigration	Electromigration	Extraction of RDL RLC Model	BEOL Joule/SHE effect on RDL temperature	Cu dedrite	Electro-chemical corrosion	RDL cracking	µbump/TSV/ Package/ Board effects on RDL stress			Effect of RDL temp on electrical model	Effect of RDL stress on electrical model	CPI/CBPI induced failures: RDL cracking & delamination	Effect of temp and stress on RDL EM			
	Au/Cu Wirebonding	Electromigration				IMC Corrosion		Bond wire fatigue		Cu/ELK cracking	Bonding force models							
	µBump/C4 Bump/UBM	Electromigration Induced voids	Black's model; Multiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	µbump electrical model	Die Internal Joule/SHE temp effect & external temp effect on bump temperature	UBM delamination	Galvanic effect (electro-chemical reaction)	Bump joint cracking; Under Bump ELK cracking; Under pad cracking in substate	CTE mismatch induced stress; Fatigue	Tensile stress causes bump peel; cracks at µbump; UBM and interface	Fracture/fatigue from shock, drop, impact, Vibr; e.g. in die attach, dielectric layer, inter-poser, UBM, solder joints	Effect of temp on bump electrical model	Effect of bump stress on electrical model	Multi Physics Bump EM - local current, temp, temp gradient and stress effect on µbump EM	Bump fatigue: effect of local temp & stress on fatigue life	Package material thermal/mechanical properties; Die metal stack and thermal/mech properties; µBump/C4 bump/TSV thermal mechanical properties; Cu/ELK fracture criteria; Void initiation and propagation criteria; Interconnect fatigue/creep model; Package interface fracture criteria; Moisture diffusion and vapor pressure model; IMC thermal/mech/electrical properties; Photonics optical properties		
	TSV/Interposer/ EMIB	Electromigration; Barrier Dielectric breakdown	Black's model; Multiphysics EM model including elctron, thermal gradient, stress gradient and atomic diffusion	TSV electrical model	Internal Joule/SHE temp effect on the TSV temp; External temp effect on TSV temp.			Cu pumping/TSV pop up	Cu extrsion due to CTE mismatch with Si; plastic rachetting at high temp			Effect of TSV temp on electrical model	Effect of TSV stress on electrical model	TSV EM response to local current, temp field and stress; TSV Pop out and effects on TSV/Si delaminaton	Barrier breakdown - How does voltage/current, temp and stress affect TSV barrier BD?			
Packaging /System	Passivation	Passivation cracking	EOS induced cracking			Passivation cracking & delamination; underfill/Mold compound delamination		Passivation cracking	CPI stress in SIN									
	Underfill					Underfill to die/substrate delamination; underfill swelling	Moisture degradation in underfill & at interfaces	Bump joint cracking	Solder joint fracture and fatigue due to underfill expansion									
	High Density Substrate	Metal trace electromigration		Package Substrate RLC model extraction	Co-thermal sim from die to package	Metal trace corrosion		Metal trace/via cracking				Thermal - electrical perfromance interactions	Mechanical-electrical performance interactions	Cu trace EM - effect of local current, temp and stress	Thermal & mechanical effect on Cu trace/via cracking			
	Wafer Level Package							Warpage										
	Fanout Package							Warpage										
	2.x/2.5D Interposer Package (CoWoS and EMIB, etc)							Warpage; Embedded die delamination from substrate & sidewall; µvia & µbump cracking & delamination; Solder/TIM delamination										
	3D Package (Foveros, etc)			Mold compound pop-corn; Anisotropic conductive adhesive cracks		Mold compound pop-corning		FinFET Ion shift (due to TSV/Si CTE mismatch, µBump stress, shrinkage of underfill & EMC); TSV effects on BTI/HCI; BEOL cracking; Cu pillar joint failure; Mold compound pop-corn; conductive adhesive cracking										
	Chiplet/KGD	ESD						Die edge cracking; Under bump ELK cracking										
Module/ System	Printed Circuit Board Assembly	Leakage current and shorts from Conductive filament formation	electro-chemical metal migration	PCB Board electrical model	\Co-thermal sim from die to package to system	leakage current and shorts from loss of surface insulation resistance & conductive filament formation	moisture ingress, leading to fiber-matrix debonding, and electro-chemical metal migration	Solder joint cracking ; Cracking of PTH plating; PCB delamination; trace cracking; Warpage	thermomechanical fatigue of trace and solder, IMC fracture; CTE mismatches between: component / PWB, metallization/ dielectrics	Solder joint cracking; pad cratering	Stress exceeds the material and interface strength	Effects of PCB temp and corrosion on electrical model?	Effects of PCB stress on electrical model?	Board level Solder Joint Reliability	ANSYS Mechanical	PCB thermal/ mechanical properties; Solder joint fatigue/creep model; Solder joint dynamic/ properties		

Chiplet reliability assessment capabilities: status

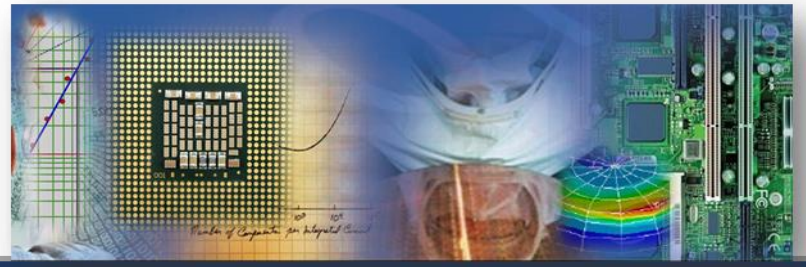
Key Elements for DfR Flow	Wafer Level DfR	Package and System Level DfR	Chip to Package to Board Interactions
Electrical and Thermal Stress	Localized Self Heating and hot spots	Global Level thermal managements	FEOL/BEOL and systeme level thermal interactions
Failure Modes	TDDB, HCI, BTI , EM and SM, etc	Warpage, delamination; C4, ubump, DBI, TSV, Optical Via interconnect fatigue and migration failure, etc	Global and local Stress effects on Cu/ELK failure, stress effects on FET's mobility
Failure Mechanism and Reliability Model	Weibull, Lognormal, Power Law Model, Aging Model, etc	Weibull, Lognormal, multiphysics models, etc; many are under development	Under development
Material Chaterization and Modeling	Modeling device thermal characteristics (Thermal resistance) Modeling device aging Modeling the impact of stress on device threshold, delay, etc.	To make materials data useable by EDA tools – and enable them to produce accurate and meaningful results – materials data needs to be presented in a machine-readable format and agreed upon with EDA tool vendor.	Modelling multi scale and multi physics failures
Process Design Kit (PDK)	Foundry Design Kit	Assembly Process Design Kit	Under development
EDA Flow	Cadence Spectre/HSPICE, etc	Ansys/Mentor, etc	Mentor/Synopsys
Circuit/System Reliability	HCI/BTI and EM Available; TDDB and SM not Available	Under development	Under development

Established
Partially Established
Under development or Not Available

Qualification and testing: Reliability validation/verification

HETEROGENEOUS INTEGRATION ROADMAP

The changing and challenging landscape



Need for dynamic, flexible models and methods

- Extreme environments
- Extreme usages/ lifetime
- Latest tech nodes
- Diverse components
- New failure modes
- Wide range of Rel tests
- Innovative FA/FI
- Stochastic modeling
- Field Telemetry
- Reliability Physics
- Test time optimizations
- Digital Twin feedback loop

Multi-physics methods to quantify 'stress' and 'strength' distributions at potential sites of failure	Qualification testing needs to be Customized, Knowledge-based and Innovative	Data feedback loop with Digital Twins to validate failure characteristics and run virtual experiments	Integrated PHM - Self-cognizant, intelligent, bio-mimetic hardware to 'age with grace'

Source: Sahasrabudhe (Intel)

Summary: Reliable Chiplets and HI Systems

Convergence of Reliability-Physics (RP) and Artificial Intelligence (AI)

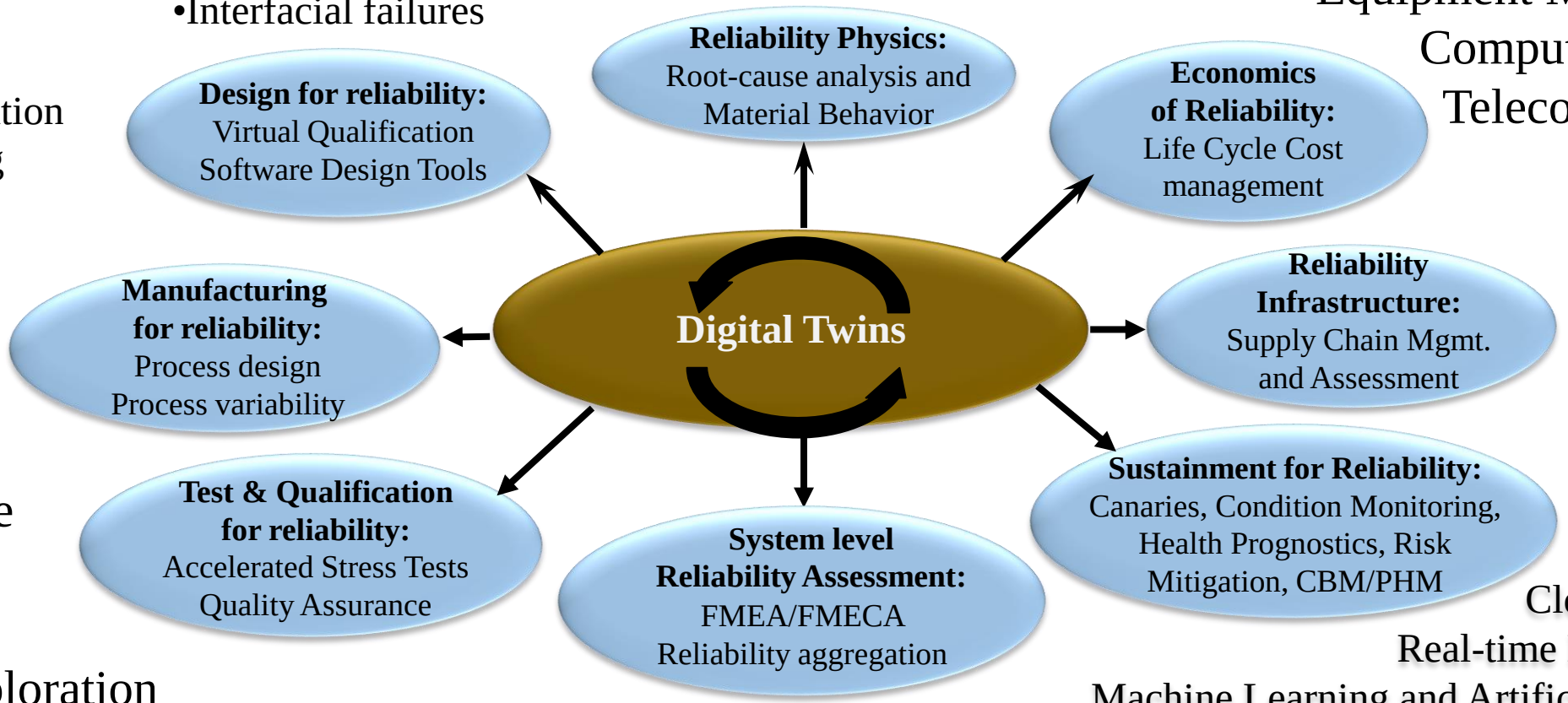
HETEROGENEOUS INTEGRATION ROADMAP

- Fatigue and Fracture
- Plasticity, creep
- TDDB
- ESD/EOS
- Electromigration
- Wear/fretting

- Whiskers
- Aging of polymers
- Interfacial failures

- Corrosion
- ECM

Semiconductor and Packaging
Equipment Manufacturers
Computer/Consumer
Telecommunication
Medical



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Intelligent, resilient, self-cognizant, self-healing chiplet-based HI systems

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