
# Too Hot To Test

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# System Power Modeling and Analysis for Test

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Thrace Systems

# Introduction

CEO of Thrace Systems, focuses on System Power EDA
Co-chair of CDX (Chiplet Design Exchange) workstream under OCP ODSA
Previously 18 years and Broadcom/Avago/LSI/LSI Logic
Responsible for power tools and methodology

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Product line

PowerMeter™ is a comprehensive and collaborative power analysis platform for System Level Power Analysis

Cloud-native for best-of-class collaboration and concurrent analysis

IEEE2416 model generator

Design Dashboard Engine

# Agenda

**Power and Thermal Analysis Overview**

- Objectives
- Definitions
- System Level Power models
- Flows

**Models in action**

- Chiplet system power and thermal models and results

**Q&A**

# Objectives of Power and Thermal Analysis

Resolve Thermal concerns

Need to know sequence, location, amount and duration of power dissipation

Power supply concerns

Need to know worst case current draw and current draw change

Battery concerns

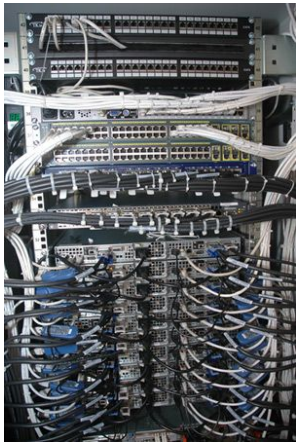
Need to know energy consumption over very long period of time

# Flow and model needs: What is your System?

**System**

Any configuration of elements outside of a unit's power supplies

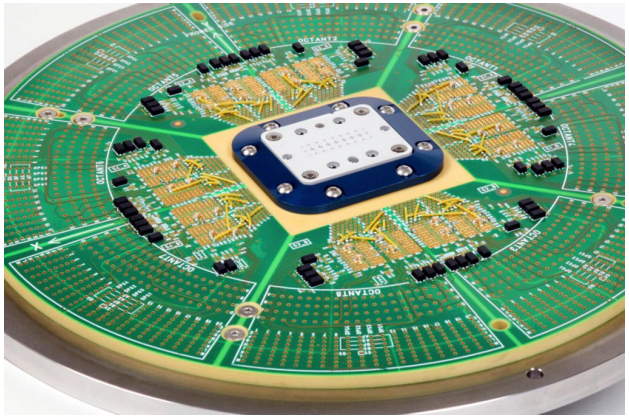
This includes supplies, boards, connectivity, packaging, other components inside or outside of the package, or lack of them



**Scenario**

A full set of configuration parameters to describe a single unit of operation

This includes voltage levels, ambient temperatures, modes of operation



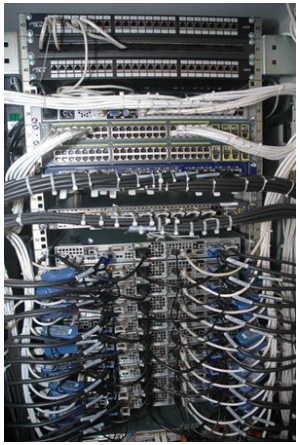
# Flow and model needs: What is your System?

**Planning for Test needs to start as early as architecture level**

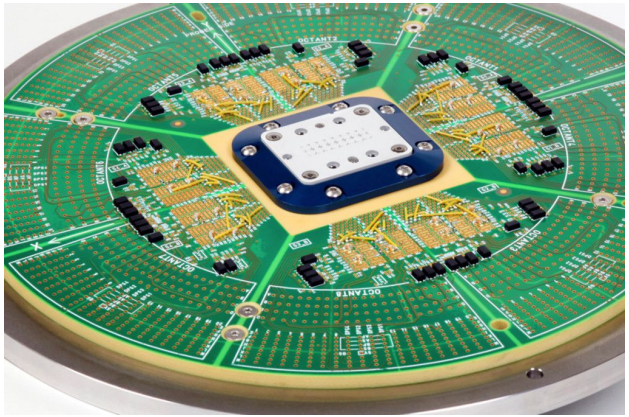
Plan supplies (System)

Plan thermal aspects of system, both application and test (System)

Plan test flow and sequences (Scenarios)



**Sets a baseline electrical and thermal constraints**



**Need flexible System Power Models**

Maintain compatibility over time and between flows

Modeling parameters outside of typical bounds

# System Power Model (SPM)

**Thrace System's System Power Model works from pre-RTL architecture level to post-Si analysis**

- Designed with "any-system" in mind
- Maintains historical learnings through technology mapping

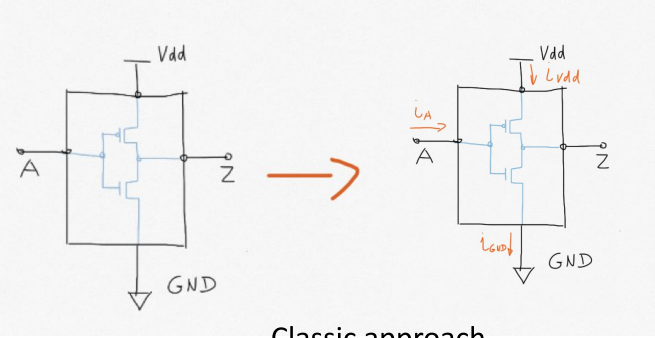
**Higher level of abstraction modeling than classic models (Liberty)**

- Can model almost anything - regulators, SERDES, transaction power
- Designed to scale to handle large and complex systems

**Includes support for IEEE2416 Power Contributors**

- Announced at DAC'20 first production IEEE2416 generator as part of PowerMeter
- See Tutorial replay here https://si2.org/dac-upm-tutorial/

# Introduction to IEEE2416



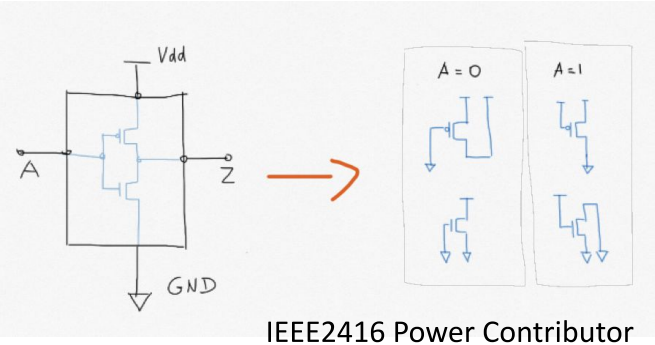

Classic approach

Classic approach to power modelling (Liberty)

- Capture boundary pin currents at a **fixed Process, Voltage and Temperature**

  PROS: Very Simple models

  CONS: Fixed value, **not possible to vary P,V,T**, need a new model




IEEE2416 Power Contributor

IEEE2416 approach targets variable Process, Voltage and Temperature post model generation

- Capture circuit details, estimate leakage later

  PROS:

  Designed with **variable P,V,T** in mind

  **End-user can vary P,V,T**

# CDX Reference flow

ODSA CDX workstream

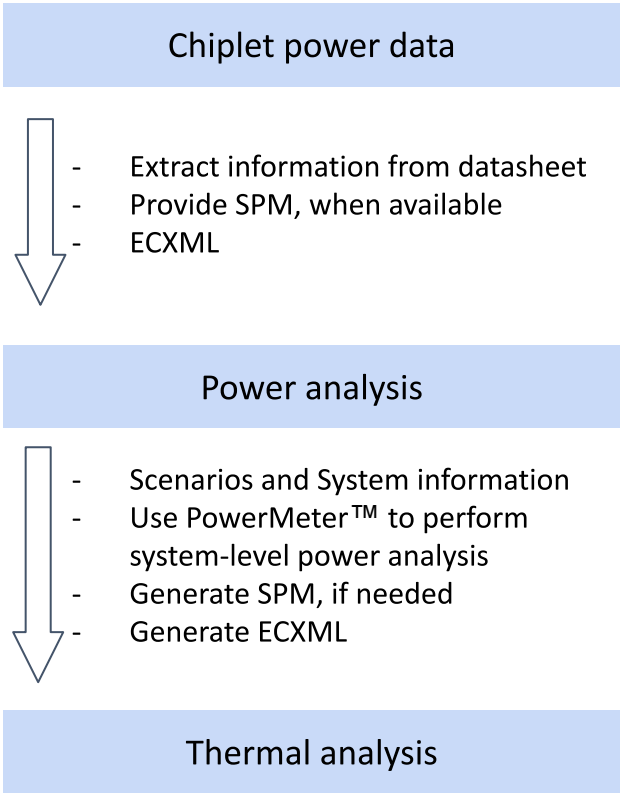
- Focus on flow pipe clean and PoC
- Design data seeded by zGlue - OmniChip Reference Design

Si2 UPM workgroup

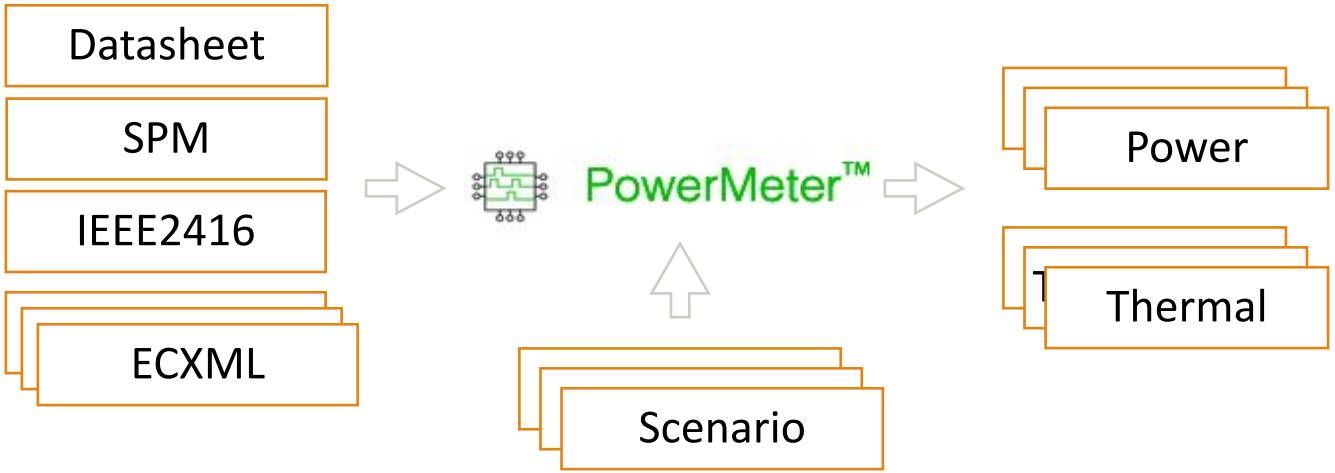
- Focus on IEEE2416 “IEEE Standard for Power Modeling to Enable System Level Analysis”, aka UPM

JEDEC

- Released ECXML spec in Sept’20



# Reference Flow




Concurrent Multi-Mode Multi-System functional and test power and thermal analysis

# CDX Reference design power analysis

Power data in datasheet

- Can it be converted to machine readable format?
- Can it be understood by tools?

System model?

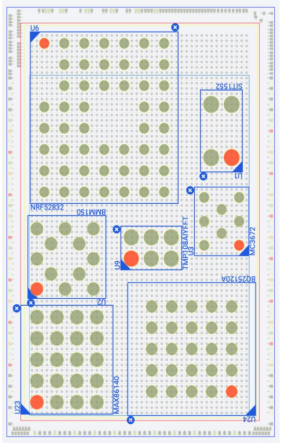
Scenario definition

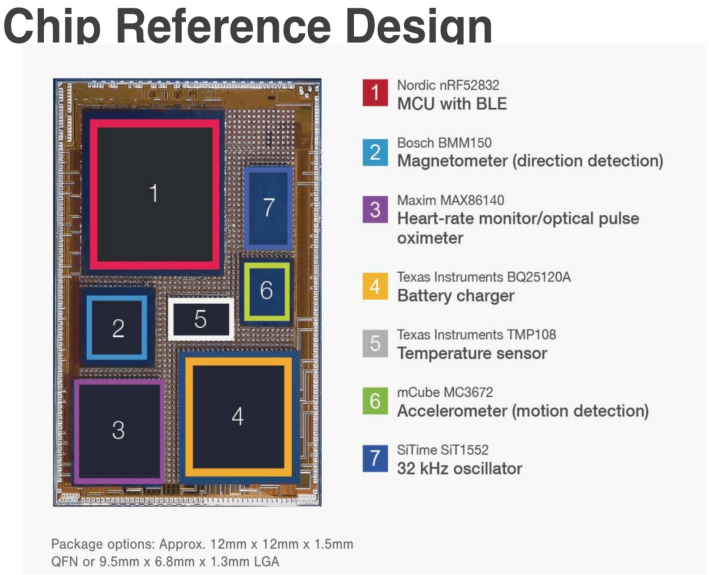
- Choose 2 application scenarios

Power analysis

- Power and energy

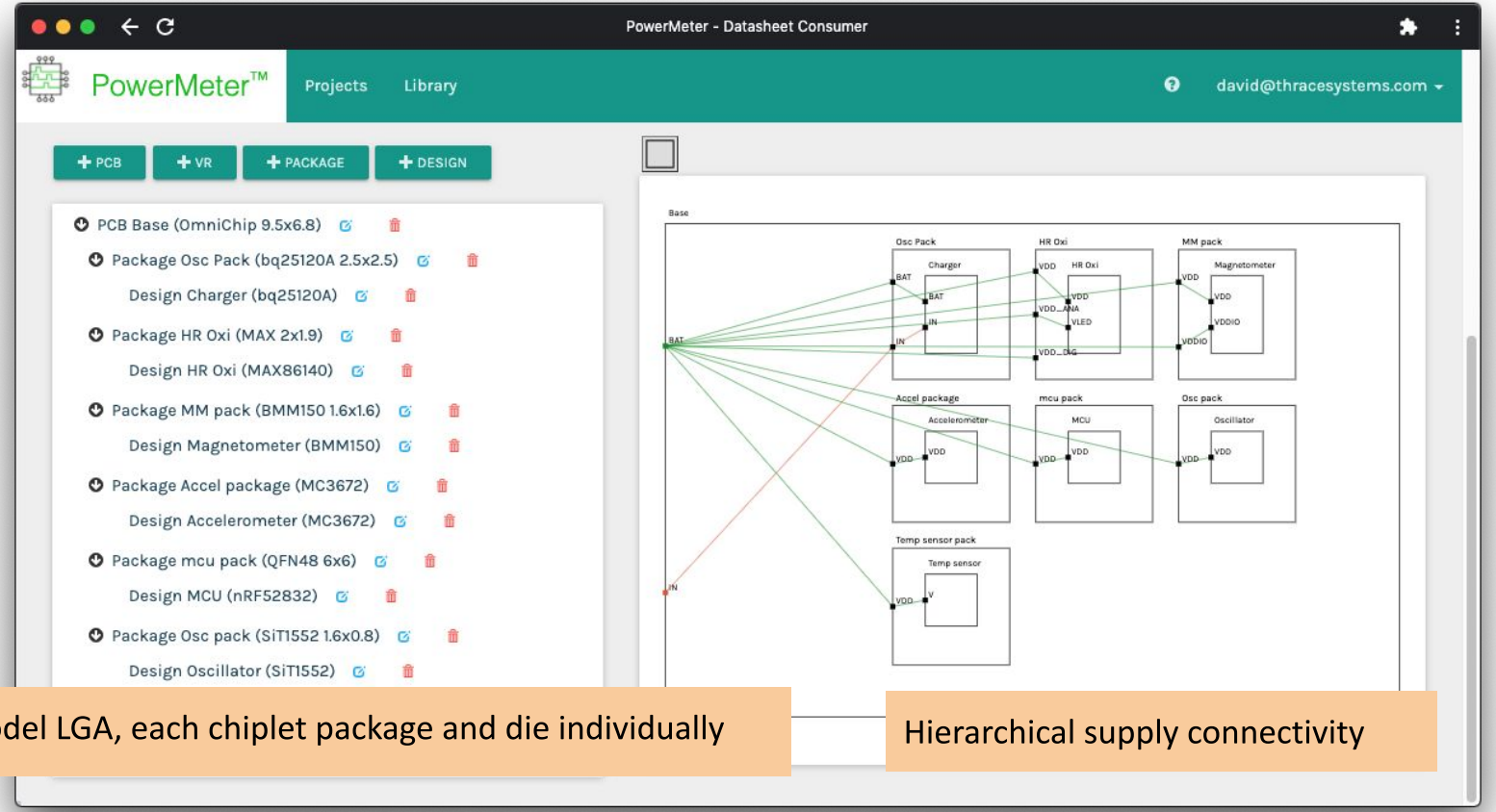
Full analysis results here (see May 8, 2020 links) or here






zGlue

# CDX Example System: Setup Overview




Model LGA, each chiplet package and die individually

Hierarchical supply connectivity

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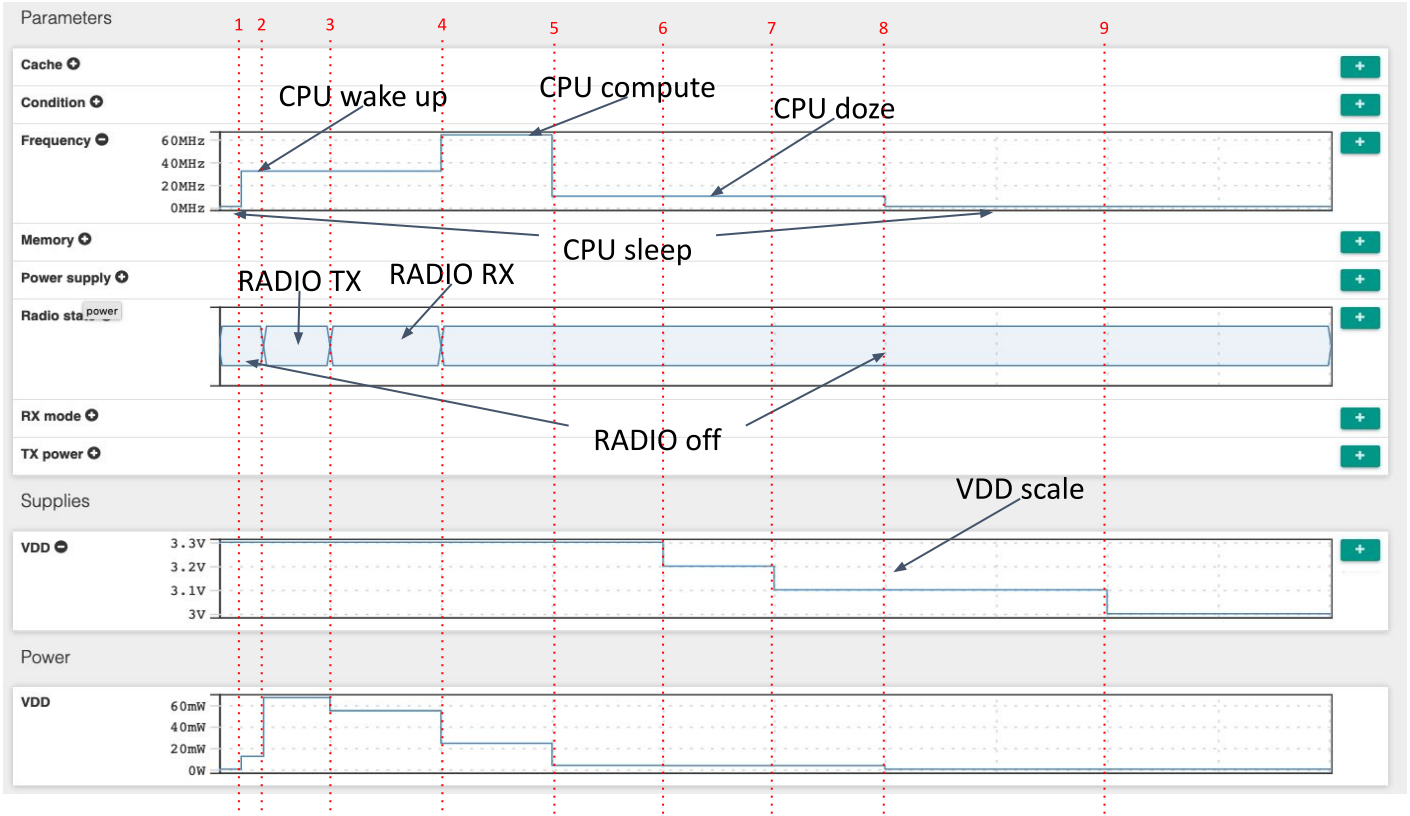
# MCU Scenario definition and power analysis

1. CPU wake up for processing
2. Begin TX
3. TX done, begin RX
4. RX done, compute result
5. Doze
6. Lower voltage
7. Lower voltage again
8. CPU sleep
9. Lower voltage again

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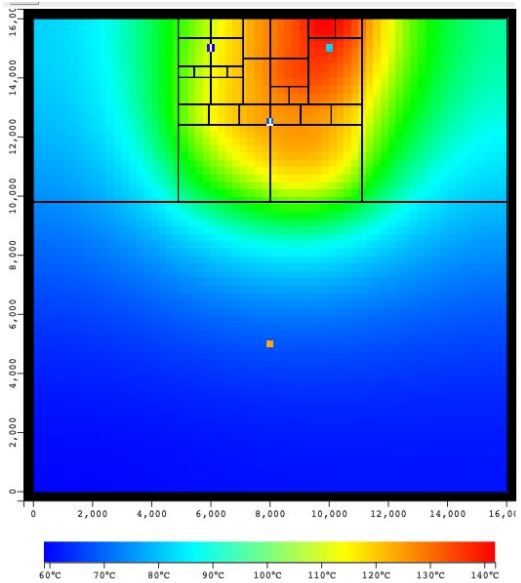
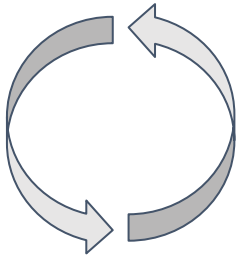
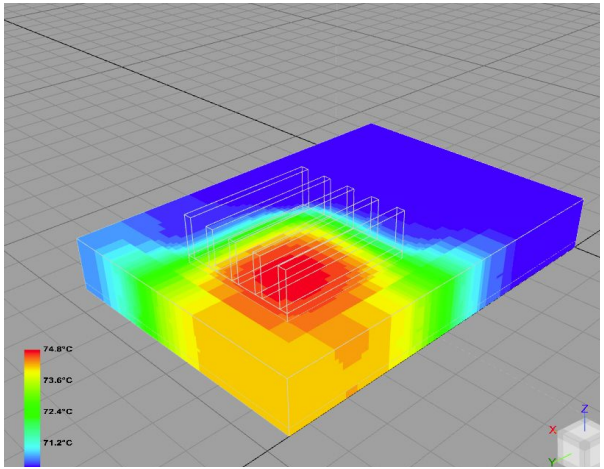
# Die & System Collaborative Thermal Analysis






High resolution Die level temperature analysis (sub-10um)
Performed by SoC/Chiplet designers
Uses simplified System Environment Model

High resolution System level temperature analysis
Performed by System designers
Uses System Power Model generated by SoC designers

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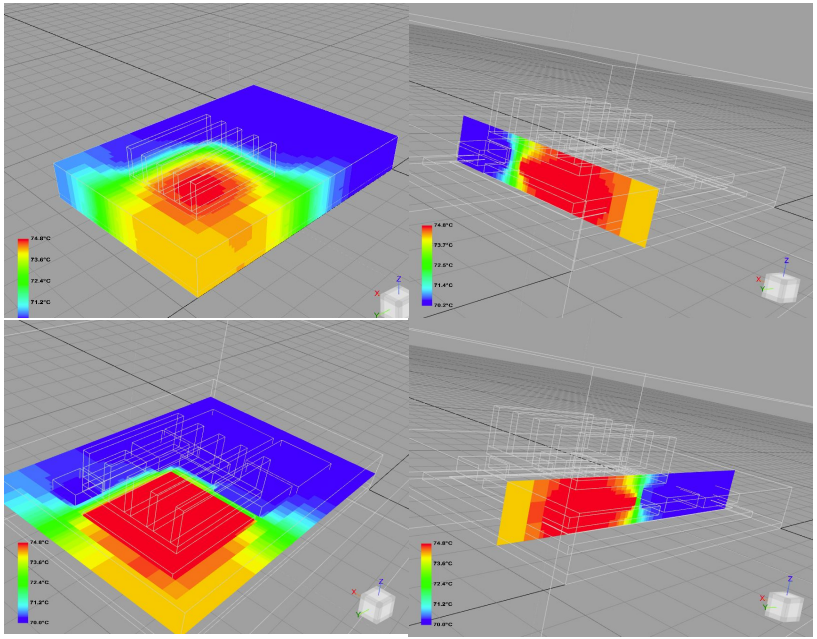
# Thermal analysis with ECXML



Concurrent analysis of Test-based Scenarios and Systems

Quickly iterate different options

Explore heat dissipation paths

| | ECXML1 | ECXML2 | ECXML3 | ... |
|---|---|---|---|---|
| Scenario 1 | 1W@35C | .. | 2W@50C | |
| Scenario 2 | | 1.2W@45C | 1.3W@34C | |
| Scenario 3 | | 0.7W@34C | | |
| ... | | | | |

# Summary

A System Power Model enables power analysis at a higher-level of any system

Collaborative and concurrent approach to power and thermal analysis is needed starting at the early design stages

Early test system specification and modeling is key to meeting targets

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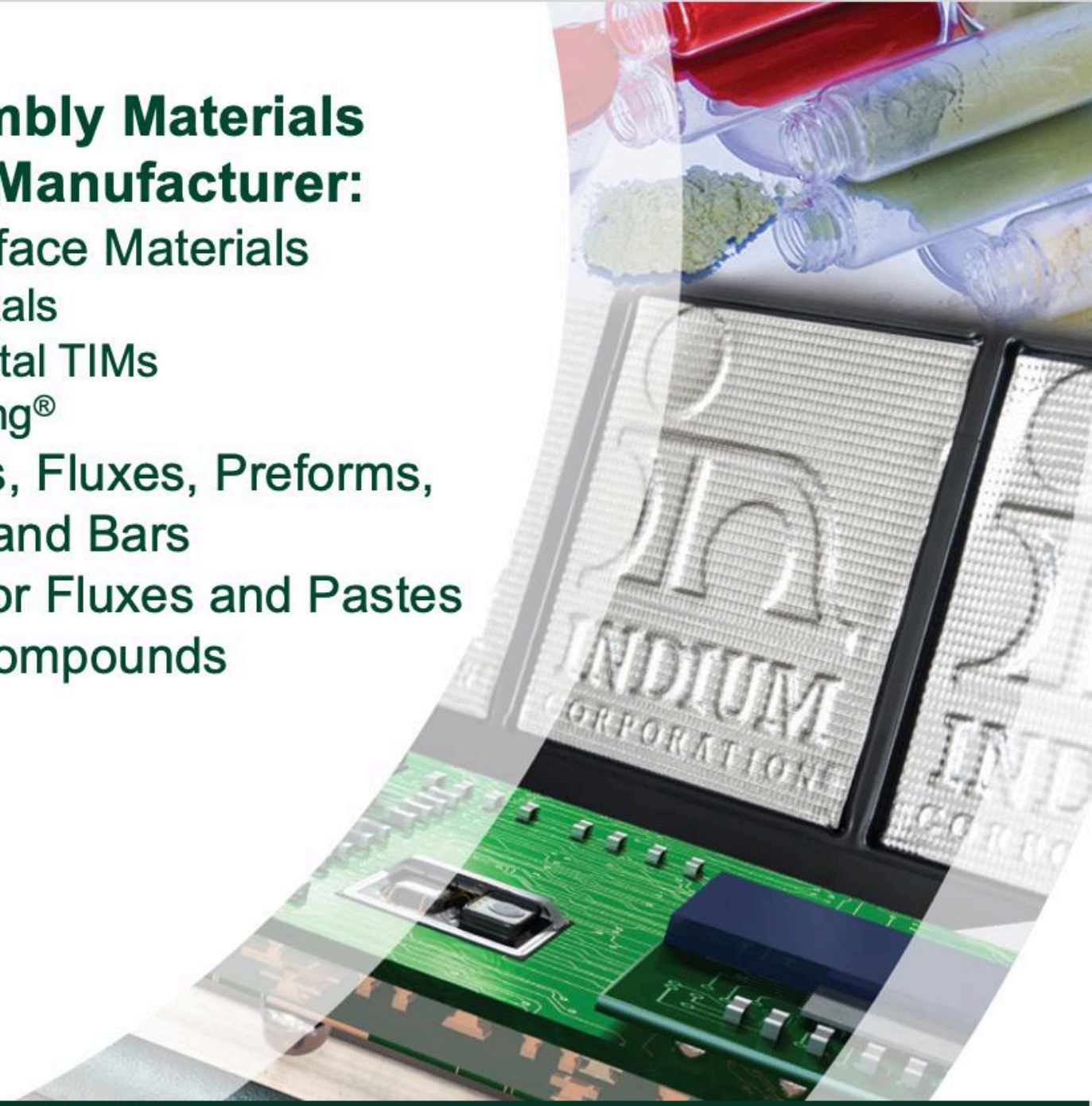


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