Too Hot To Test

February 9 - 11, 2021

www.meptec.org

MEPTEC
THE NEXT GENERATION

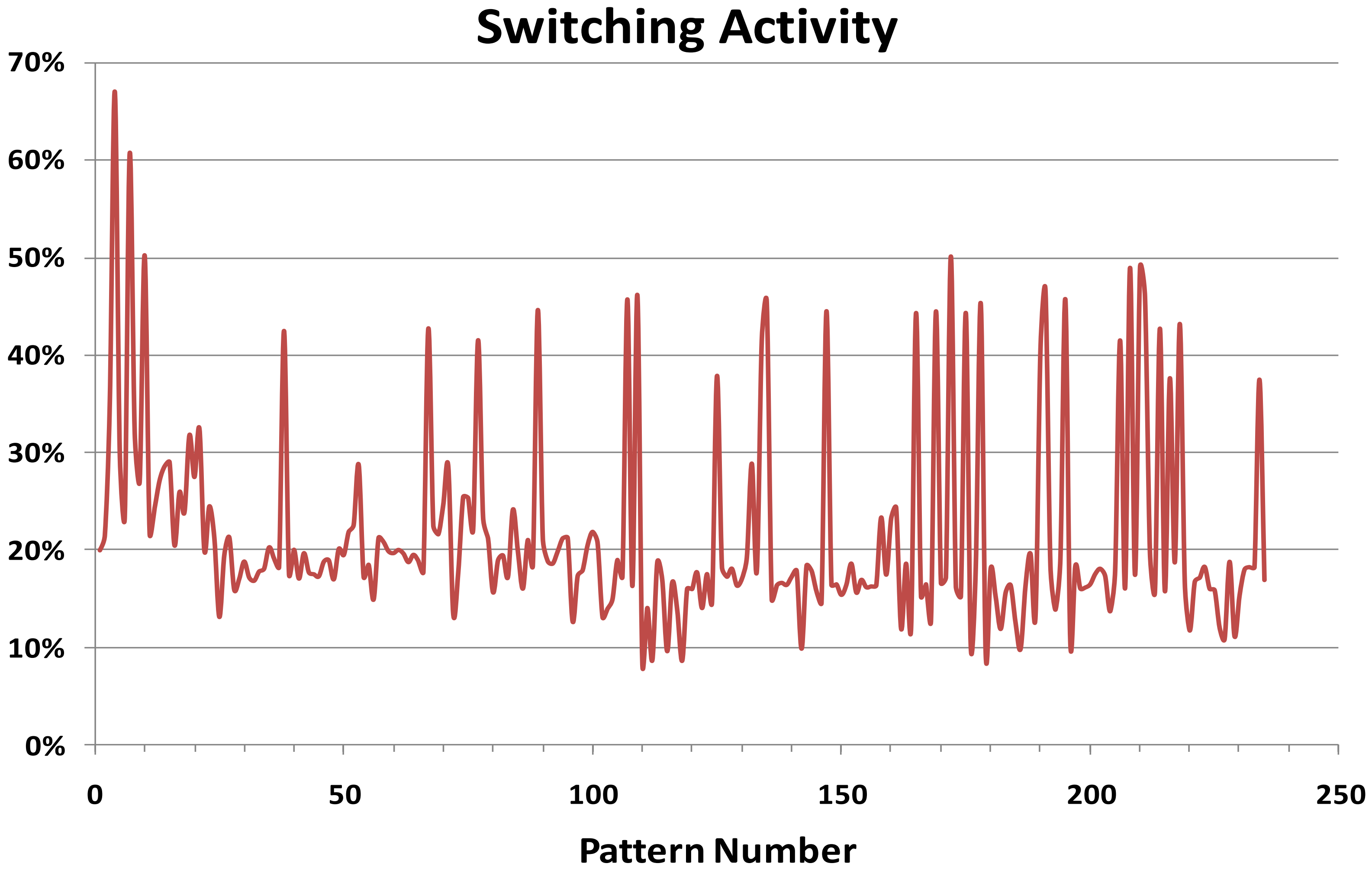
Correlation of Low-Power Synthesis and Test Capabilities to Silicon by EDA

MEPTEC 2021

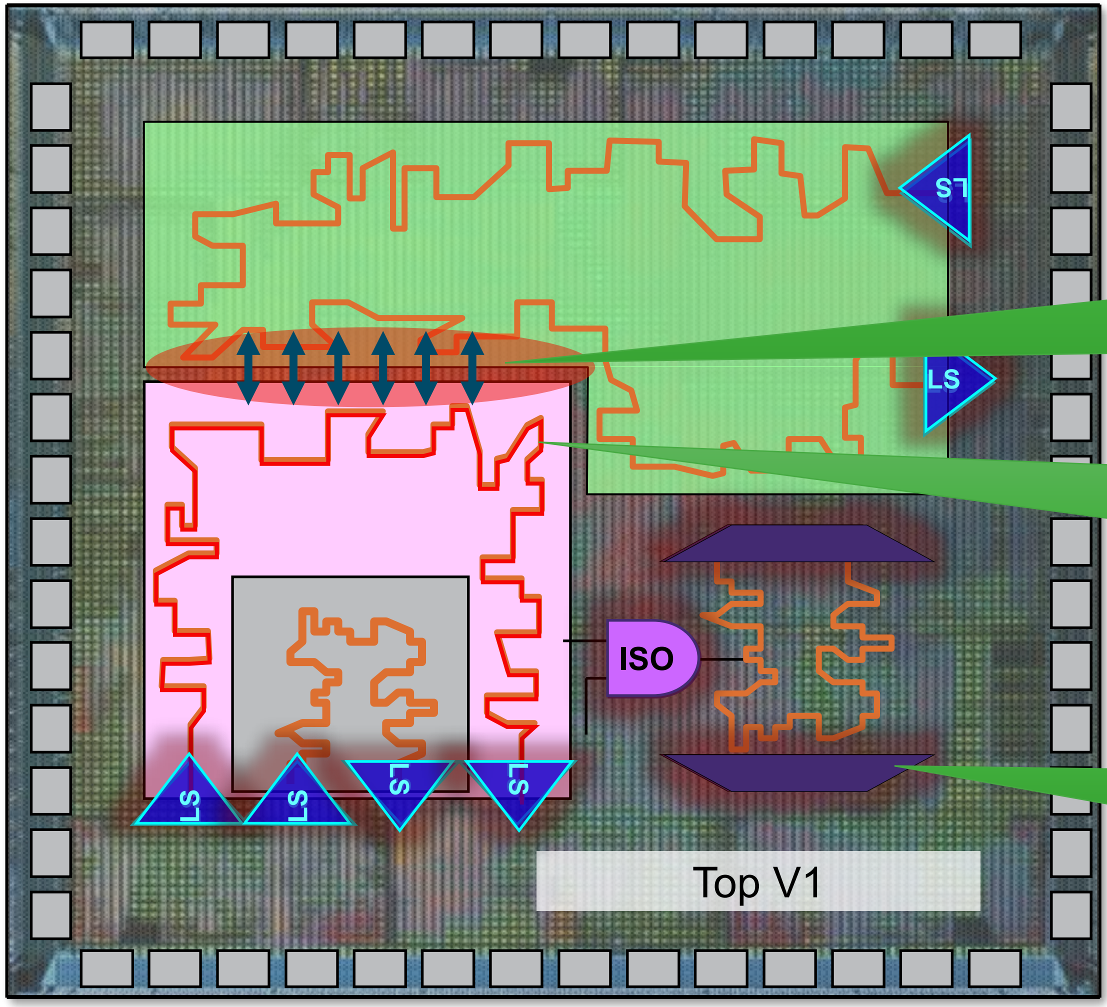
Adam Cron, Principal Engineer

Scan Testing is Power-Hungry

Up to 10X Peak Levels of Normal Operating Mode



Low-Power Design and Test



Automation in TestMAX to…

- Minimize scan chain crossings between voltage domains
- Ensure low-power constraints don't interfere with chain optimizations
- Minimize test logic power during mission mode

Hardware

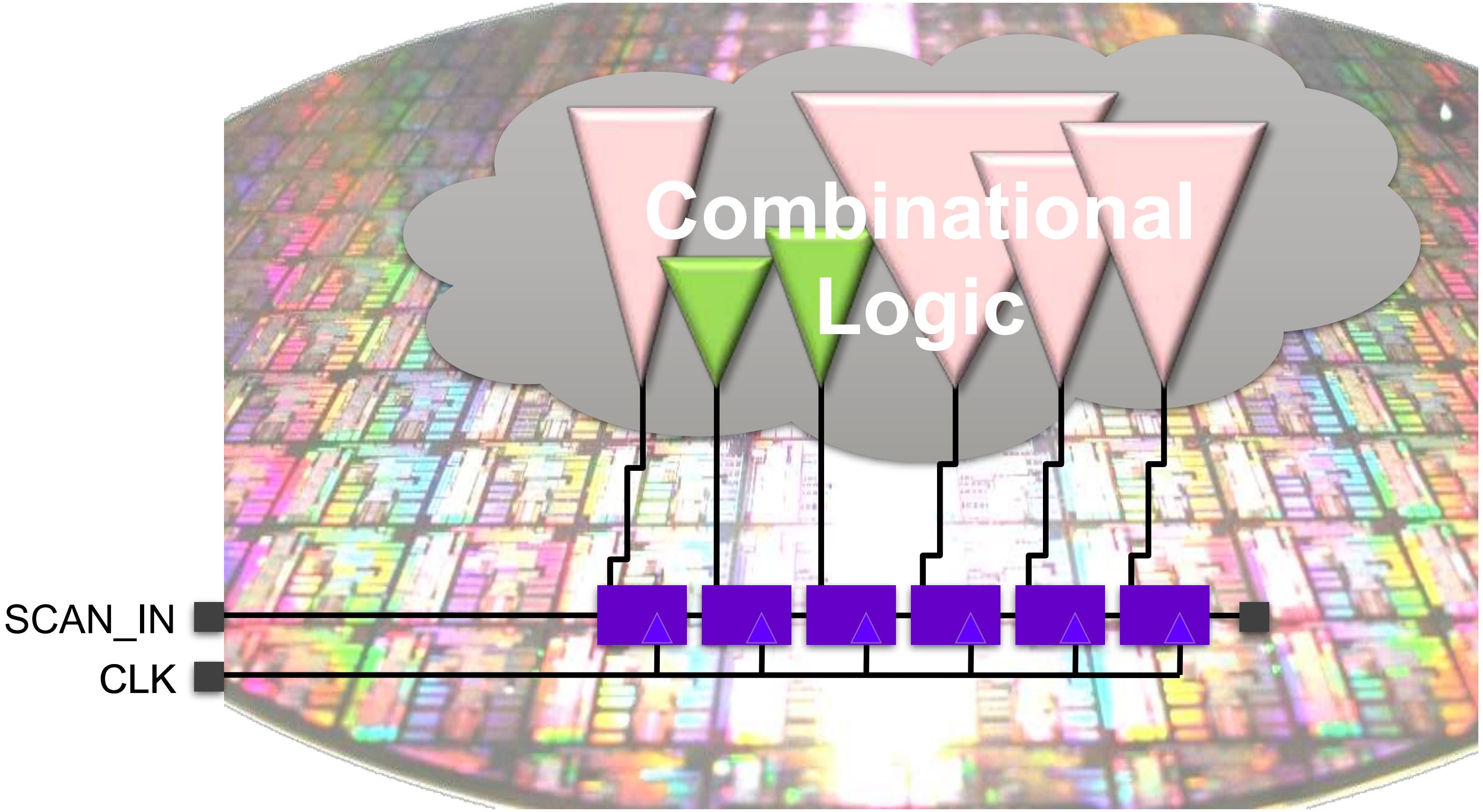
Shift

Q-Gating (Functional Output Gating)

- Adds a gate at the functional output of scan flop
- Logic driven by the functional output does not toggle during scan shift

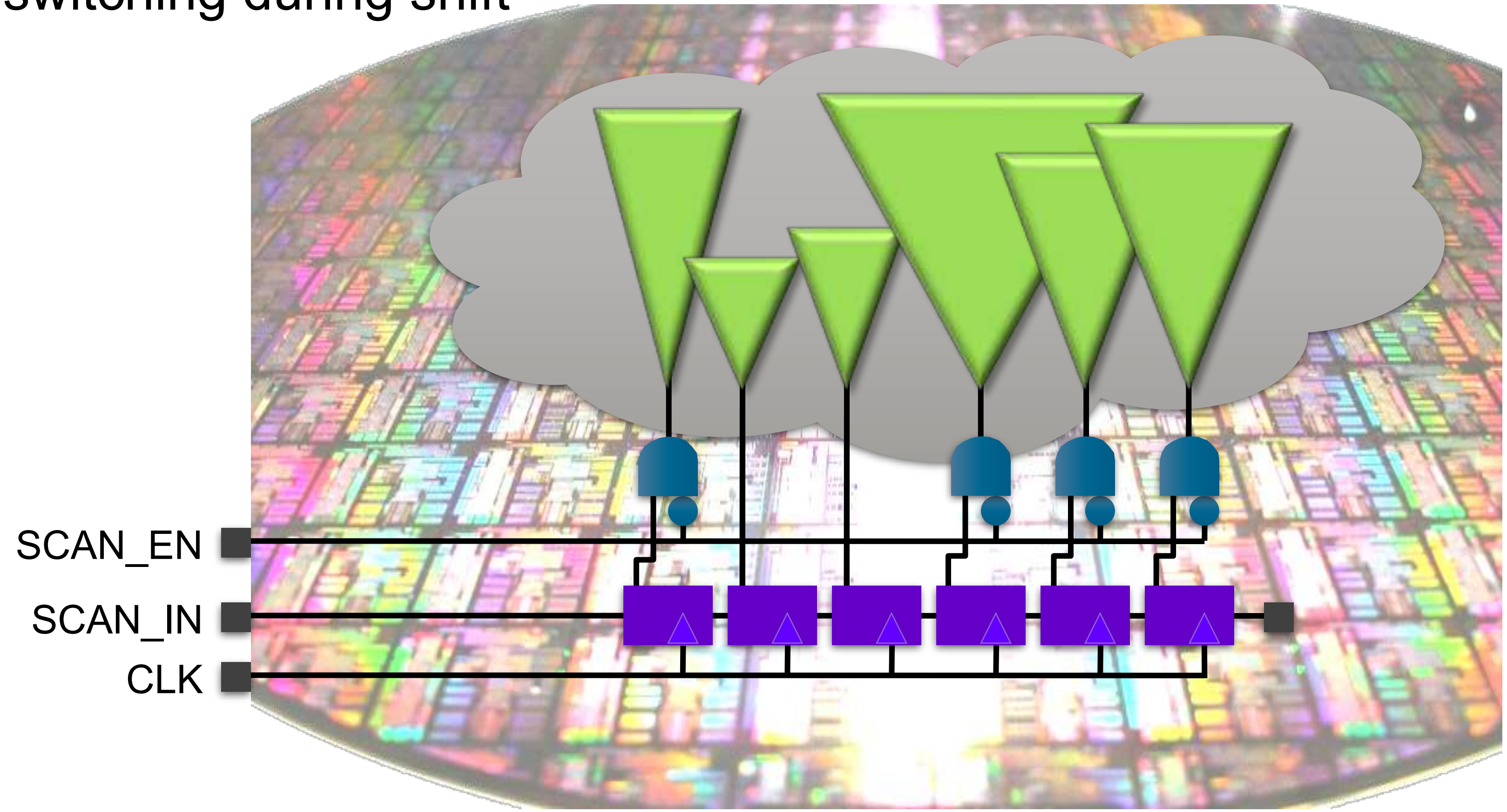
- Benefit: reduce power dissipation during shift

Shifting Produces Switching Activity in Logic Cones

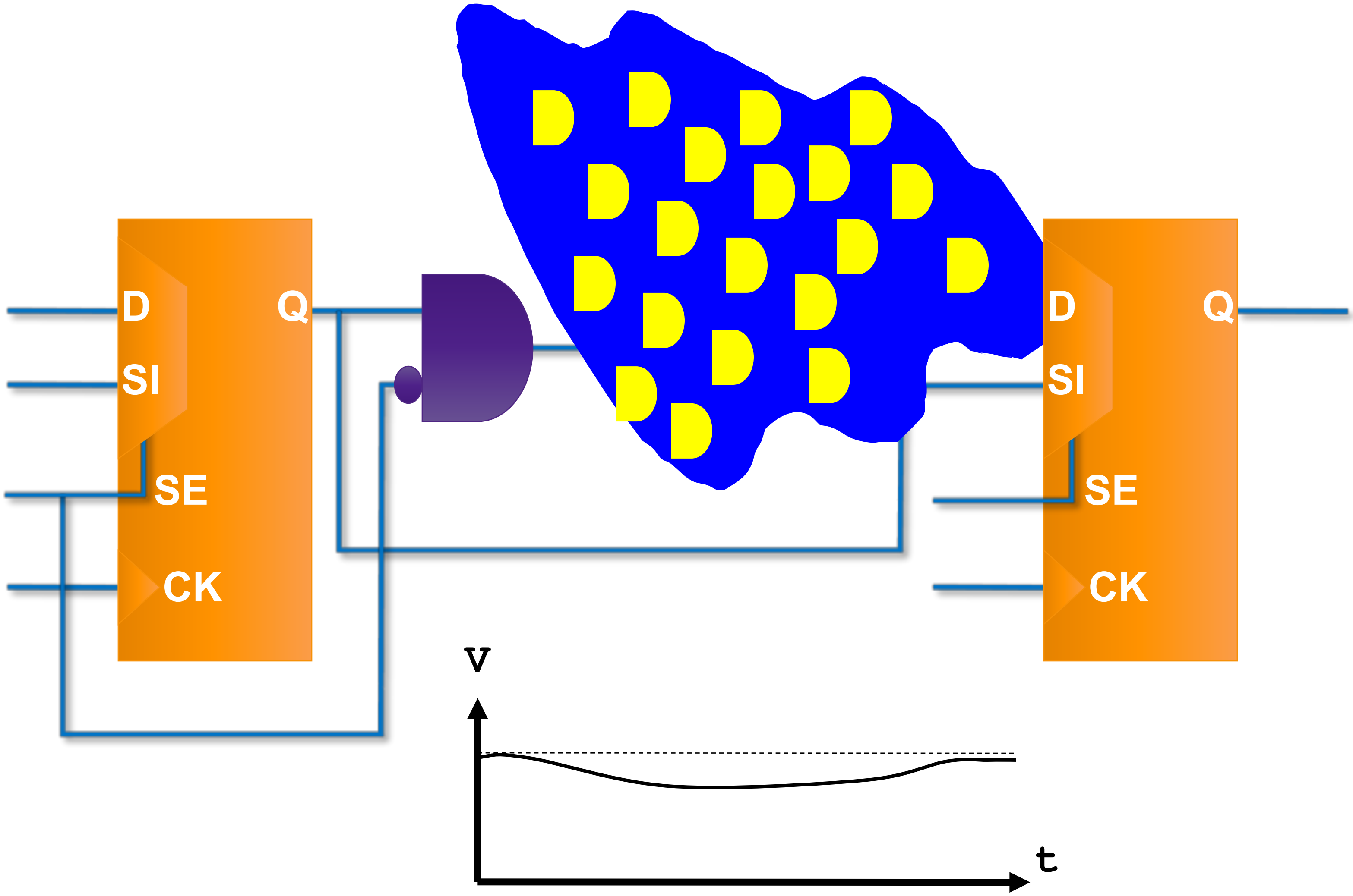


Power-Aware DFT

Q-gating reduces switching during shift



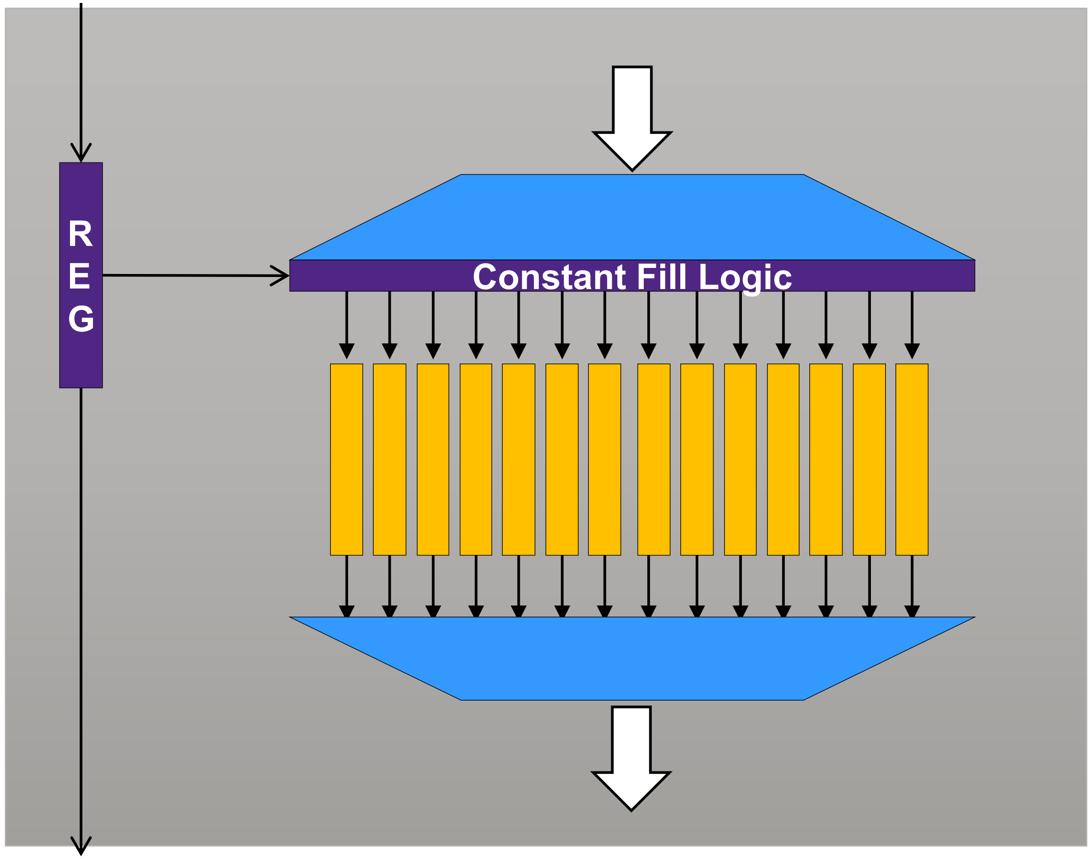
Power-Aware DFT



Reducing Shift Power for DFTMAX Compression

Compression codec layer

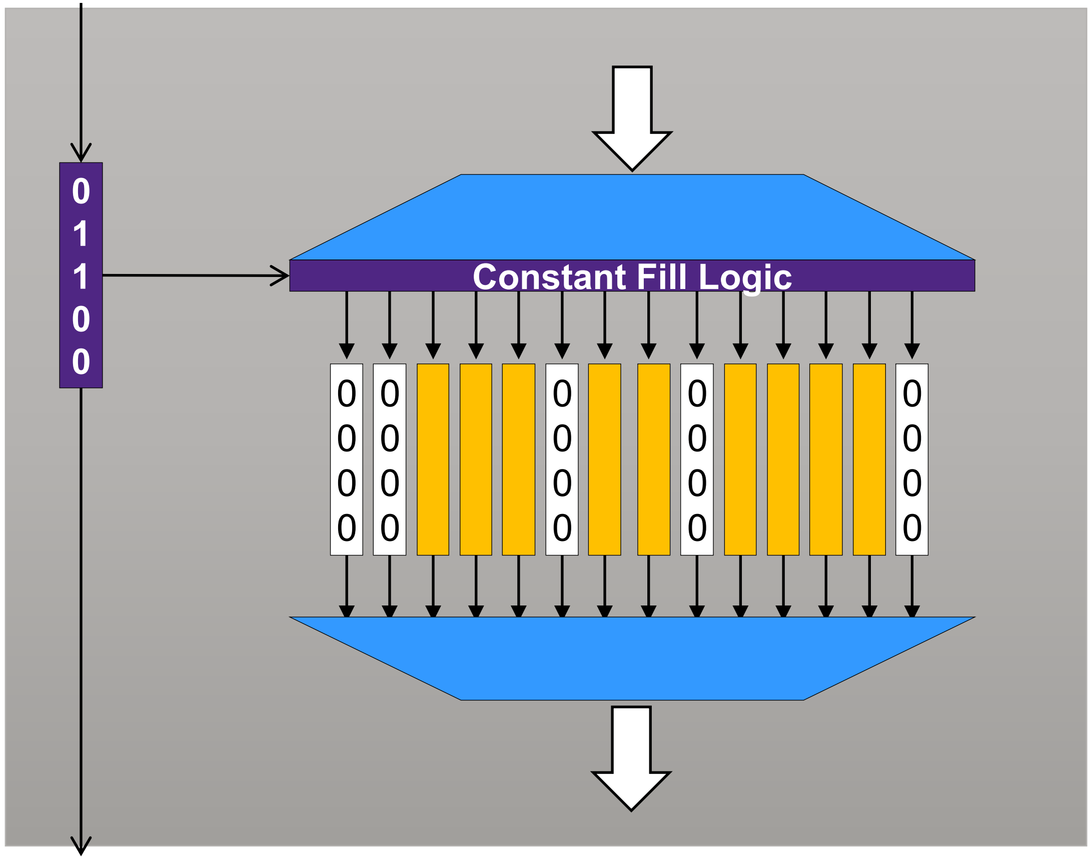
- Logic will fill scan chains with 0
  - Simple combinational logic
- Register will select scan chain fill
  - Dedicated scan chain, or shared with clock chain
- Register will have shift/update stage
  - Stable during shift of internal chains



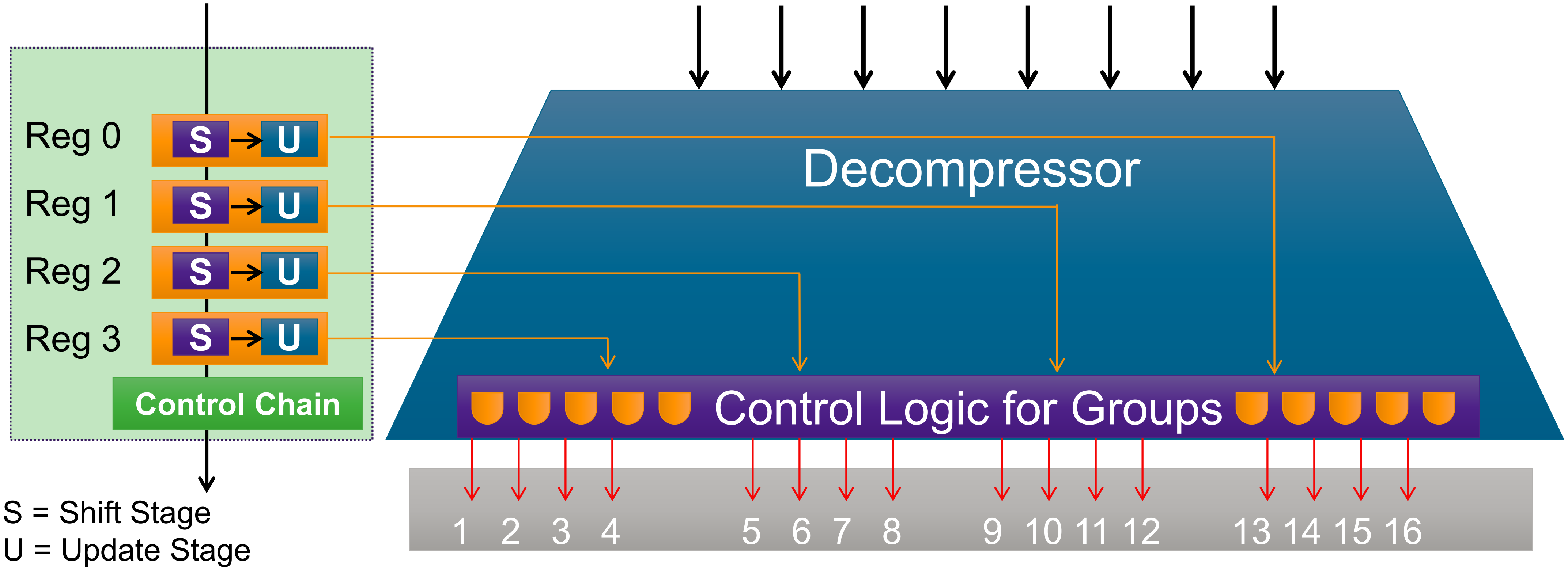
Reducing Shift Power

ATPG-driven selection

- User will specify peak shift toggle rate
- ATPG will use rate to determine number of zero-filled scan chains
  - Each pattern will select a set of chains
- Shift power register value for pattern N will be set in pattern N-1



Control of Chain Groups

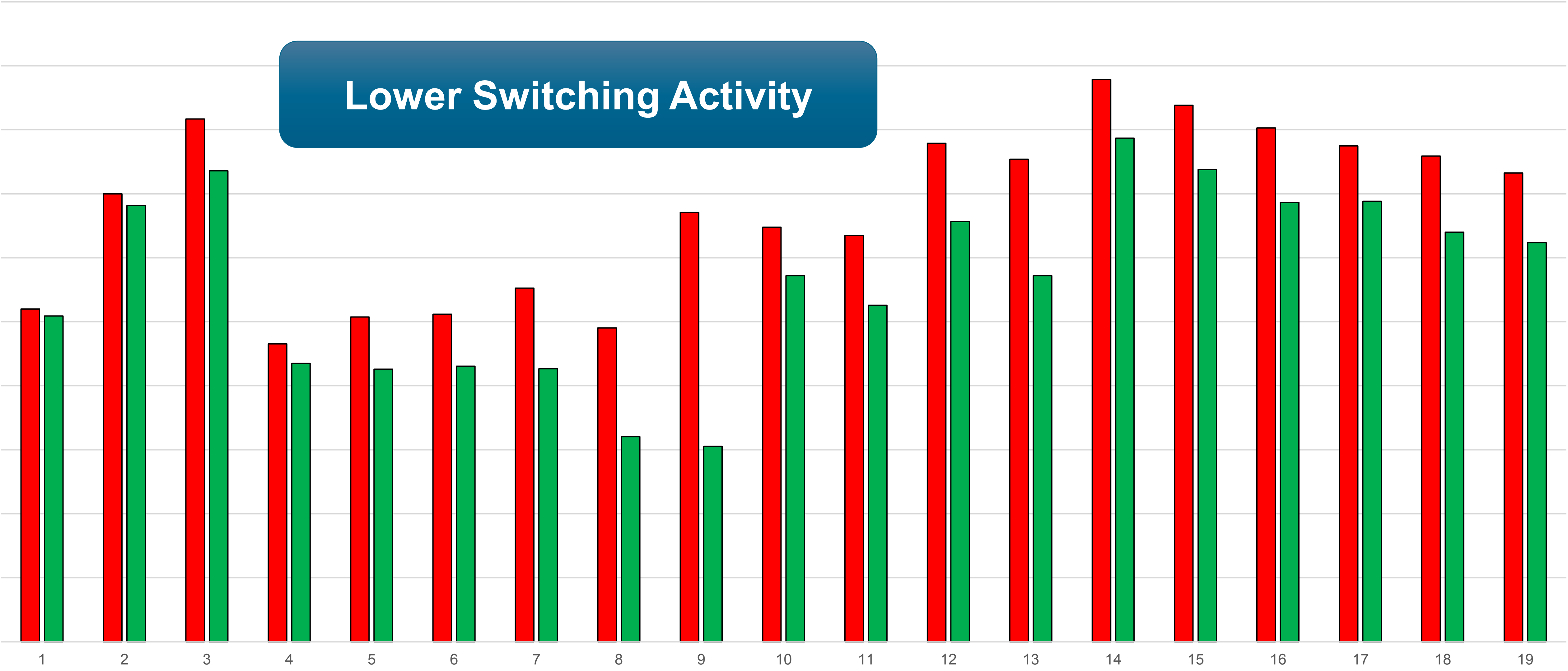


S = Shift Stage
U = Update Stage

Benefit

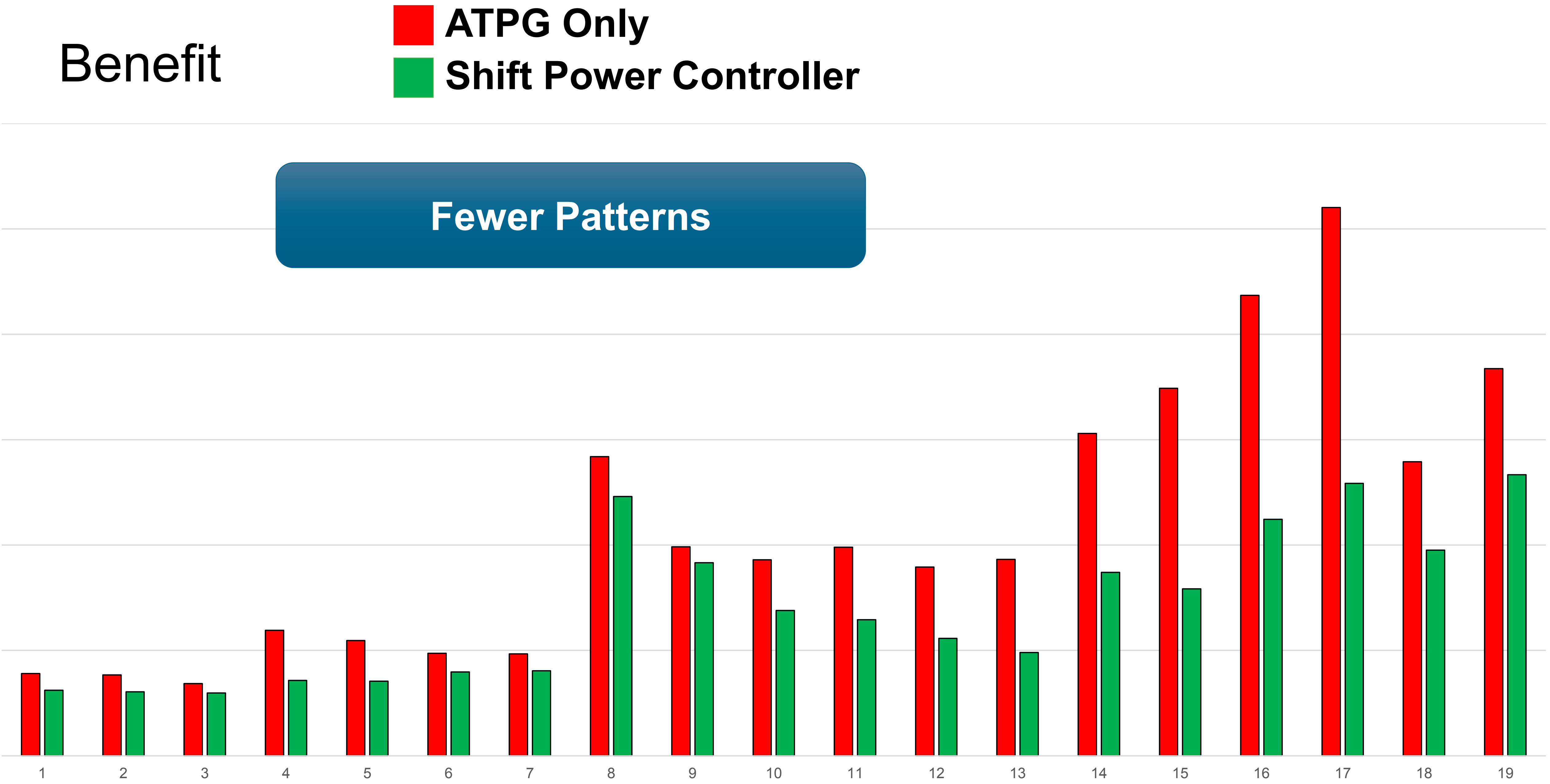
🟥 **ATPG Only**

🟩 **Shift Power Controller**



Lower Switching Activity

Benefit


🟥 ATPG Only
🟩 Shift Power Controller
Fewer Patterns
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19

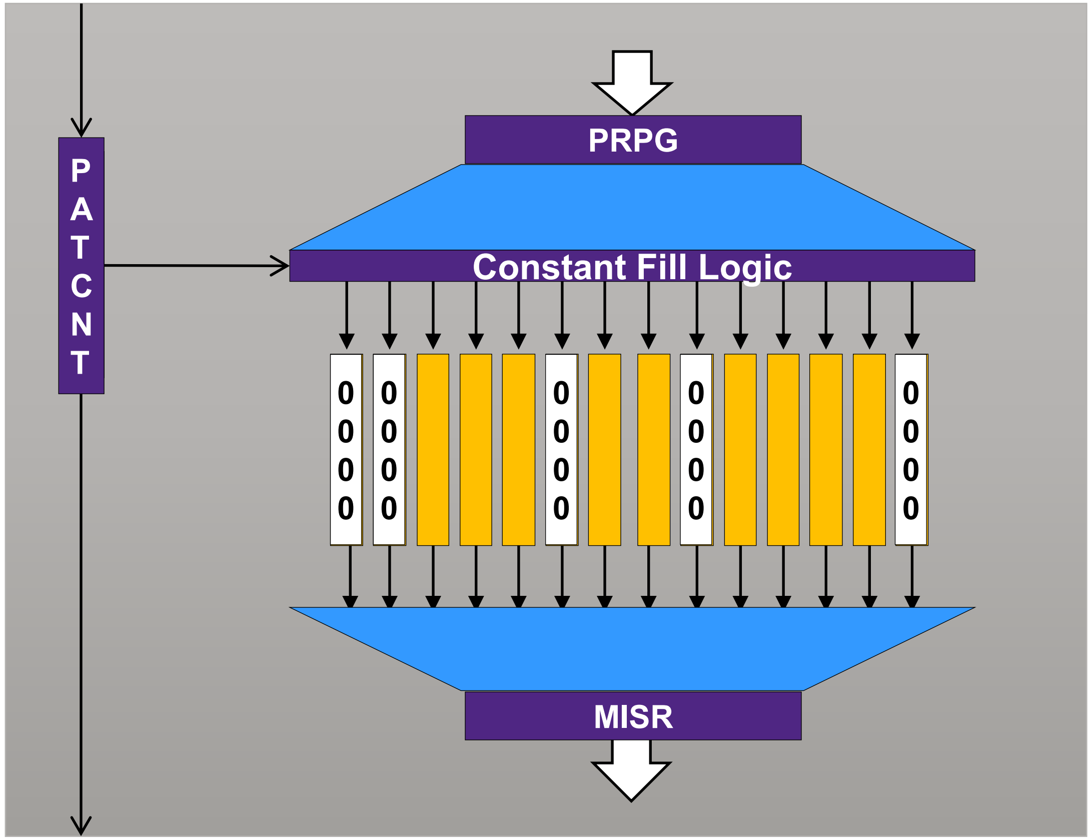
In-System DFTMAX LogicBIST Shift Power Control

- Logic fills scan chains with 0
  - Simple combinational logic
- Pattern Counter selects scan chain fill
- DFTMAX LogicBIST

```
set_logicbist_configuration \
  -shift_power_groups true  \
  -num_shift_power_groups N
```

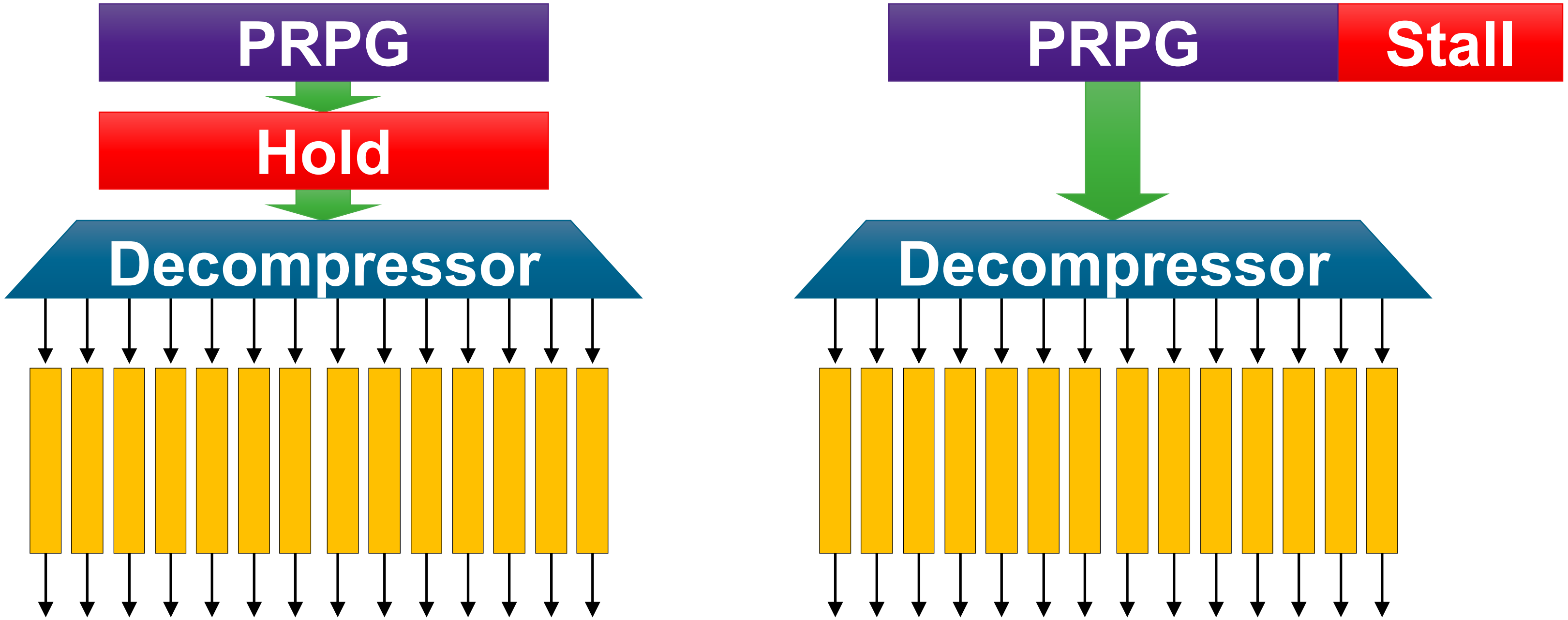
- TetraMAX ATPG

```
set_atpg -seq_comp_shift_power N
```



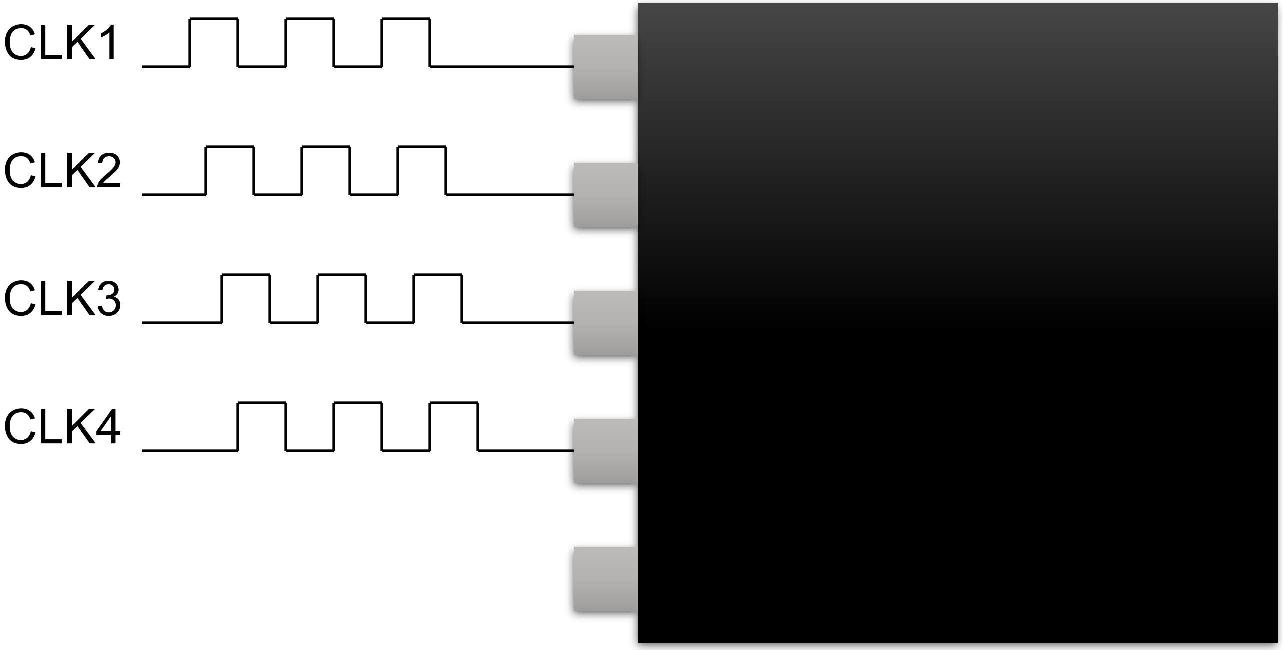
Low-Power Shift Mechanisms for Pseudo-Random Data Sources

- In-System LogicBIST might use other mechanisms to hold data
- DFT compression codecs that use pseudo-random pattern sources can use hold or stall mechanisms to stop PRPG data changes between shift-clock cycles



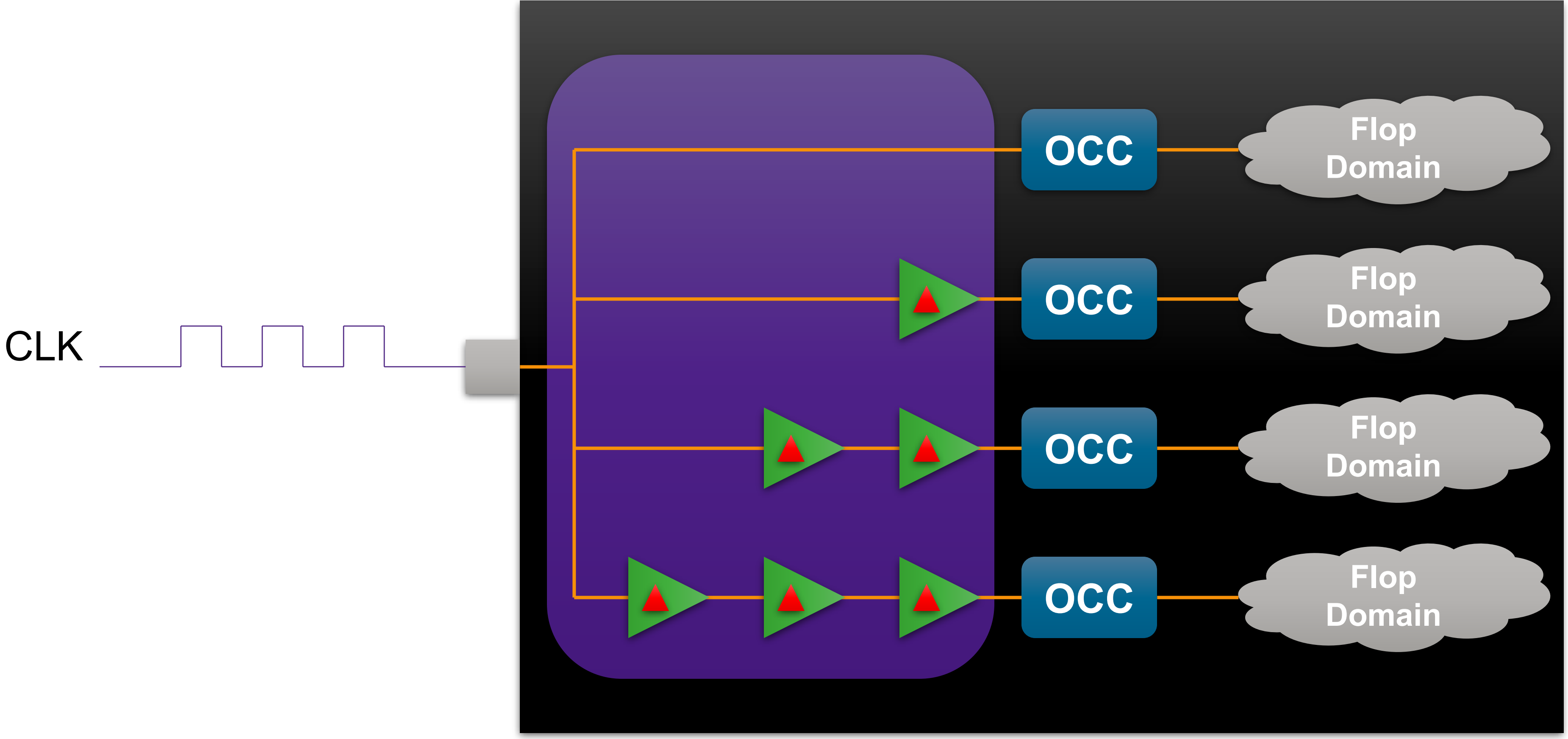
External Shift Clock Skewing

- Adjust external clocking during shift so that multiple shift clocks do not overlap



Internal Shift Clock Skewing Delay-Based

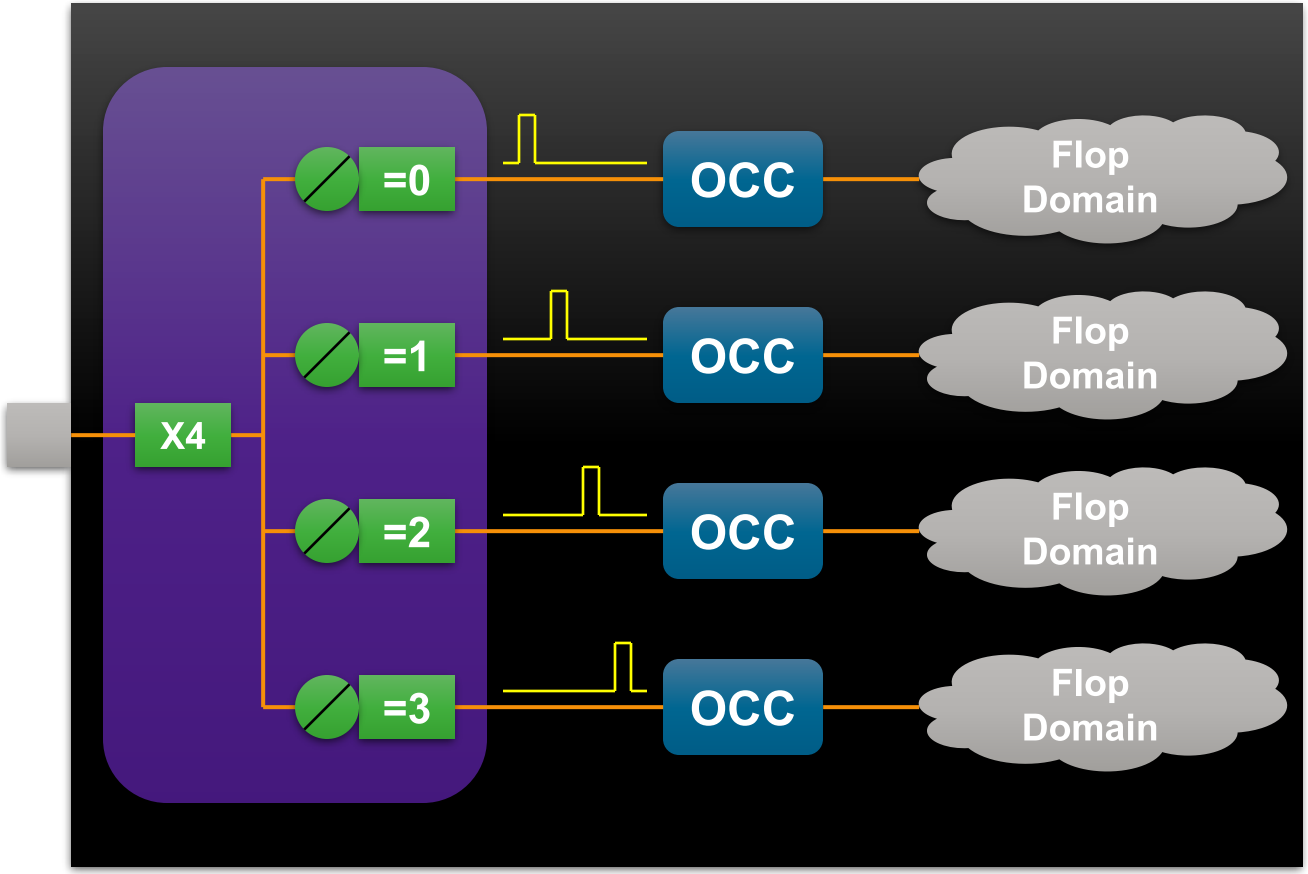
- Add delays in shift clock so that edges in various domains do not overlap



Internal Shift Clock Skewing Register Based

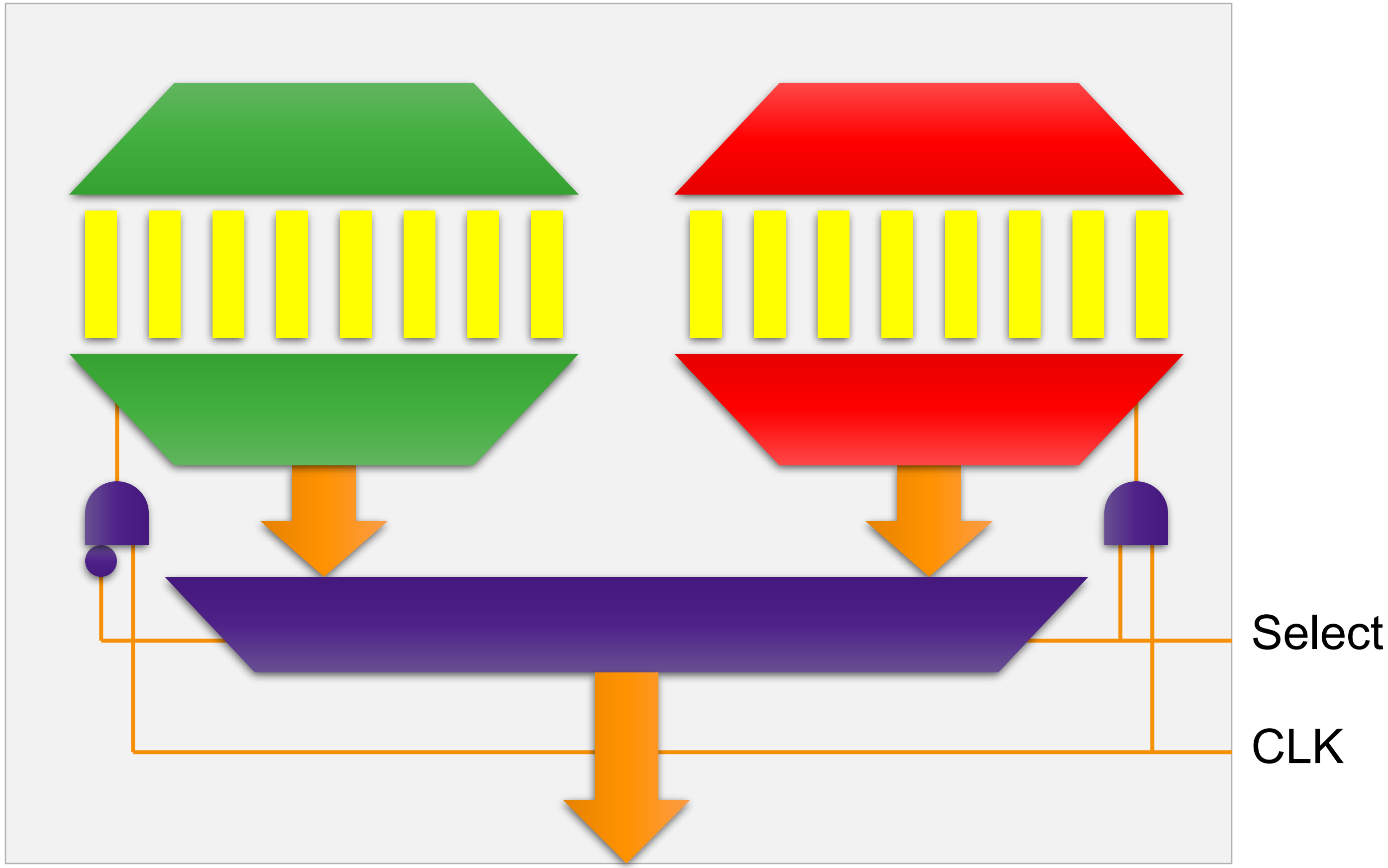
- Multiply up and down the external clock
- Pick out-of-phase clocks to drive various domains
- Use buffer for ATPG model

- Easily performed on designs using serialization and deserialization in the scan path data delivery infrastructure



Multiplexed `load_unload`

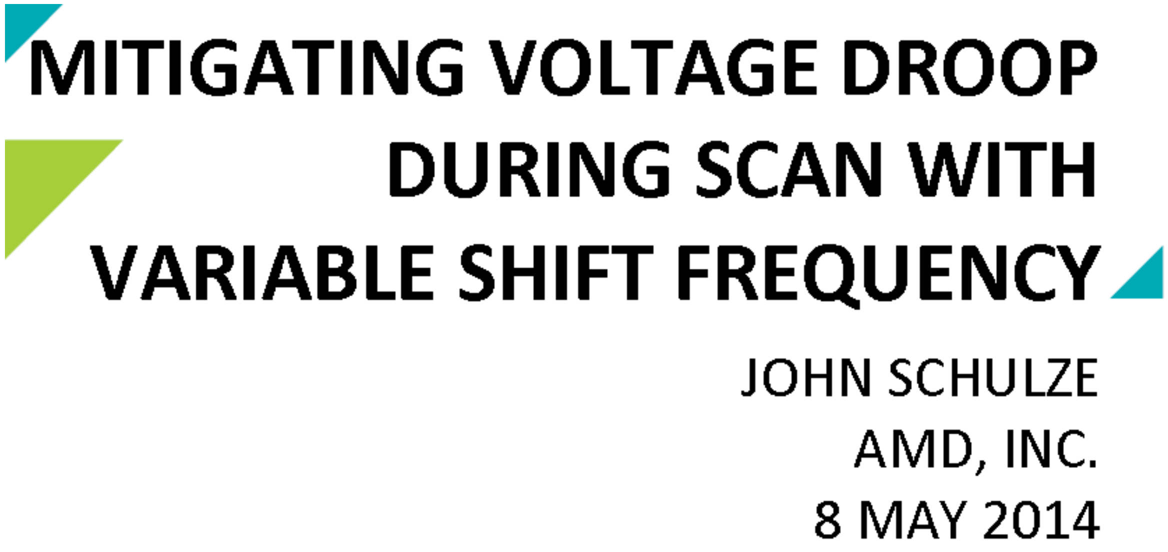
- Add DFT to control clocks such that all blocks do not shift at the same time (shift groups), but all capture at the same time



External Shift Clock Frequency Modulation

- (Based on AMD presentation at SWDFT and ITC 2014)
- Find a large voltage drop at the start of shift and adjust frequency to remove large drop
- Then speed up frequency again after some number of shifts have completed

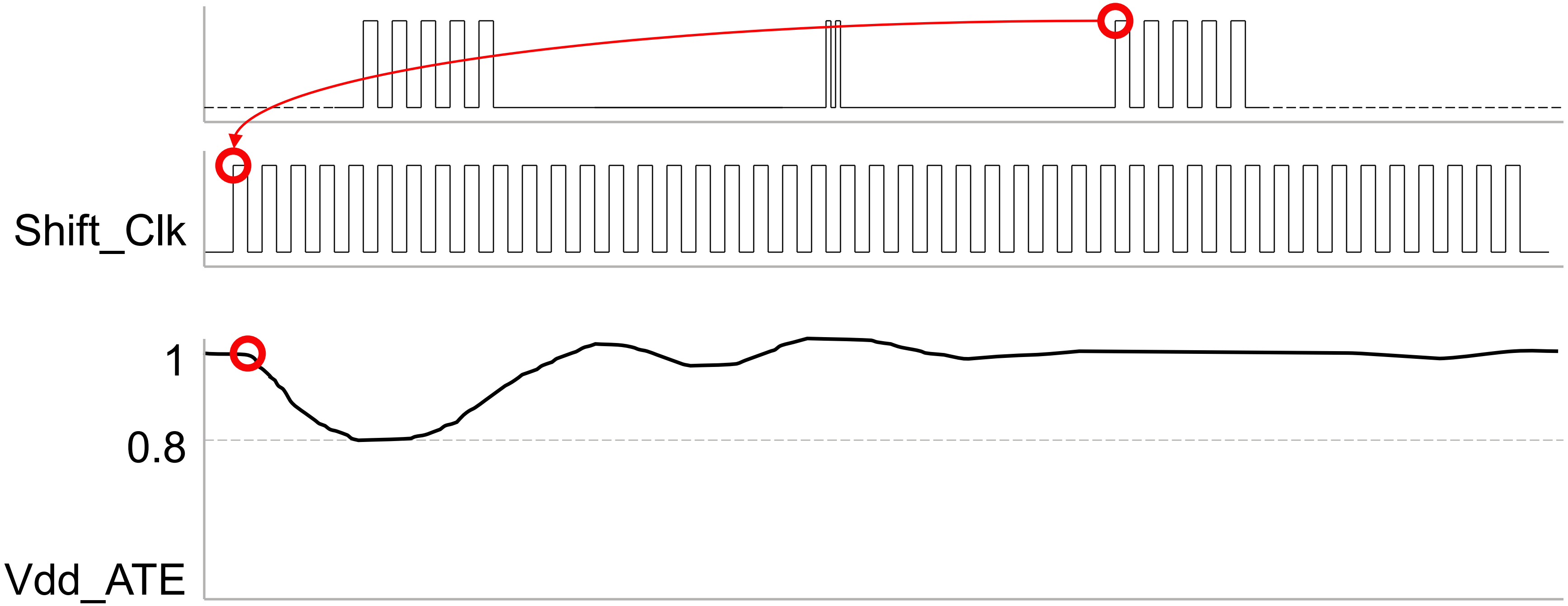
- The following slides were inspired by:

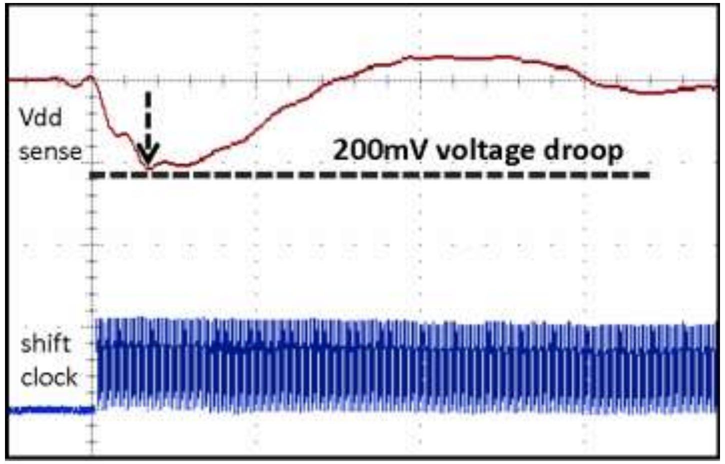


MITIGATING VOLTAGE DROOP
DURING SCAN WITH
VARIABLE SHIFT FREQUENCY

JOHN SCHULZE
AMD, INC.
8 MAY 2014

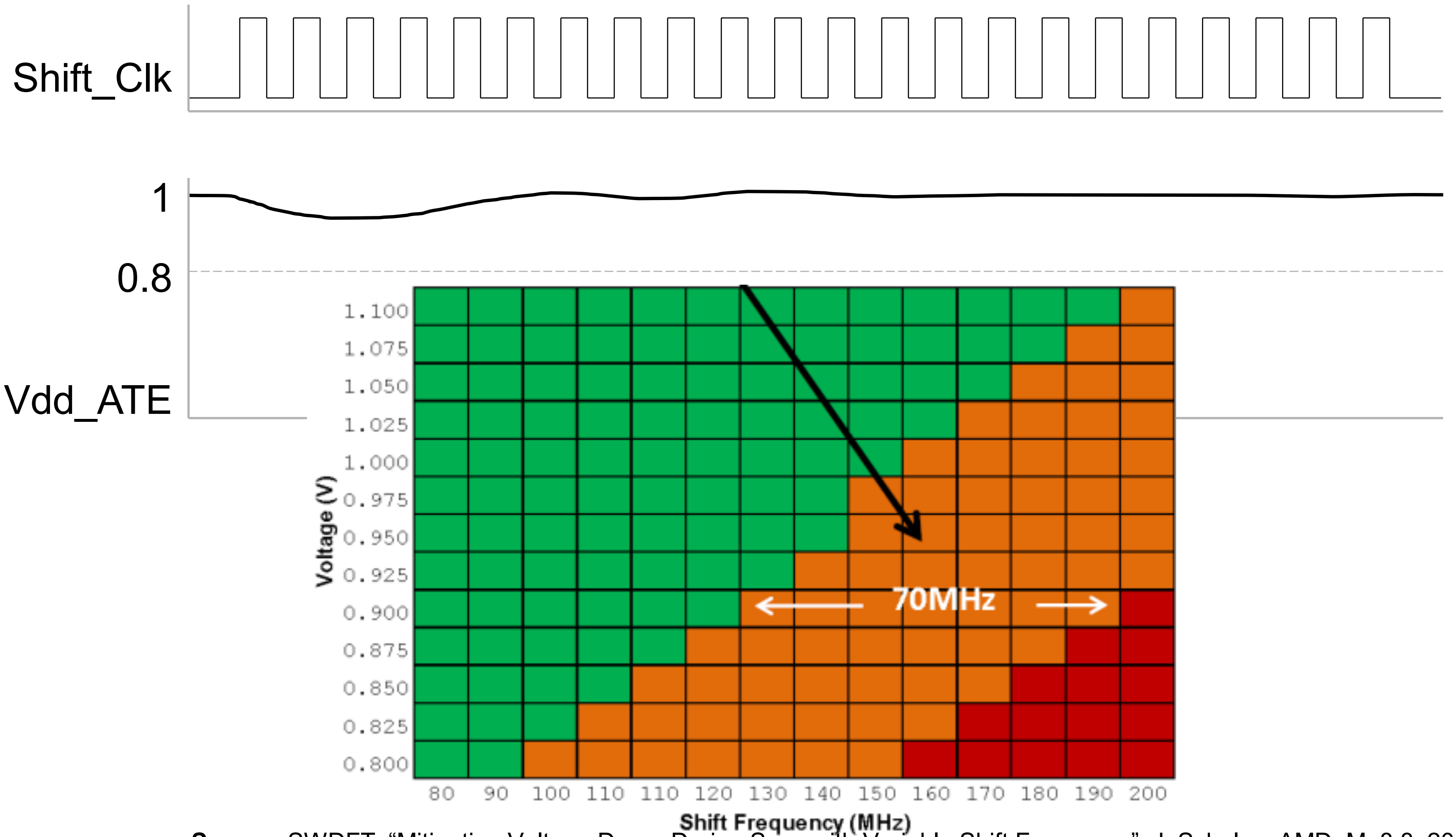
Large Voltage Droop During Shift





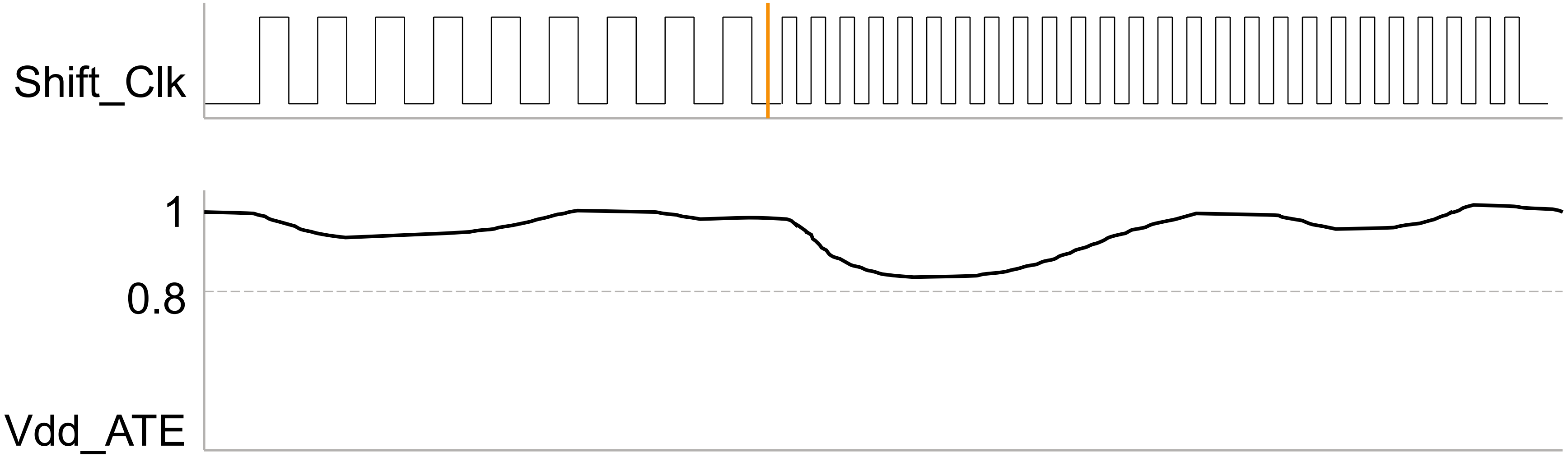
Source: SWDFT, “Mitigating Voltage Droop During Scan with Variable Shift Frequency”, J. Schulze, AMD, Ma8 8, 2014

Slow Down Shift Clock

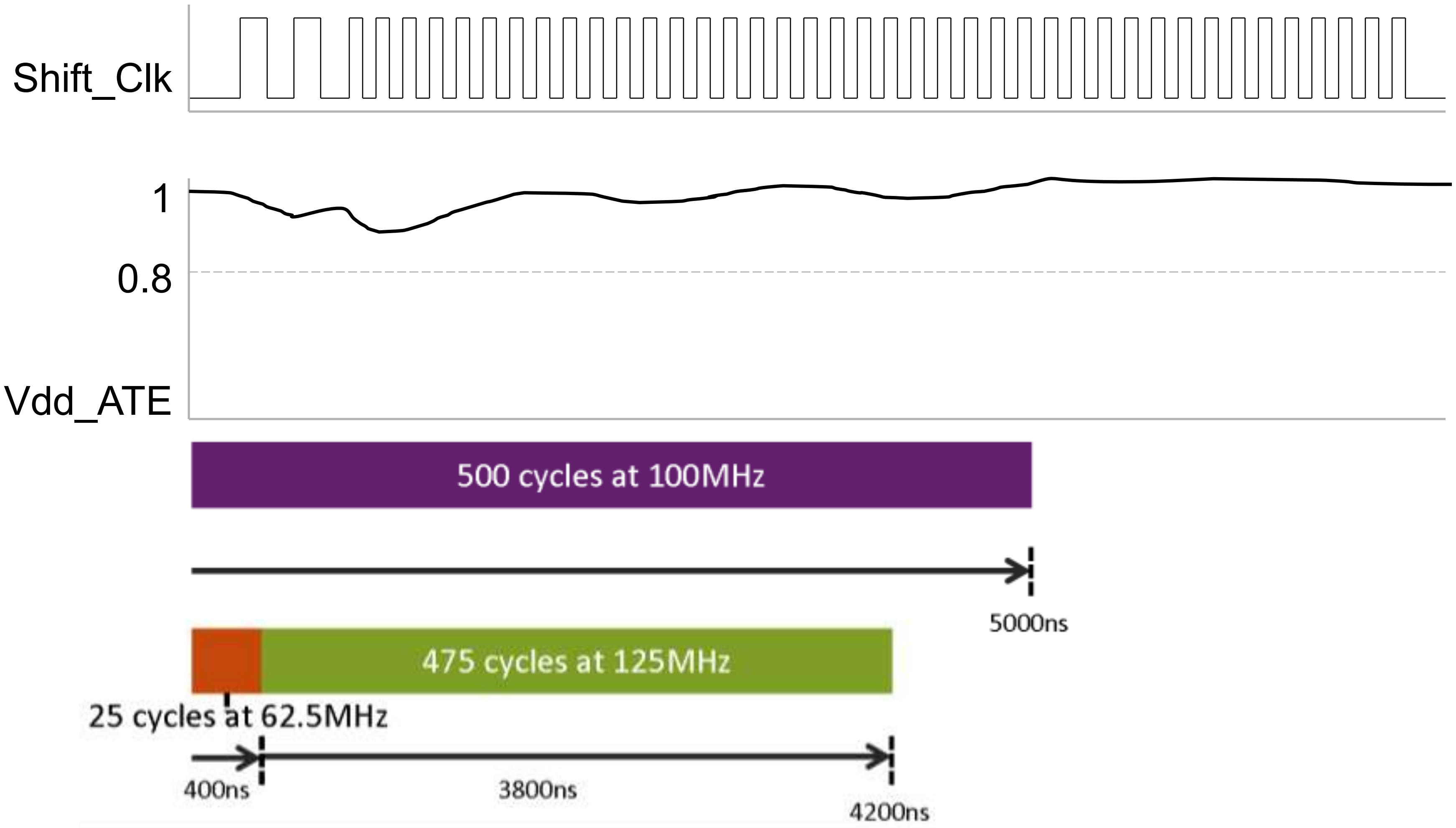


Source: SWDFT, “Mitigating Voltage Droop During Scan with Variable Shift Frequency”, J. Schulze, AMD, Ma8 8, 2014

Speed Shift Clock Up Later…



Find the Right Combination



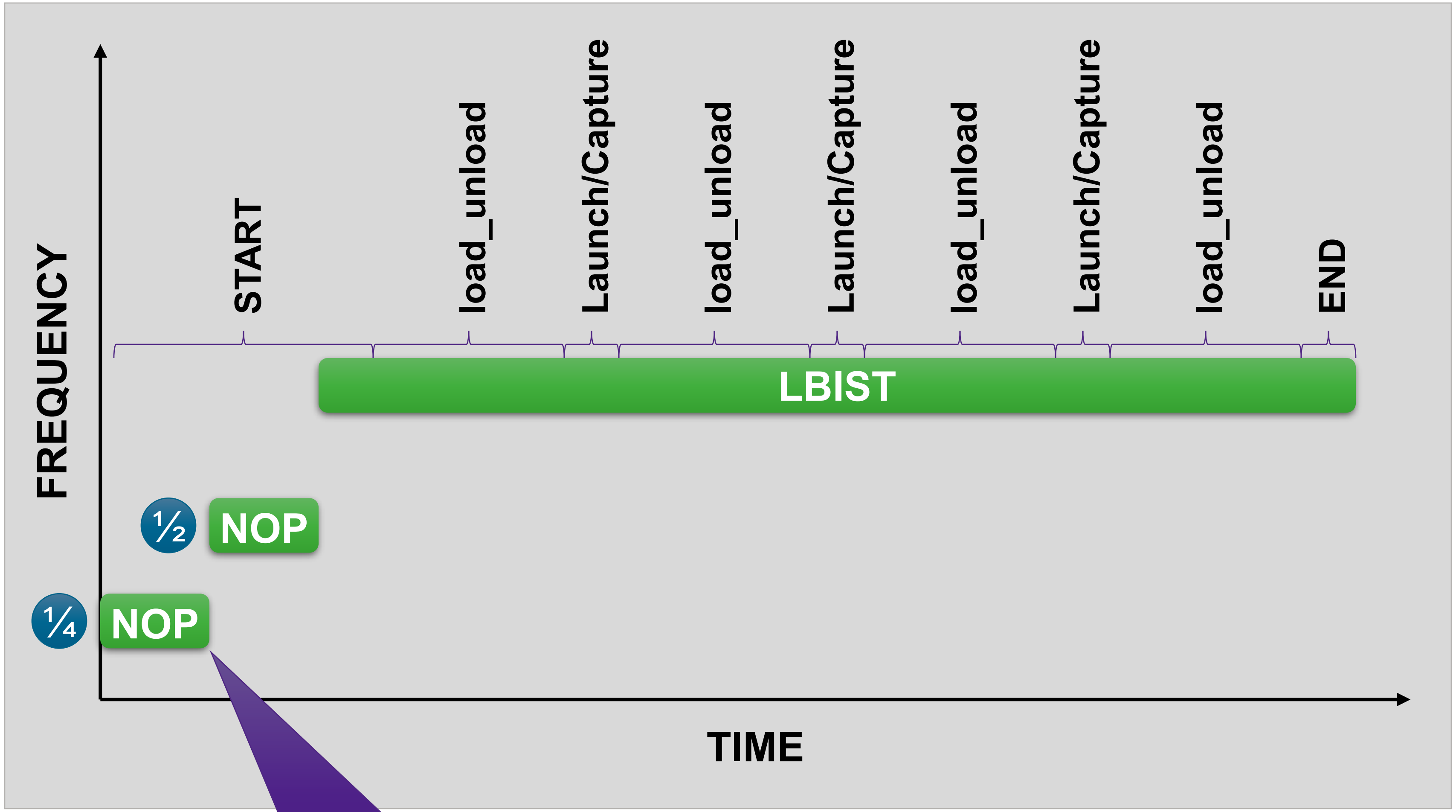
Source: SWDFT, “Mitigating Voltage Droop During Scan with Variable Shift Frequency”, J. Schulze, AMD, Ma8 8, 2014

Shift Speed in Normal LBIST Run

`set_logicbist_configuration -power_ramp_up disable`

LogicBIST Frequency Ramp-Up

```
set_logicbist_configuration -power_ramp_up enable
```



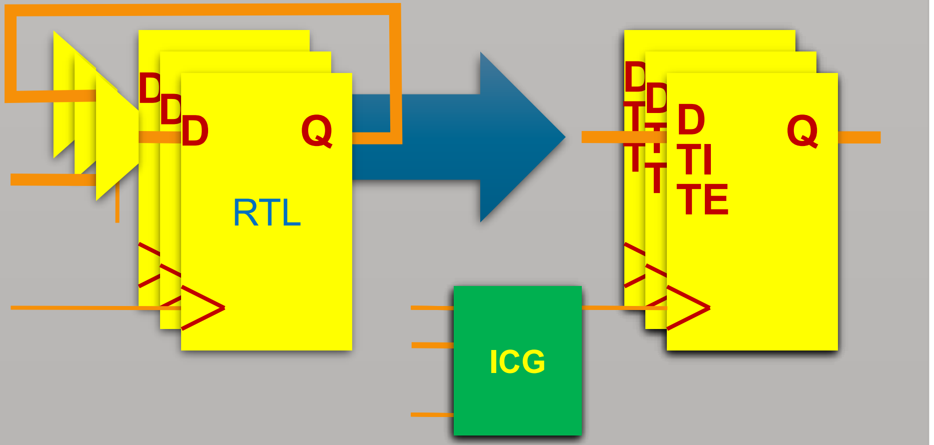
Slower Frequency load_unload Cycles

LogicBIST Frequency Ramp-Up and Down

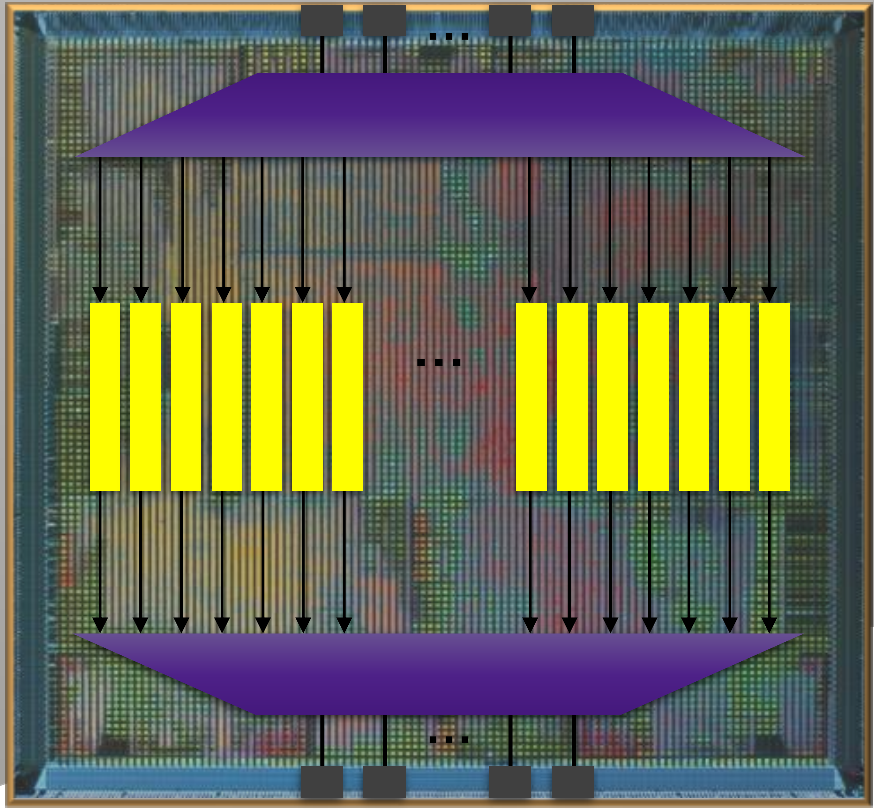
`set_logicbist_configuration -power_ramp_up enable -power_ramp_down enable`

Capture

```
compile_ultra -gate_clock -scan
```



```
set_dft_configuration -scan_compression enable
```



```
create_test_protocol
```

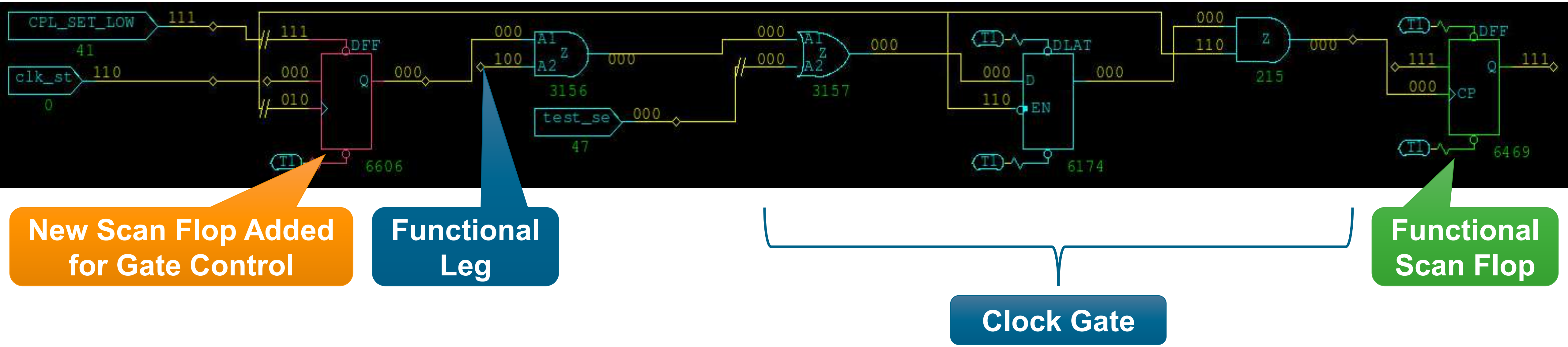
```
dft_drc
```

```
insert_dft
```

DFT To Limit Capture Power

- When requiring a hard capture power budget (`set_atpg -power_effort high`), this feature adds controllability resolution

`set_scan_configuration -capture_power_limit N`



New Scan Flop Added for Gate Control

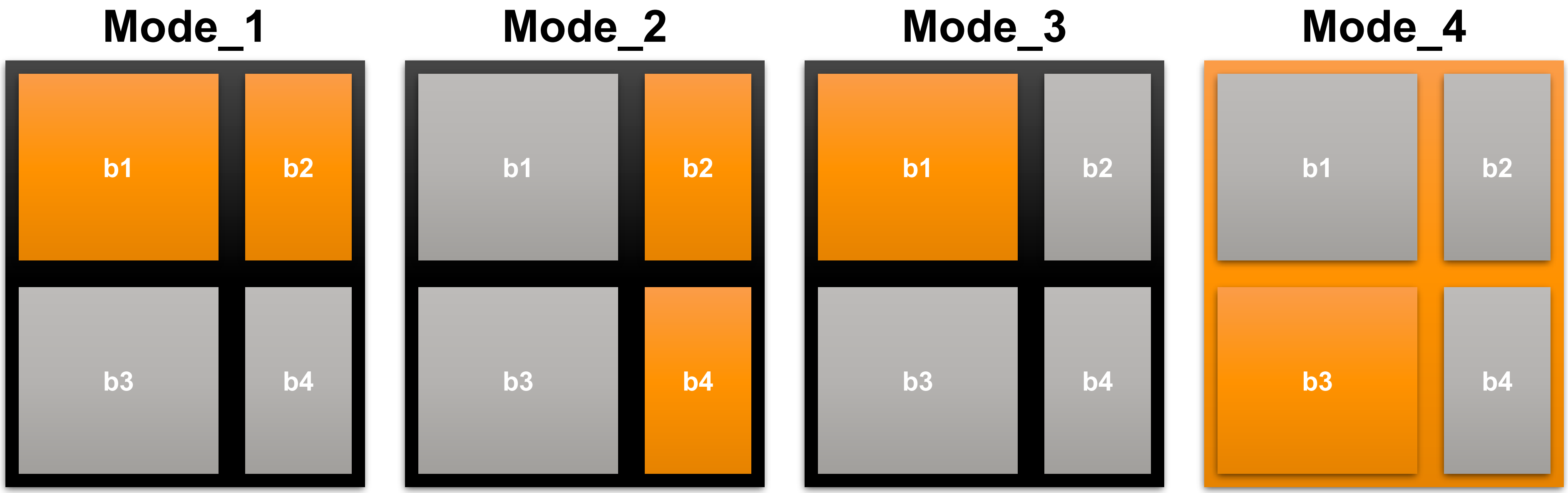
Functional Leg

Clock Gate

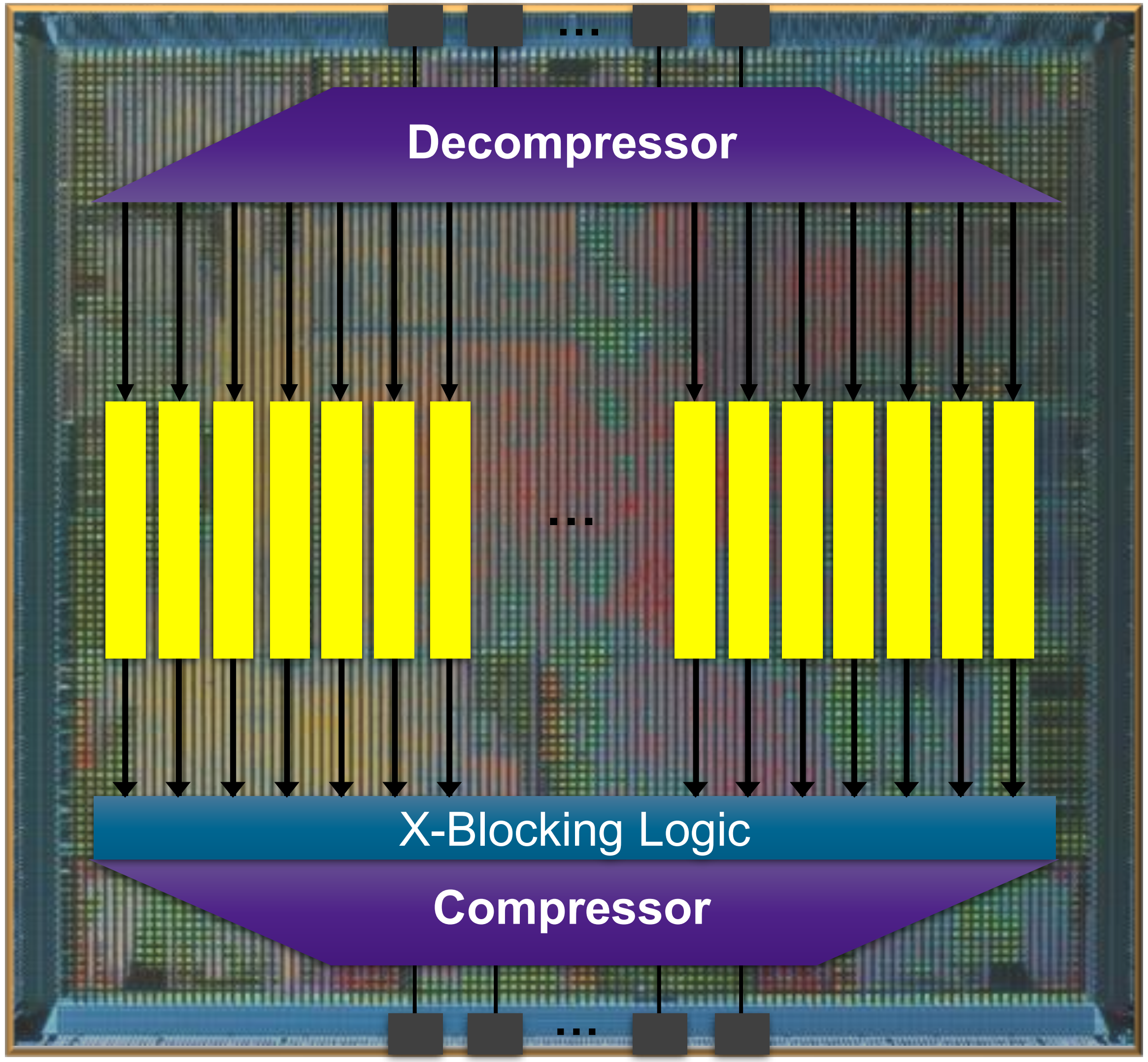
Functional Scan Flop

Block-at-a-Time

- Create more or redundant modes so that groups of modules can be tested serially, if required



Low-Power Compressor



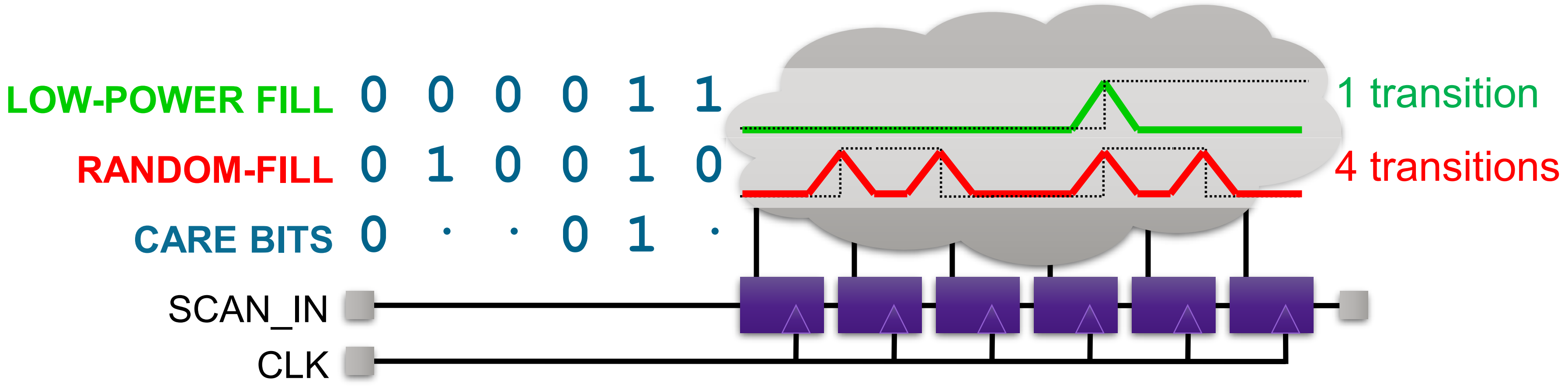
- Eliminates power consumption due to switching activity in the compressor during functional mode
- Eliminates the toggling activity in the DFTMAX compressor when the XOR tree is inactive
  - When SE inactive → no activity in the compressor

Patterns

Shift

Low-Power Fill During ATPG to Limit Shift Power

Reduces Switching During Shift



LOW-POWER FILL 0 0 0 0 1 1

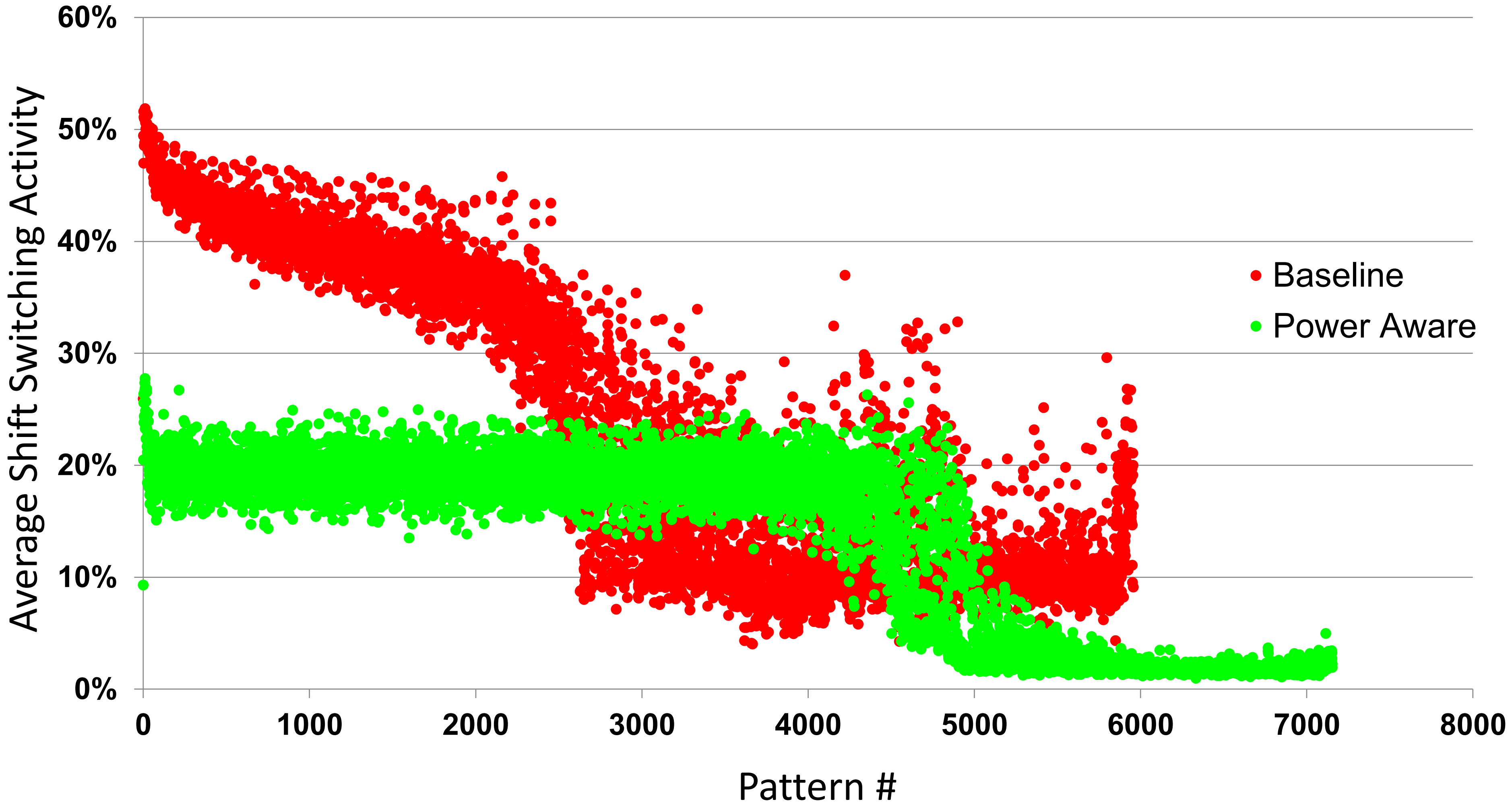
RANDOM-FILL 0 1 0 0 1 0

CARE BITS 0 · · 0 1 ·

1 transition

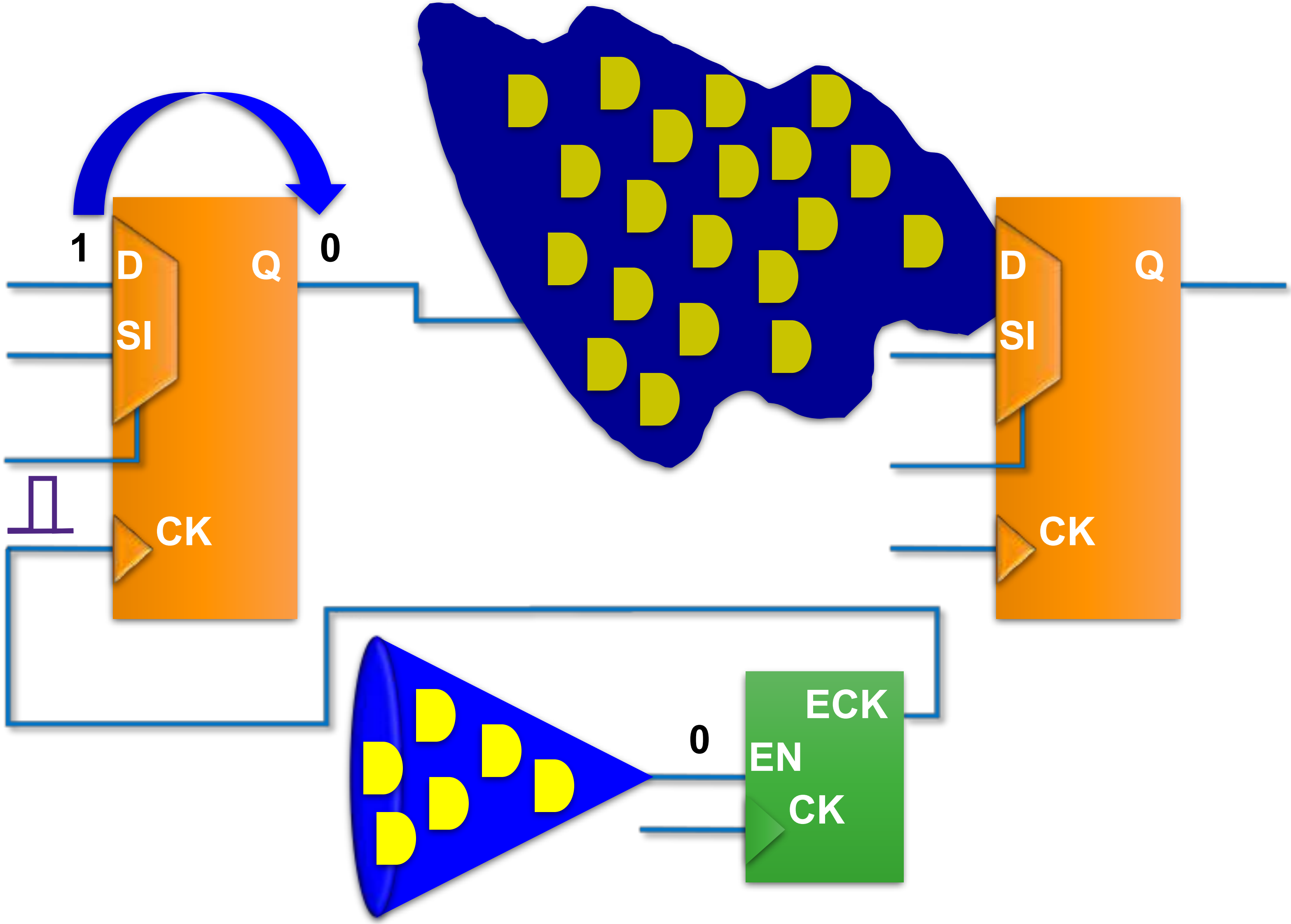
4 transitions

Shift Power Reduction

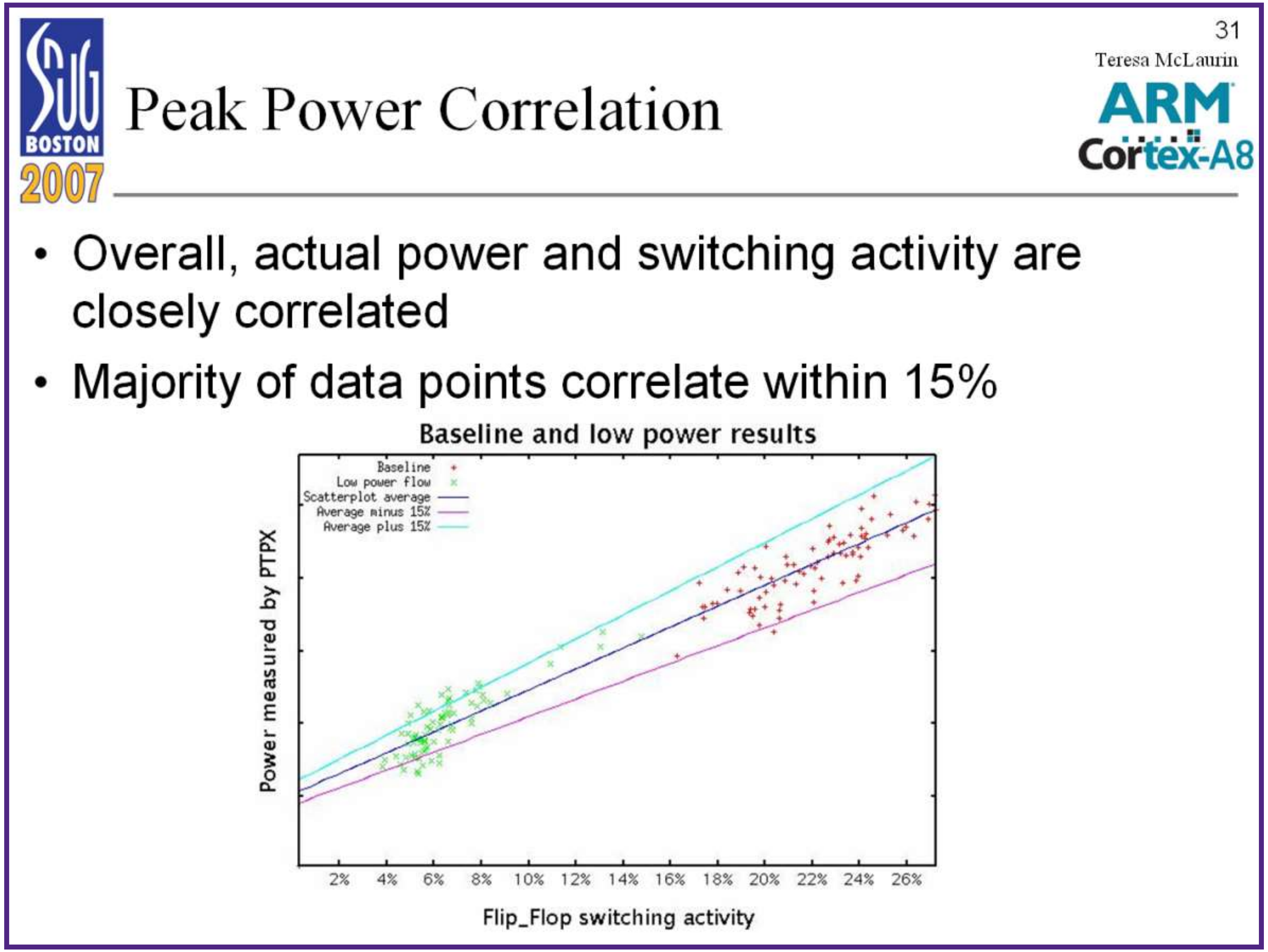


Capture

Power-Aware ATPG for Capture Power Reduction



Flop Switching and Power Correlation



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Teresa McLaurin

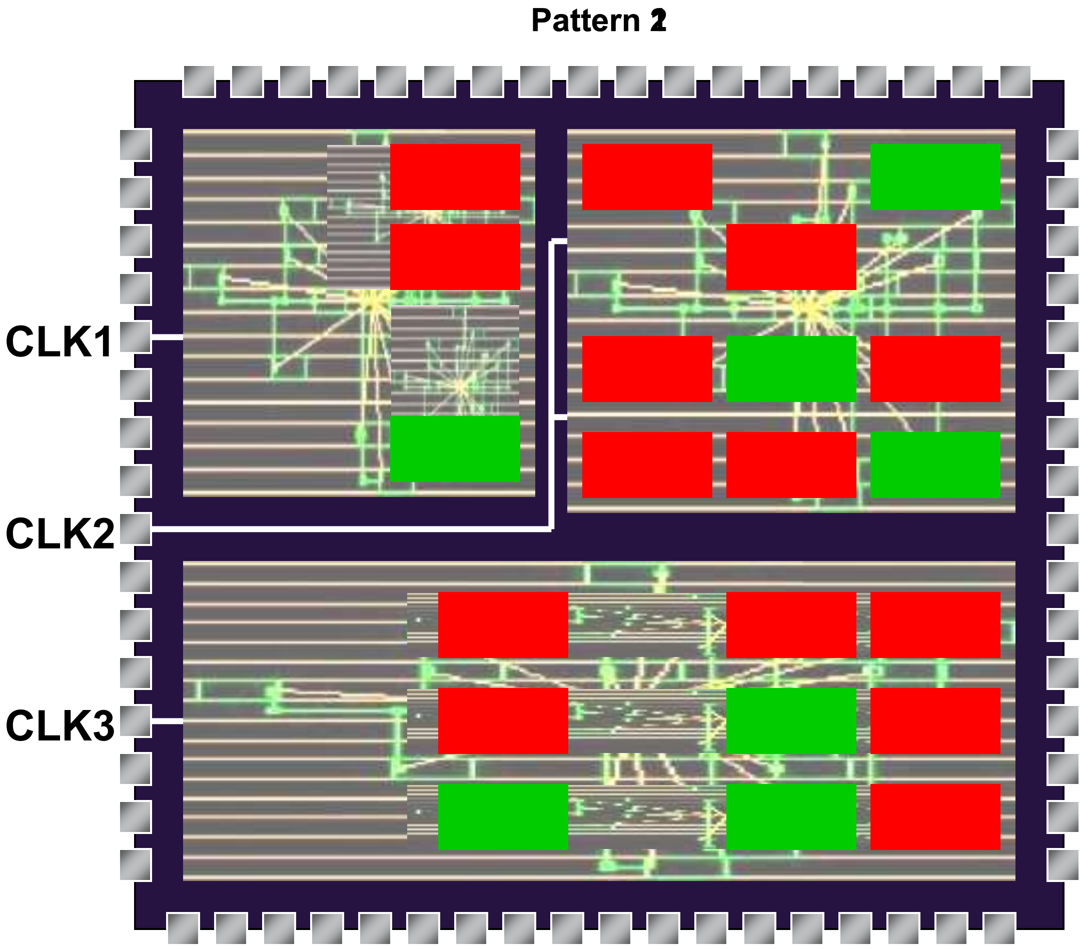
Peak Power Correlation

- Overall, actual power and switching activity are closely correlated
- Majority of data points correlate within 15%

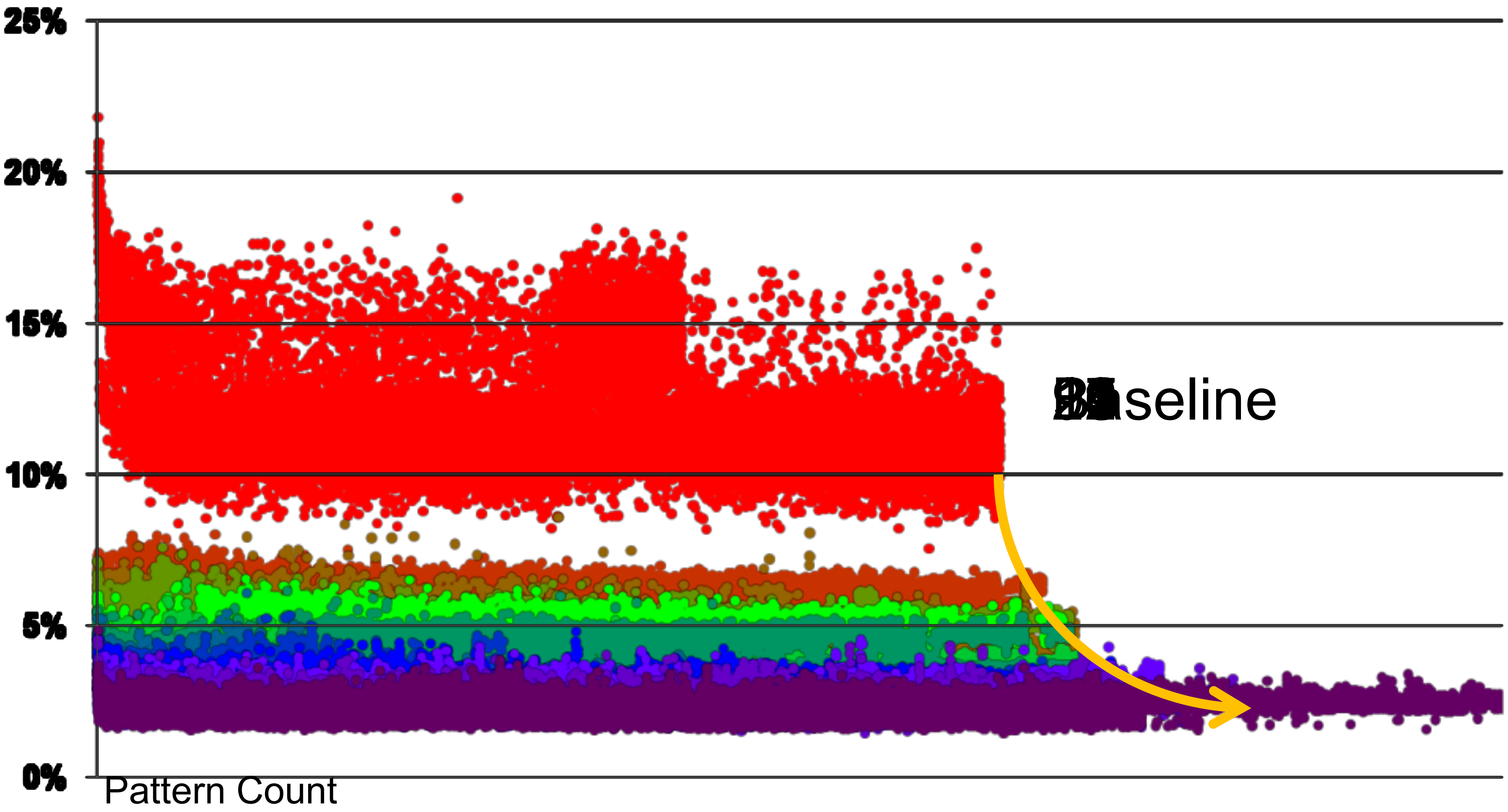
Baseline and low power results

ATPG Meets Power Budget With Fine-Grained Clock Control

- ATE clocks
- On-chip **C**lock **C**ontroller
- **C**lock **G**ating **C**ell
- Automatically meets power budget
- Avoids over-constraining ATPG



Peak Capture Switching Percent

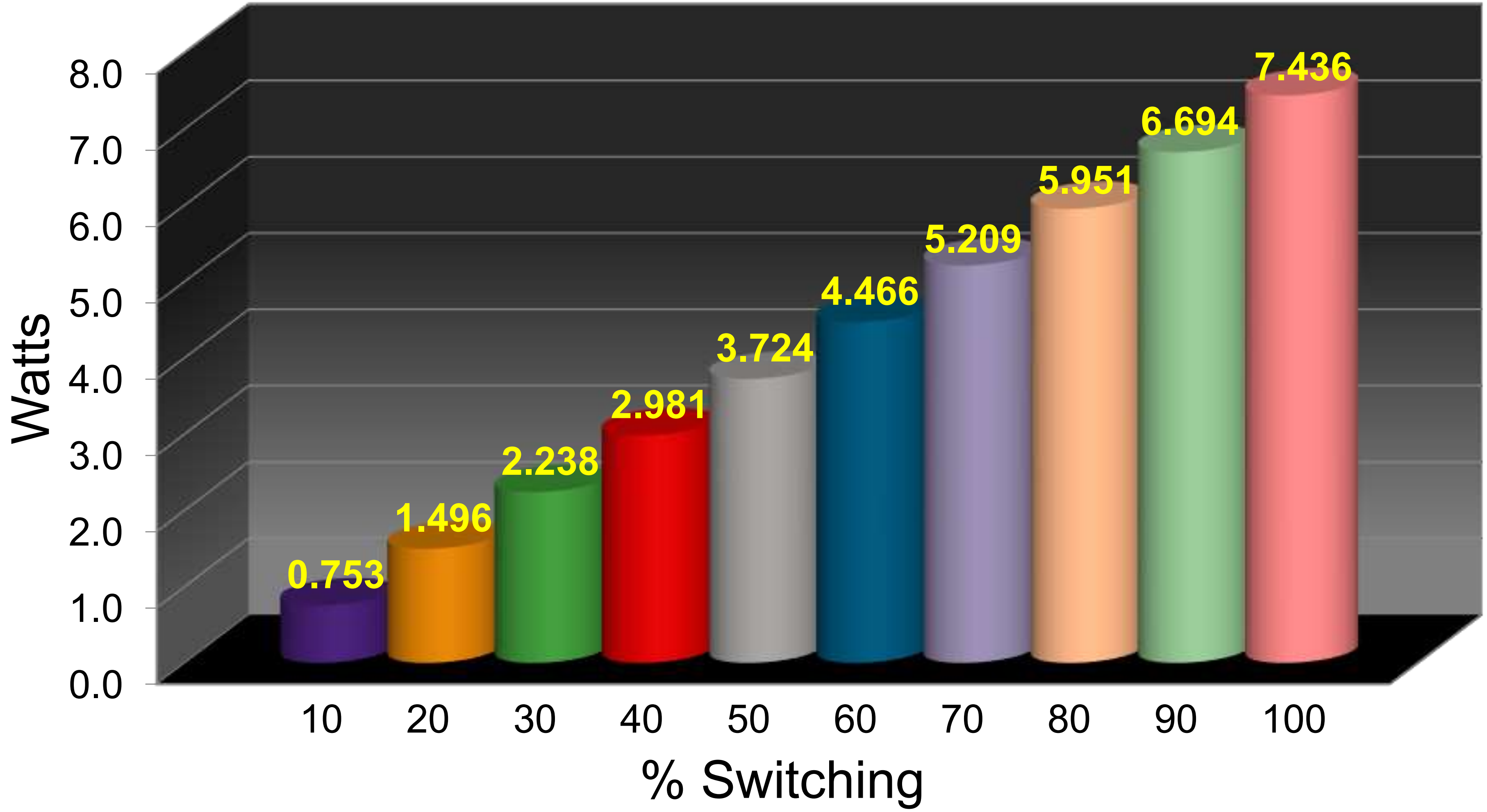


Baseline

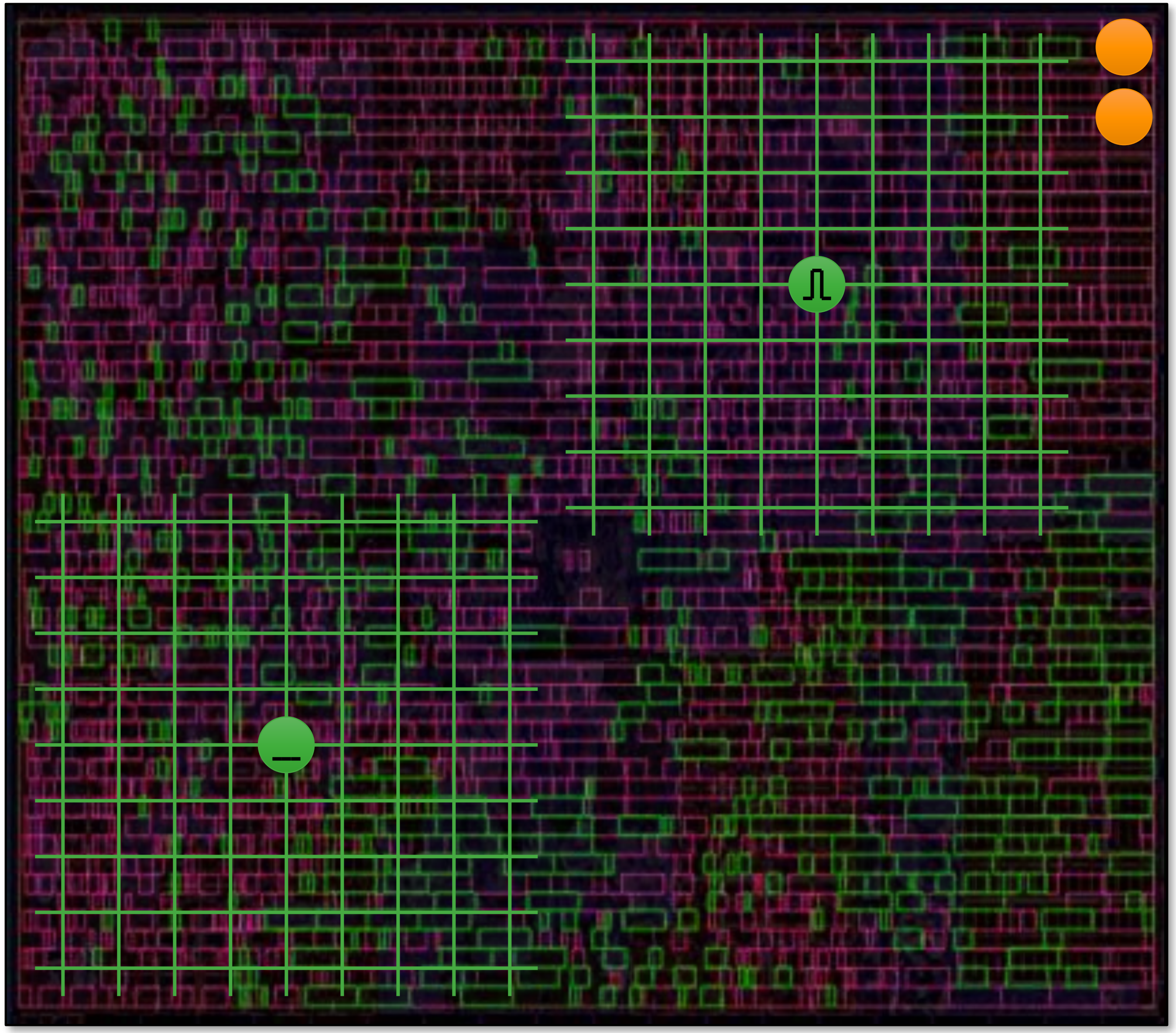
Correlation

Pre-Tapeout

Switching vs. Power (~10-year-old method)

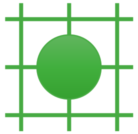


Power Grid – For Illustration Purposes, Only



● VDD

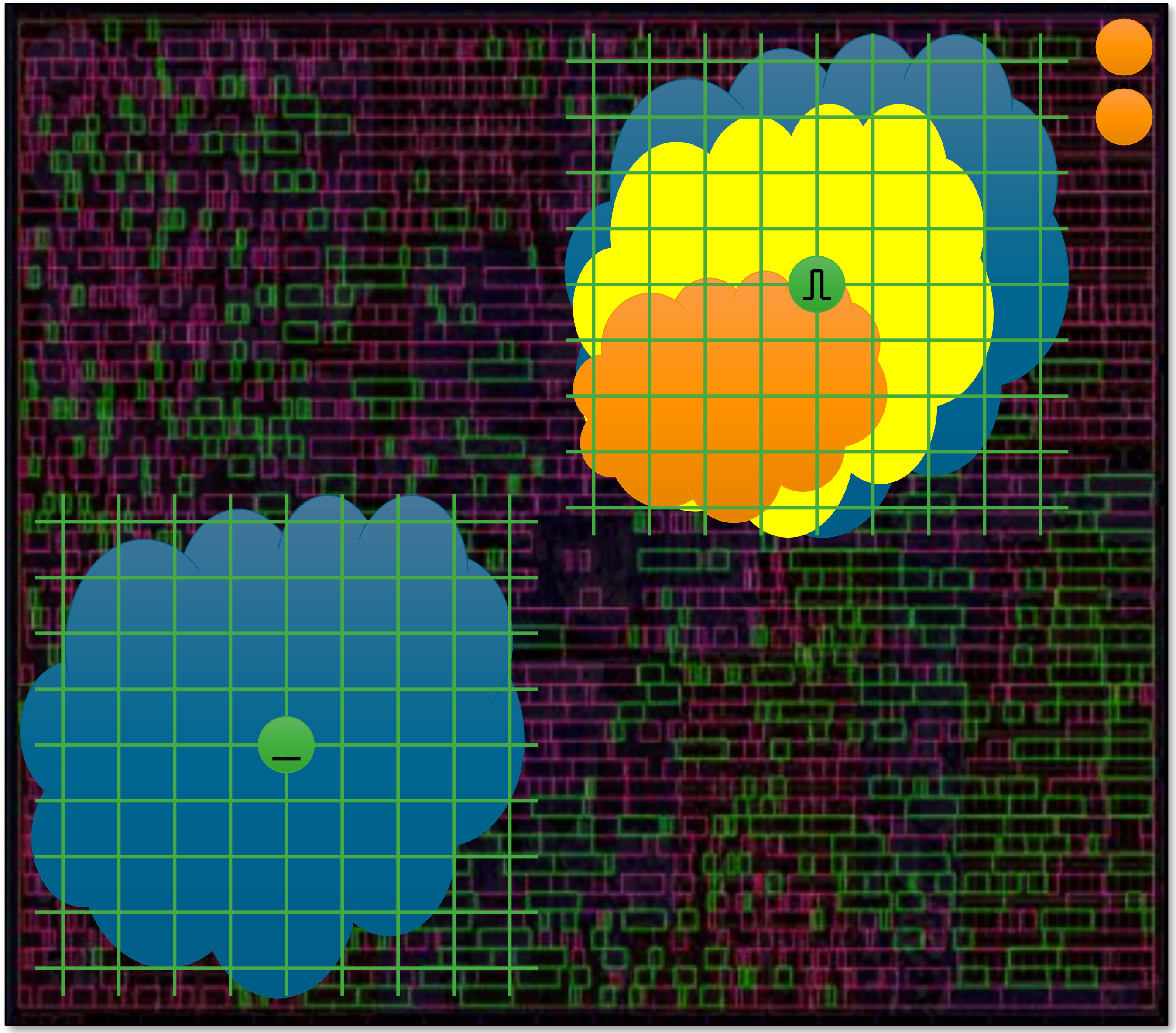
● VSS



= OCC and Clock Mesh

- Same design in 2 places
- Same pattern set applied

Power Grid – For Illustration Purposes, Only

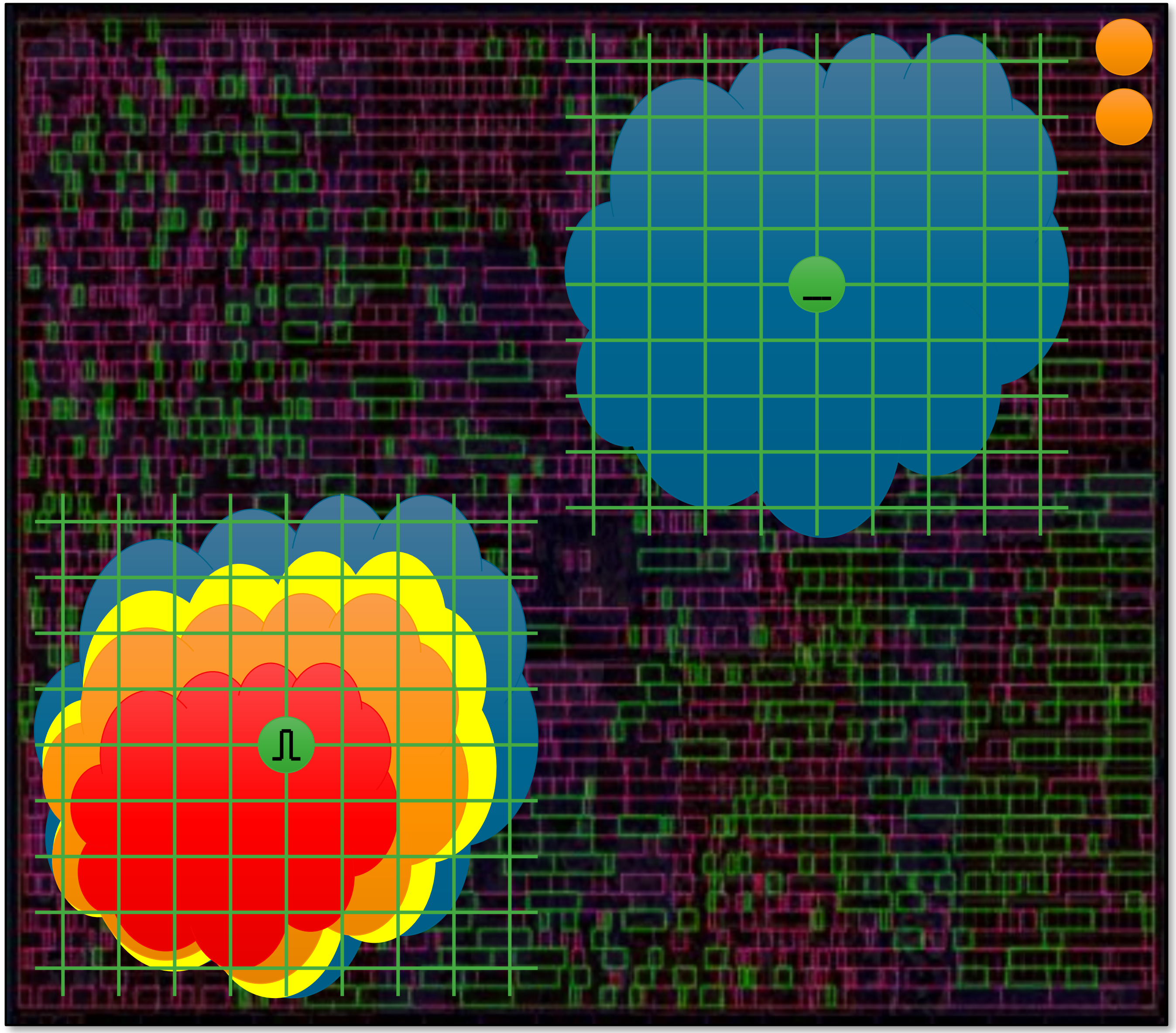


● VDD

● VSS

- IR-drop close to power source pins

Power Grid – For Illustration Purposes, Only



● VDD

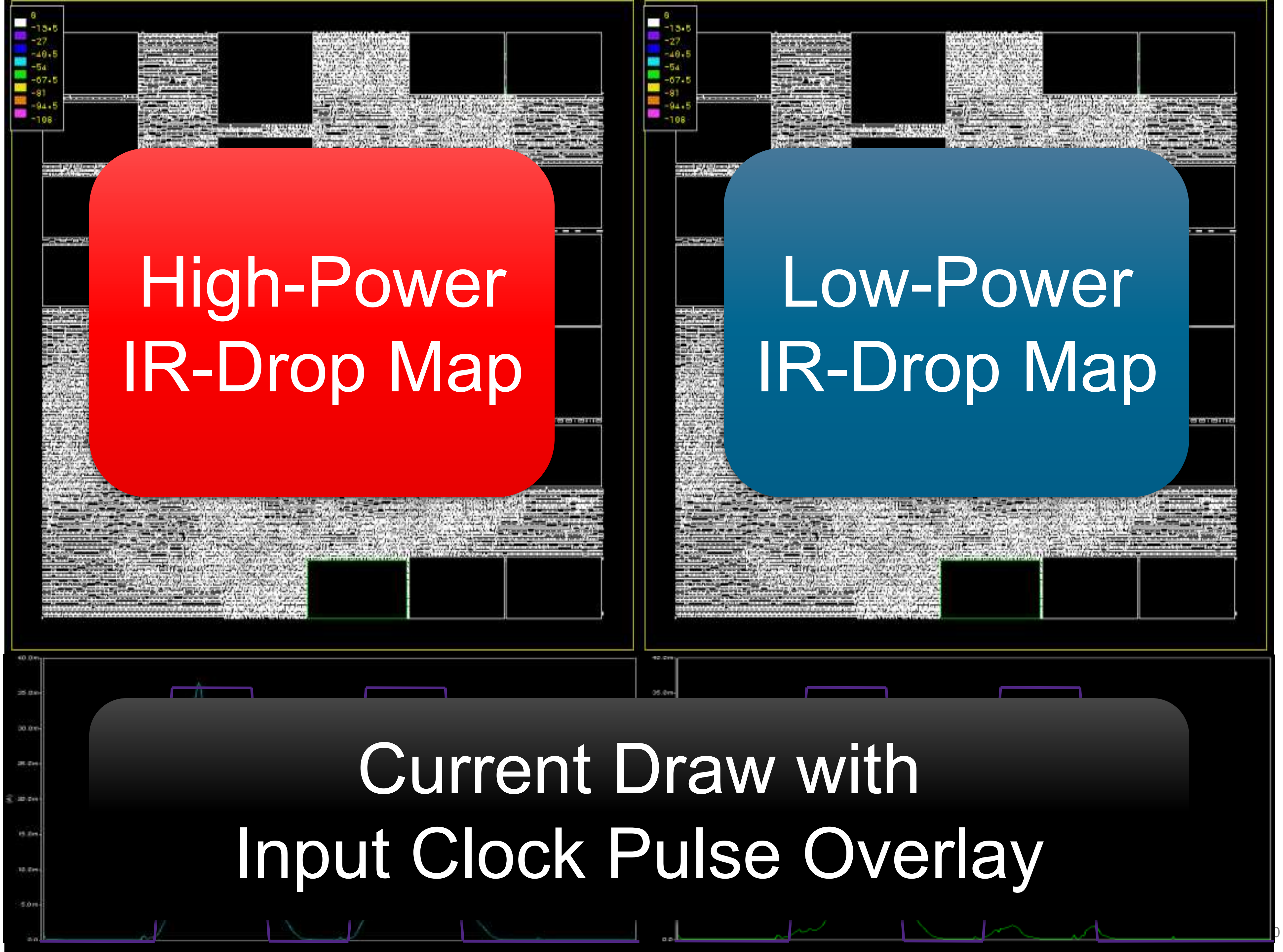
● VSS

- IR-drop far from power source pins

PrimeRail Side-by-Side

- PrimeTime-PX results

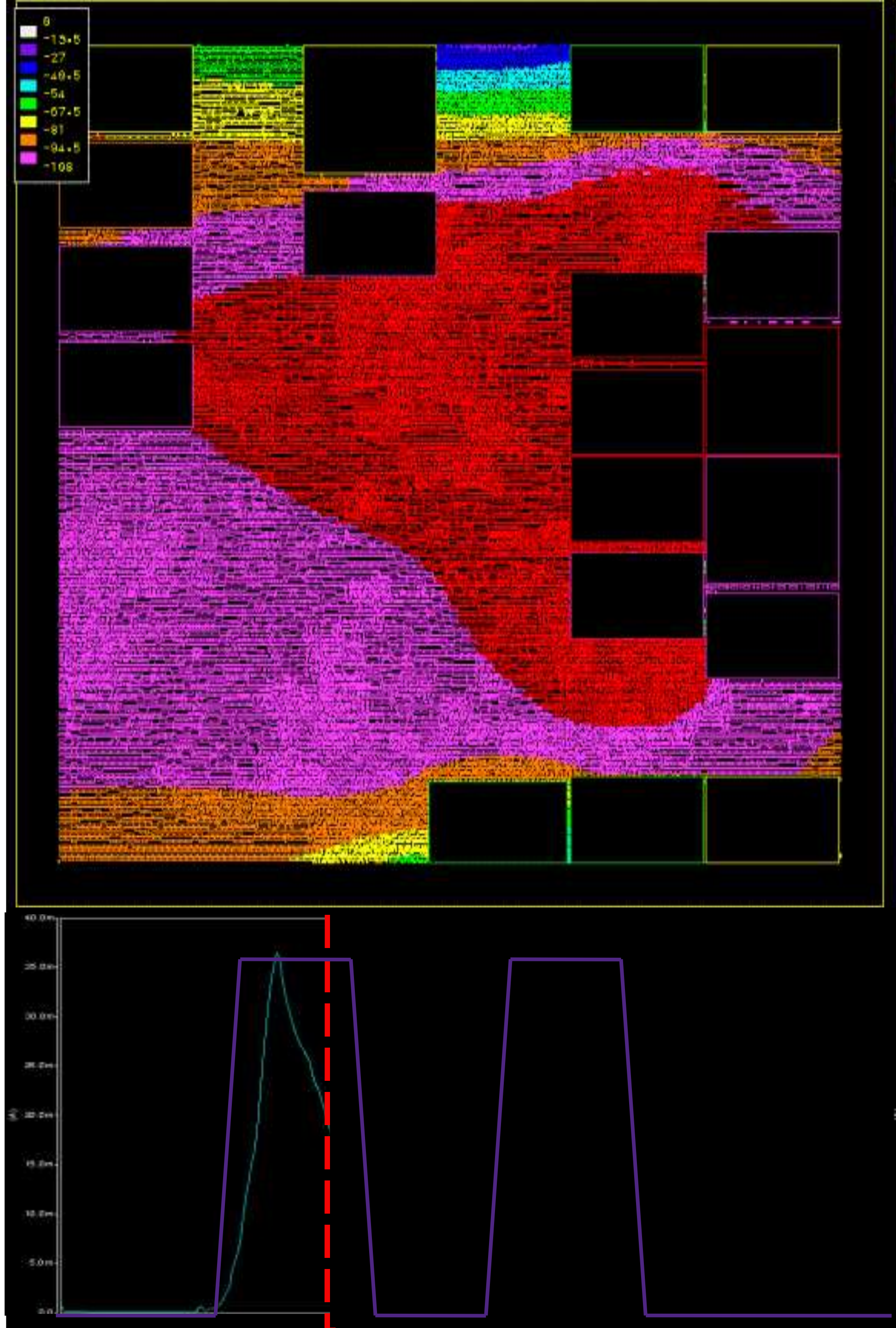
```
read_vcd high_power.vcd -strip AAA_tmax_testbench_1_16/dut \
 -time {3500 3800}
```

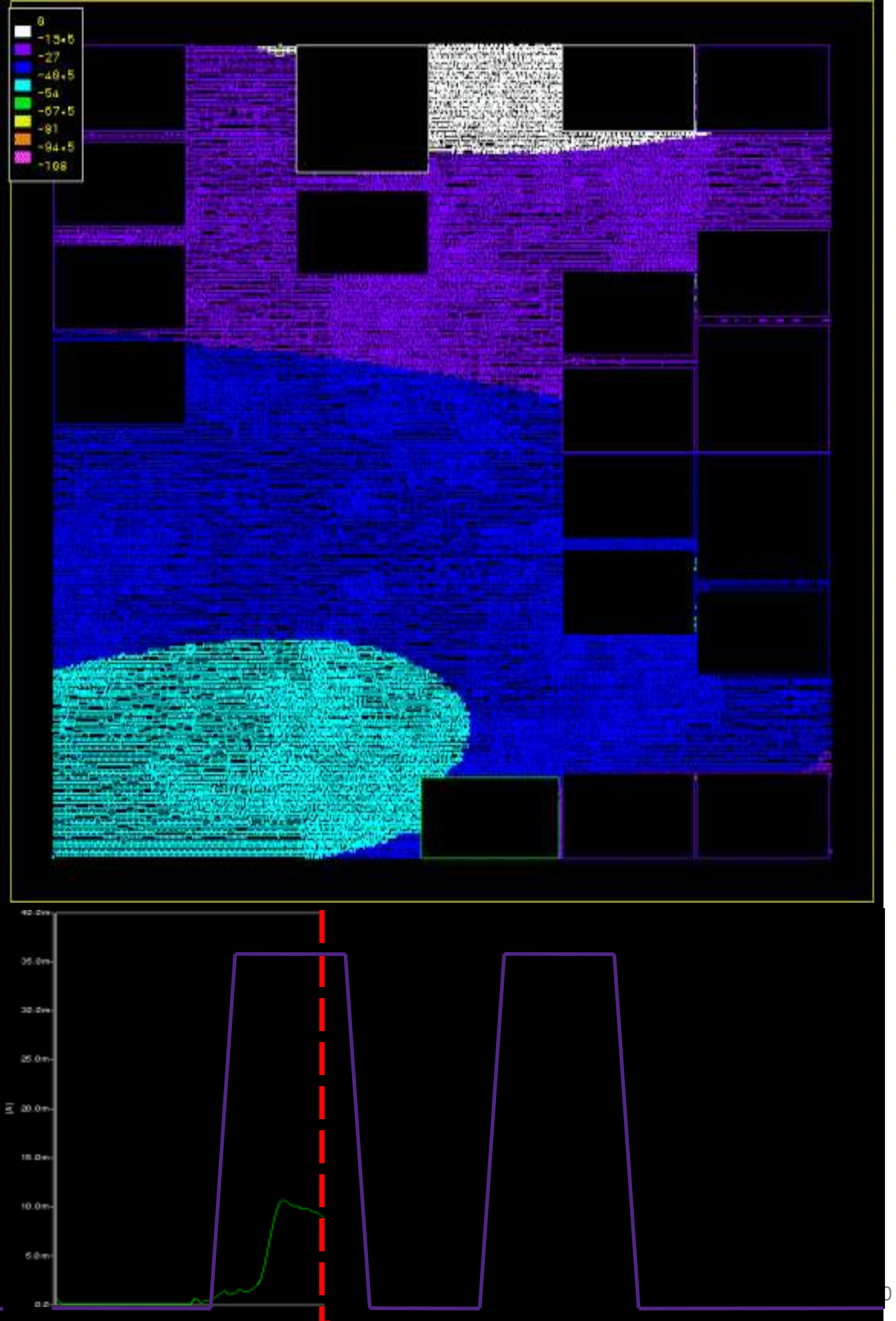


High-Power
IR-Drop Map

Low-Power
IR-Drop Map

Current Draw with
Input Clock Pulse Overlay


0
-13.5
-27
-40.5
-54
-67.5
-81
-94.5
-108
40.0m
35.0m
30.0m
25.0m
(A)
20.0m
15.0m
10.0m
5.0m
0.0


0
-13.5
-27
-40.5
-54
-67.5
-81
-94.5
-108
40.0m
35.0m
30.0m
25.0m
(A)
20.0m
15.0m
10.0m
5.0m
0.0

Technology Has Evolved

- Old techniques used flip-flop switching as a proxy for power
- Some tools supported combinational gates, as well

- But a correlation was still required, and reporting was only as good as the input models

- New technology uses power models to drive ATPG metrics and settings
- Flop switching, clock pulsing, combinational logic toggling, and memory accesses all drive results

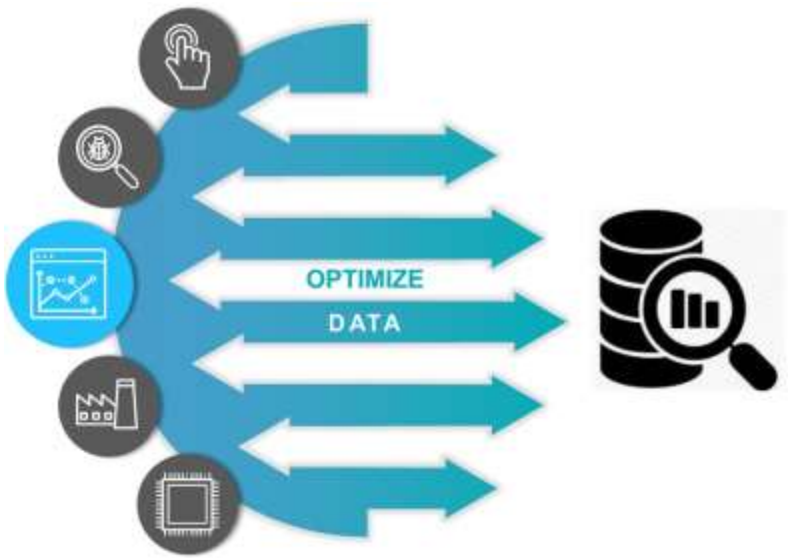
- Idea is to set WATTS as a threshold, and report results in watts

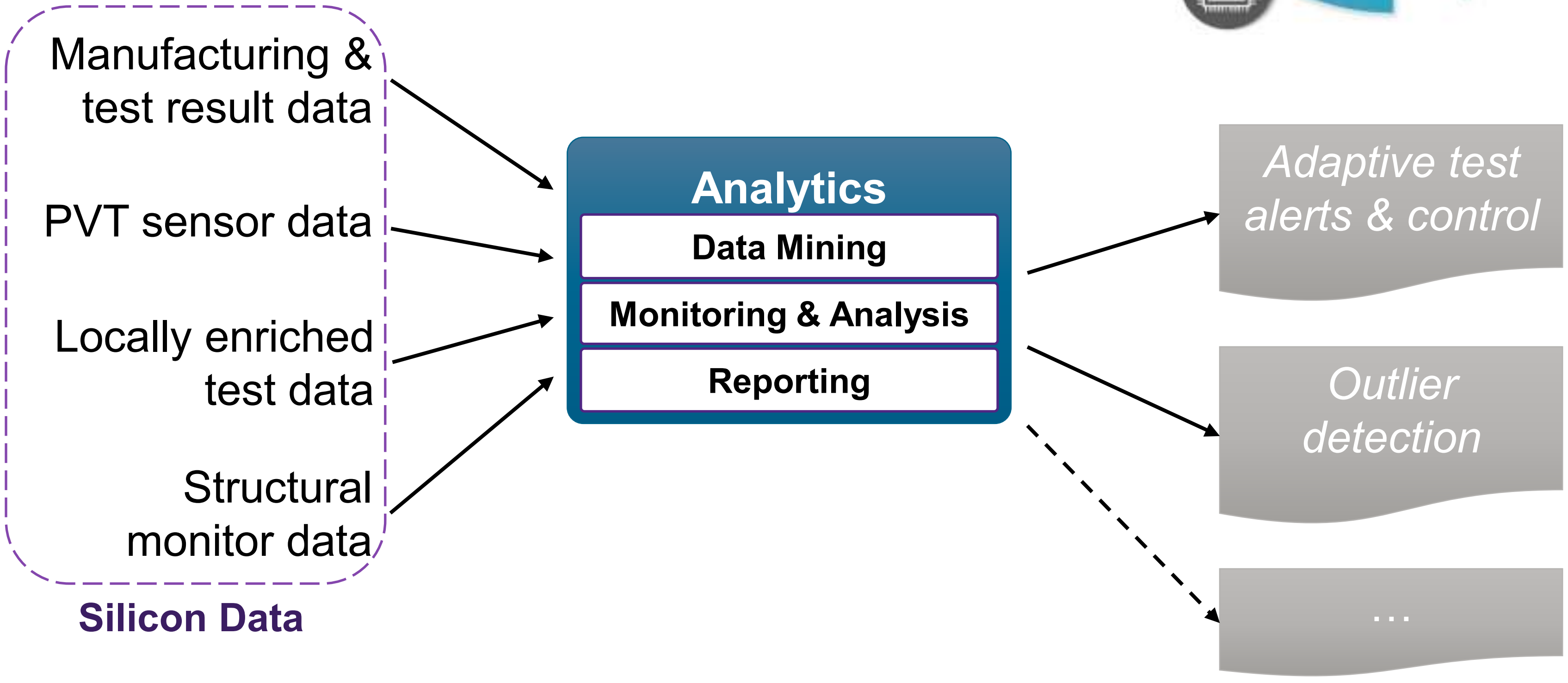
Post-Tapeout

Test Optimization

Test, in-chip monitoring, analytics

- Adapt tests and screening criteria through ongoing analysis of silicon and manufacturing test data
- Enhanced decisions for reliability & quality





Manufacturing & test result data

PVT sensor data

Locally enriched test data

Structural monitor data

Silicon Data

Analytics

Data Mining

Monitoring & Analysis

Reporting

Adaptive test alerts & control

Outlier detection

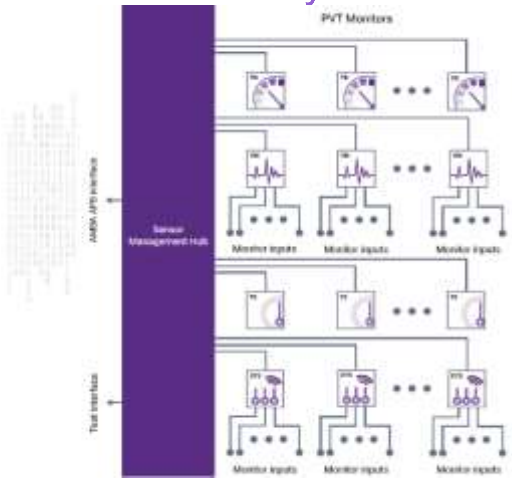
…

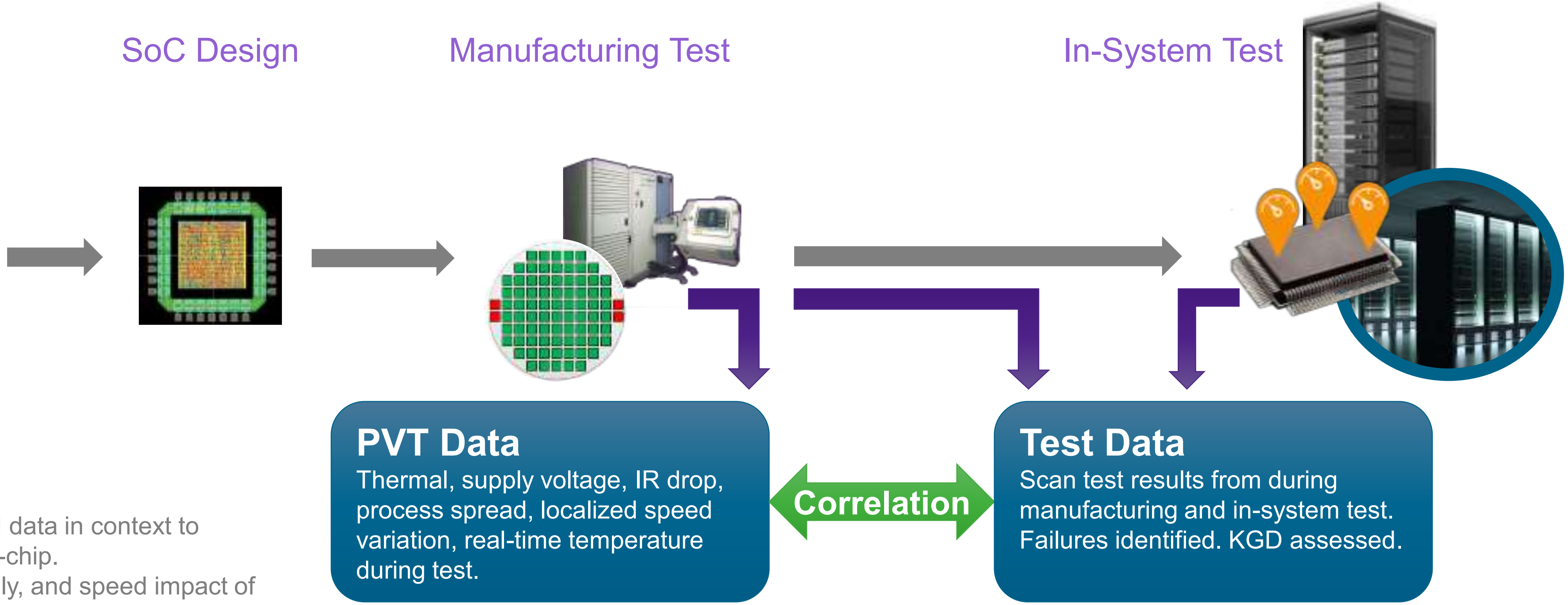
PVT Aware SCAN Testing

Failing product correlated to in-chip PVT conditions

Design → Production → In-field

PVT Monitoring Subsystem IP





PVT Data
Thermal, supply voltage, IR drop, process spread, localized speed variation, real-time temperature during test.

Correlation

Test Data
Scan test results from during manufacturing and in-system test. Failures identified. KGD assessed.

Use Case

- Assessment of SCAN data in context to physical conditions in-chip.
- Assess thermal, supply, and speed impact of failing devices.

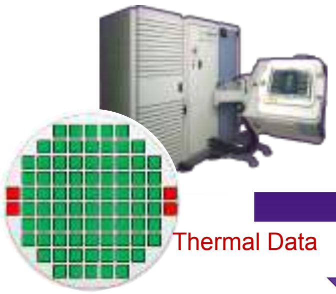
Thermally Aware SCAN Testing

SCAN test speed modulated by in-chip temperature

Production **In-field**

Manufacturing Test

In-System Test



Thermal Data

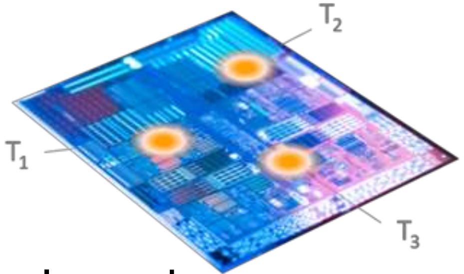
Thermal Data

Thermal clock throttling during SCAN

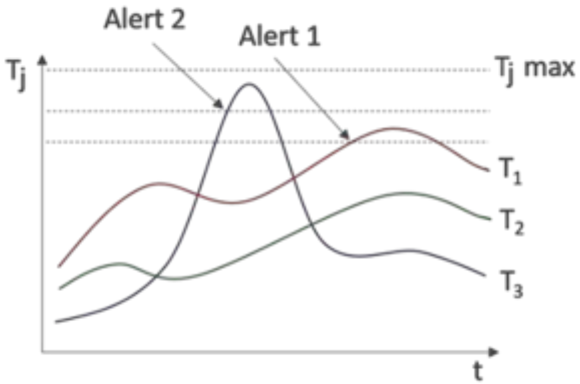
- Optimise SCAN frequency
- Avoid thermal runaway during test
- Reduce device stress

High accuracy in-chip temperature measurement

- Tighten thermal guard-banding
- Optimise testing for high-volume



On-die thermal sensing



Dynamic Frequency Scaling (DFS)

SCAN Frequency

Thank You

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MEPTEC
THE NEXT GENERATION

ADVANTEST®

A **global leader** in the ATE industry with a WW installed base of over 30,000 systems

Our nanotechnology products support leading-edge semiconductor processes at the **1Xnm node**

Our diverse workforce includes **5,500 employees** from **50 countries**

Eco-friendly policies emphasize reduction of our carbon footprint

2018 THOMSON REUTERS
TOP100
GLOBAL TECH LEADER

2018 Global Technology Leader by Thomson Reuters

60+

Innovating in the measurement arena for **60+ years**

VLSIresearch
THE BEST SUPPLIERS
Customer Satisfaction
2020

A VLSIresearch 10 BEST supplier for **32** consecutive years

Amkor's Differentiators

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Advanced Packaging Leadership
Engineering Services
Broad Portfolio

Quality

QualityFIRST Culture
Execution
Automation

Service

Design & Test Through Drop Ship
Manufacturing Footprint
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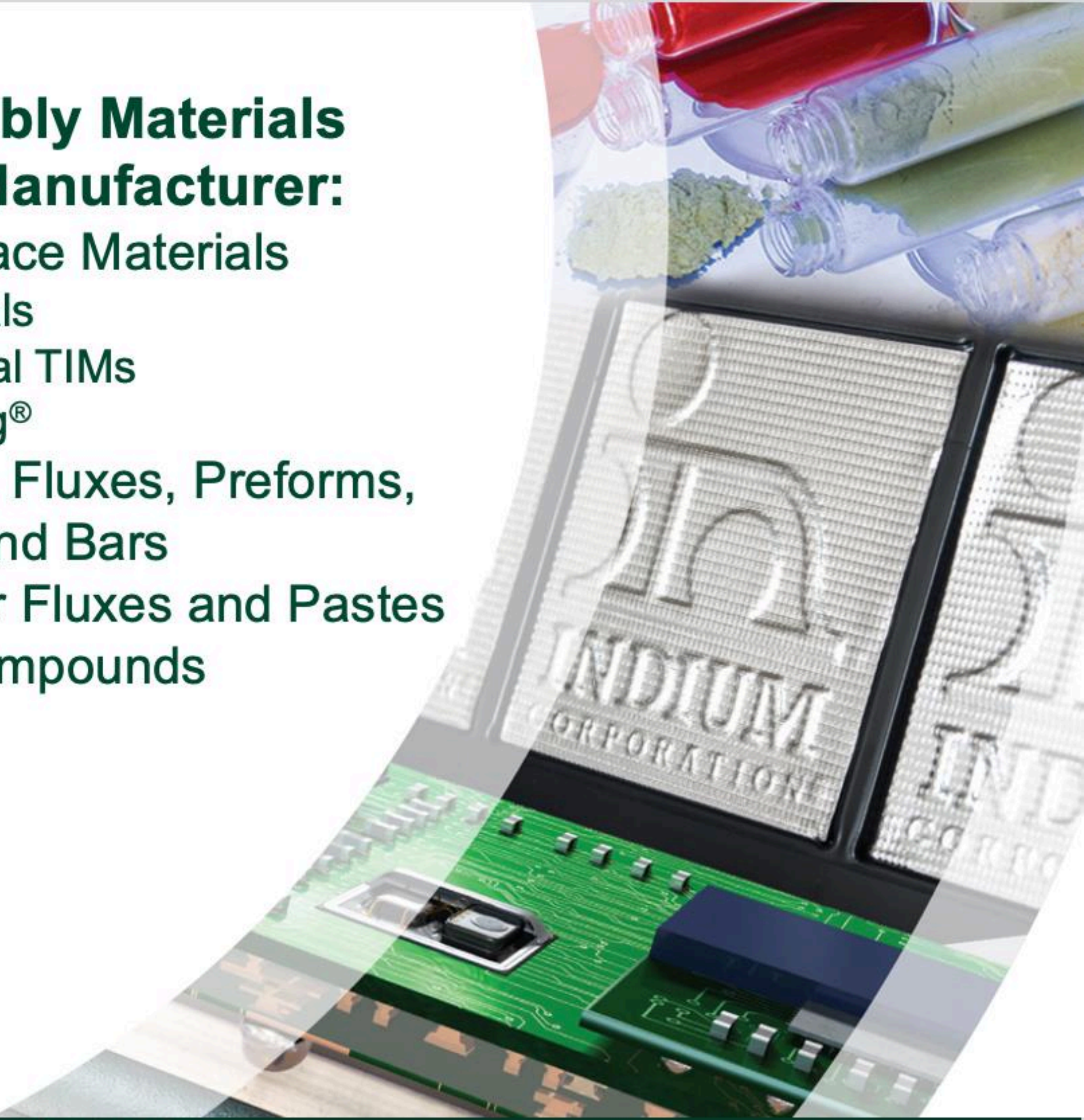
Premier Assembly Materials Designer and Manufacturer:

- Thermal Interface Materials
  - Liquid Metals
  - Hybrid Metal TIMs
  - Heat-Spring®
- Solder Pastes, Fluxes, Preforms, Alloys, Wire, and Bars
- Semiconductor Fluxes and Pastes
- Metals and Compounds



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