Too Hot To Test

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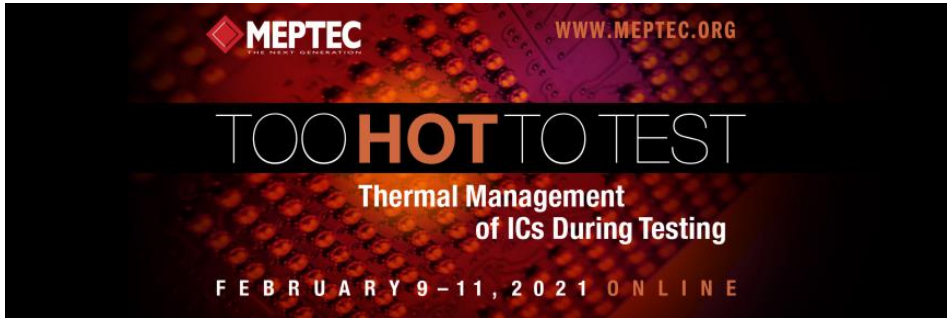


Optimizing Test Based on Device Temperature

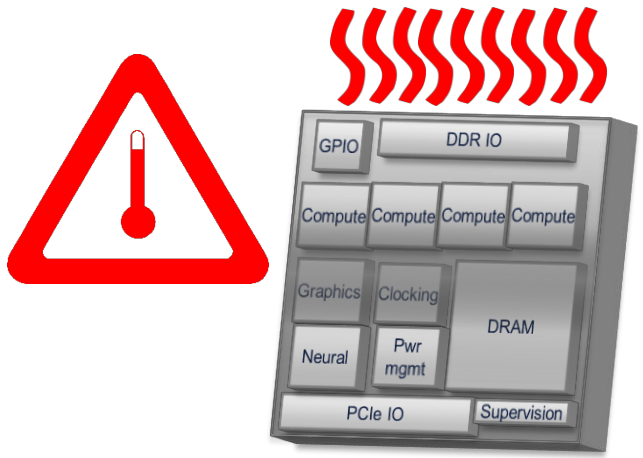
What's the Problem?

- Devices heat up the faster you try to test them, especially during structural test
  - Packaging is usually designed for mission (application) mode, where temperatures are lower
  - Test done at wafer probe has no package to conduct away heat
  - Device behavior changes with variations in temperature

- **This costs money**
  - Minor problem: test time goes up, meaning more equipment time is required to adequately test the device
  - Major problem: Thermal issues may cause device overkill (throwing away good devices)

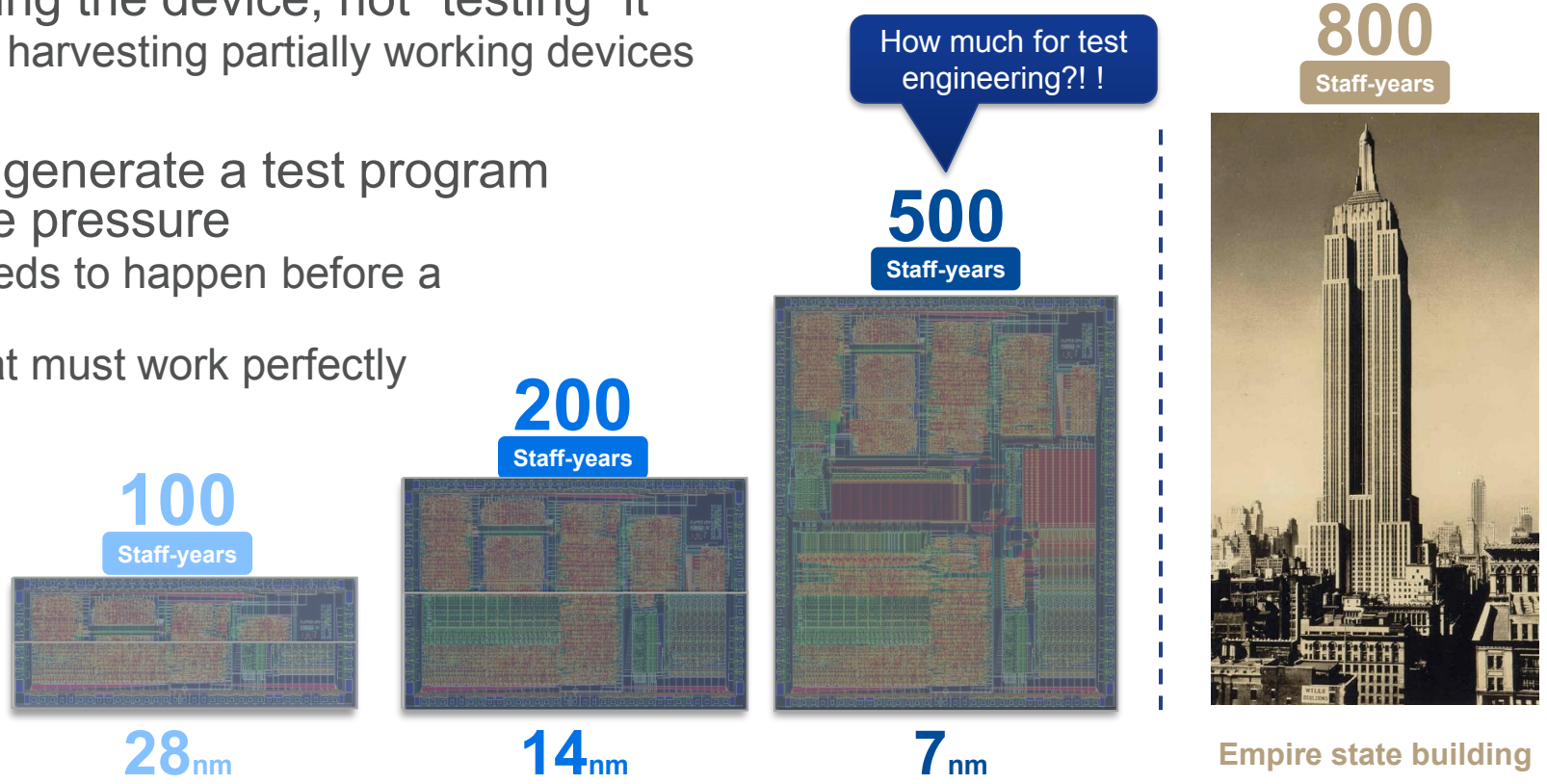
- Today there are only crude solutions to this
  - Monitor case (package) temperatures
  - Slow down testing until it works

- Can you monitor die temperature?
  - Not in ways that are really useful



A few things about “Cost of Test”

- If someone could increase yield by 5% by doubling their test time, they would do it happily
  - Test isn’t that expensive compared to silicon costs
- A lot of time is spent fixing the device, not “testing” it
  - Vdd trim, memory repair, harvesting partially working devices
- It takes a lot of effort to generate a test program and there is a lot of time pressure
  - It is the last thing that needs to happen before a device can be shipped.
  - 100,000 lines of code that must work perfectly



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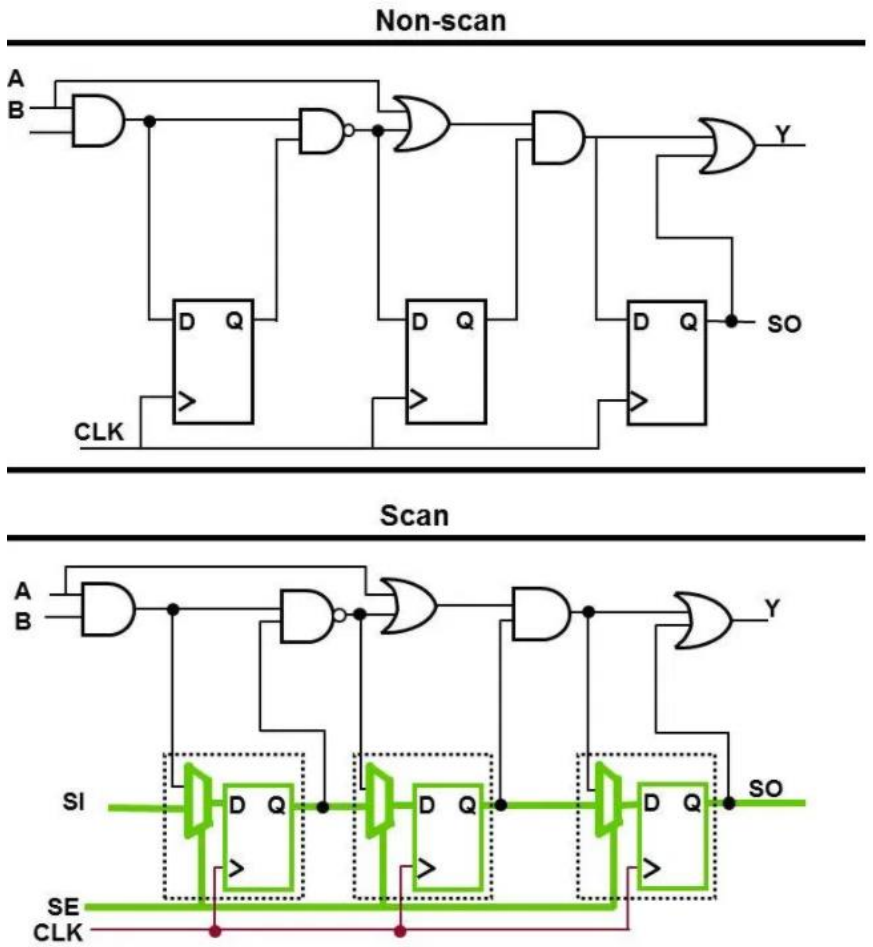
The Problem of Structural Test

- Structural test is designed explicitly to toggle as many transistors as possible to test functionality as quickly as possible
  - Activity is localized with higher activity levels
- Structural test is an “un-natural” mode of operation for the device
  - Consumes far more power
  - Generates far more heat
- Only used during test, so packaging is not optimized for this case

- What can we do today?
  - We can speed up or slow down shift rates
  - We can re-order tests
  - We can add cooling to IC handlers and prober chucks, which is expensive and imprecise



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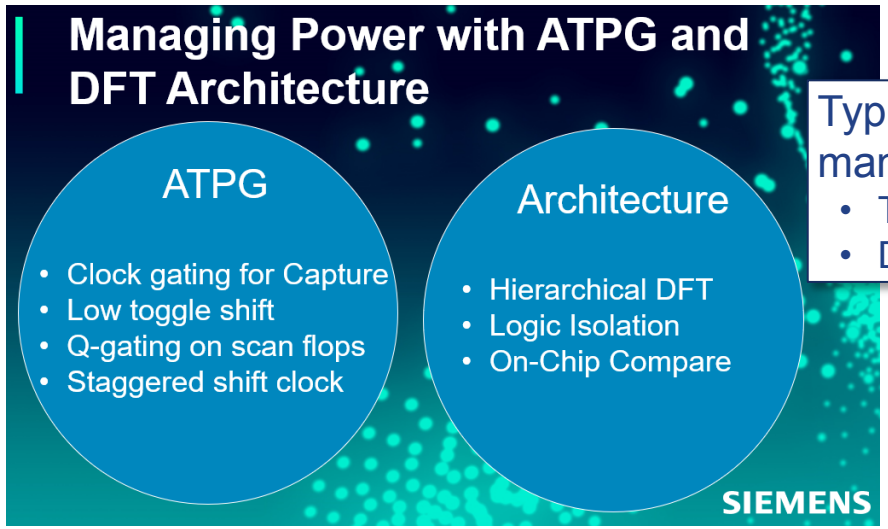
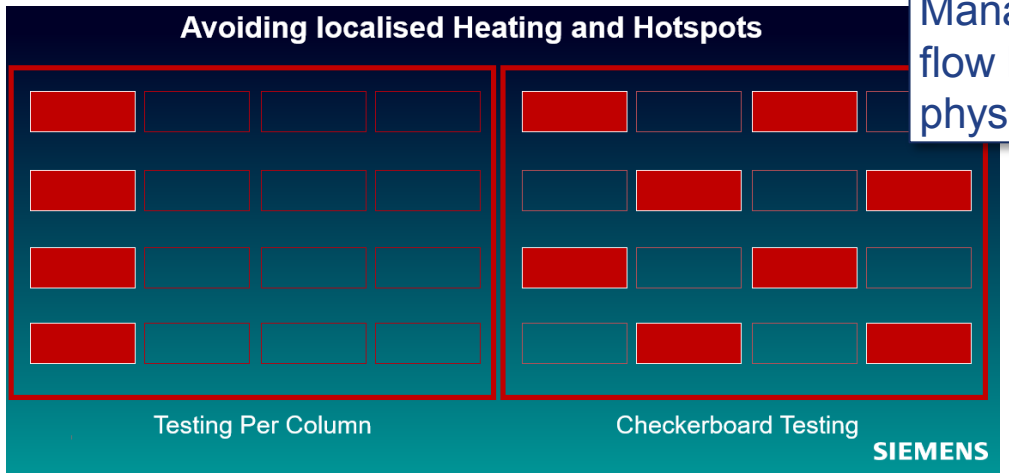
New Scan Structures Reduce Overall Cycle Count

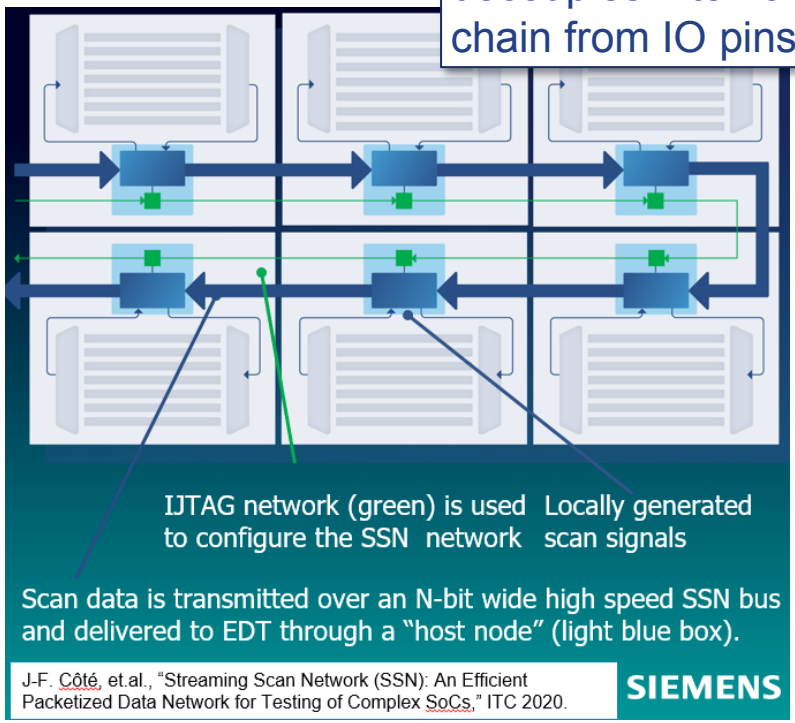


Typical tools for power management
- Test conditions (ATPG)
- Device design



Managing test flow based on physical layout

Scan "network" that reduces overhead and decouples internal scan chain from IO pins



	SSN (32b bus size)				Pin-muxed GPIO (estimated)			
Patterns	Setup cycles (IJTAG)	Scan Test Cycles	Total Test Cycles	Total Data (Mb)	Setup Cycles (IJTAG)	Scan Test Cycles	Total Test Cycles	Total Data (Mb)
10	34,703	3,280	37,983	0.28	20,446	5,740	26,186	0.29
500	34,703	136,120	170,823	4.53	20,446	241,900	262,346	7.74
10000	34,703	2,711,740	2,746,443	86.95	20,446	4,820,780	4,841,226	154.26
STF vs. SSN @ 10K patterns					*Pinmux vs. SSN*		*1.76*	*1.77*

40% Reduction in overall test cycles to do the same amount of testing

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Optimizing Test based on Device Temperature

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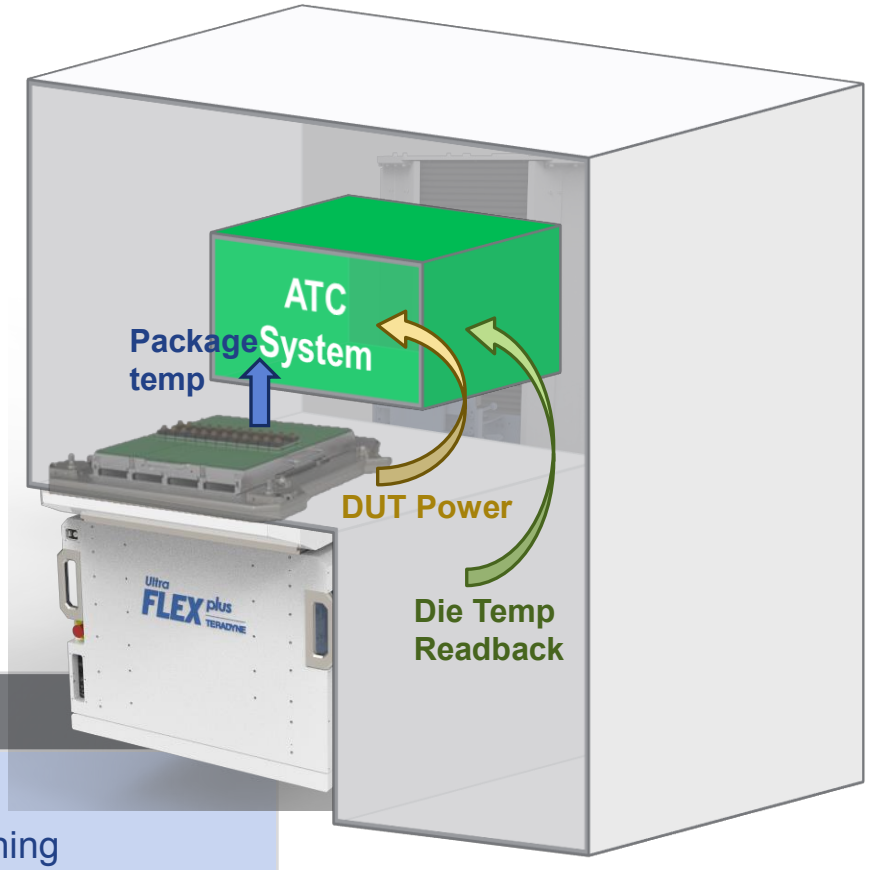
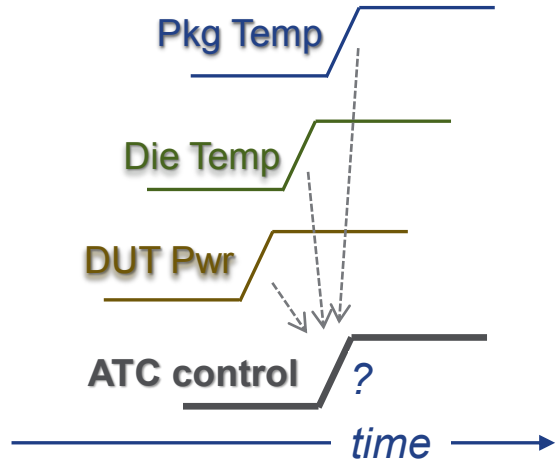
Automatic Temperature Control (ATC) Systems

- Handler and probers can provide cooling based on feedback from the DUT or Tester, but no method is really perfect



Method	Pros	Cons
Monitor package temperature	• Easy to do (self contained in handler or prober)	• Lagging (late) indicator • Can only measure one thing
Die Temperature Readback	• Exactly what you care about • Can measure multiple physical locations	• Latency is too long to use in real time • No uniformity in implementation
Monitor Device Power Supplies	• "Early indicator" of DUT temperature • Can get core-specific information • "Smart Control" of ATC	• Device is probably hot before ATC is effective
All of these	• Adaptive	• Not predictive



How to Make This Better?

If you want these…

You need to solve these…

Method	Pros	Cons
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Better Monitoring Technology Being Developed

Universal Chip Telemetry™ (UCT) by proteanTecs

- Wide range of parametric measurements
- High coverage & high resolution
- On-chip controller for data buffering & data reduction
- Negligible design penalty

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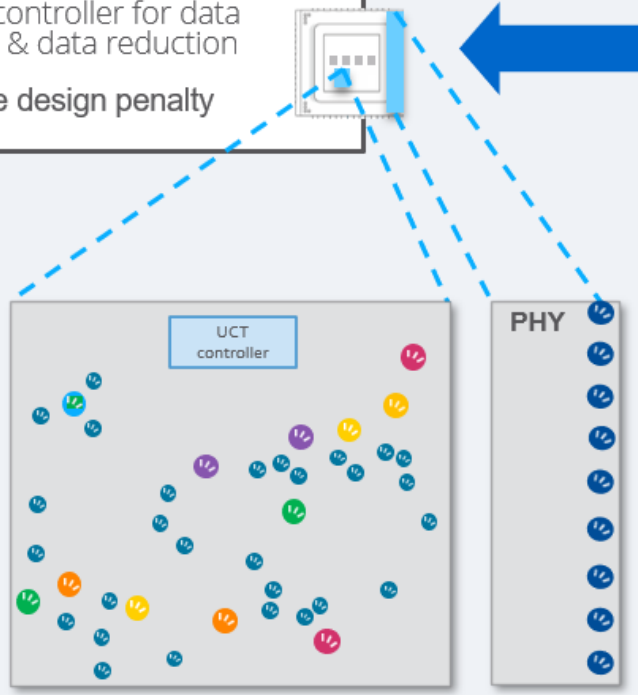


- Standard bus interfaces (JTAG, I2C, etc.)
- Operate during structural and functional test
- Operate in mission-mode as well (no special test-mode is required)

2

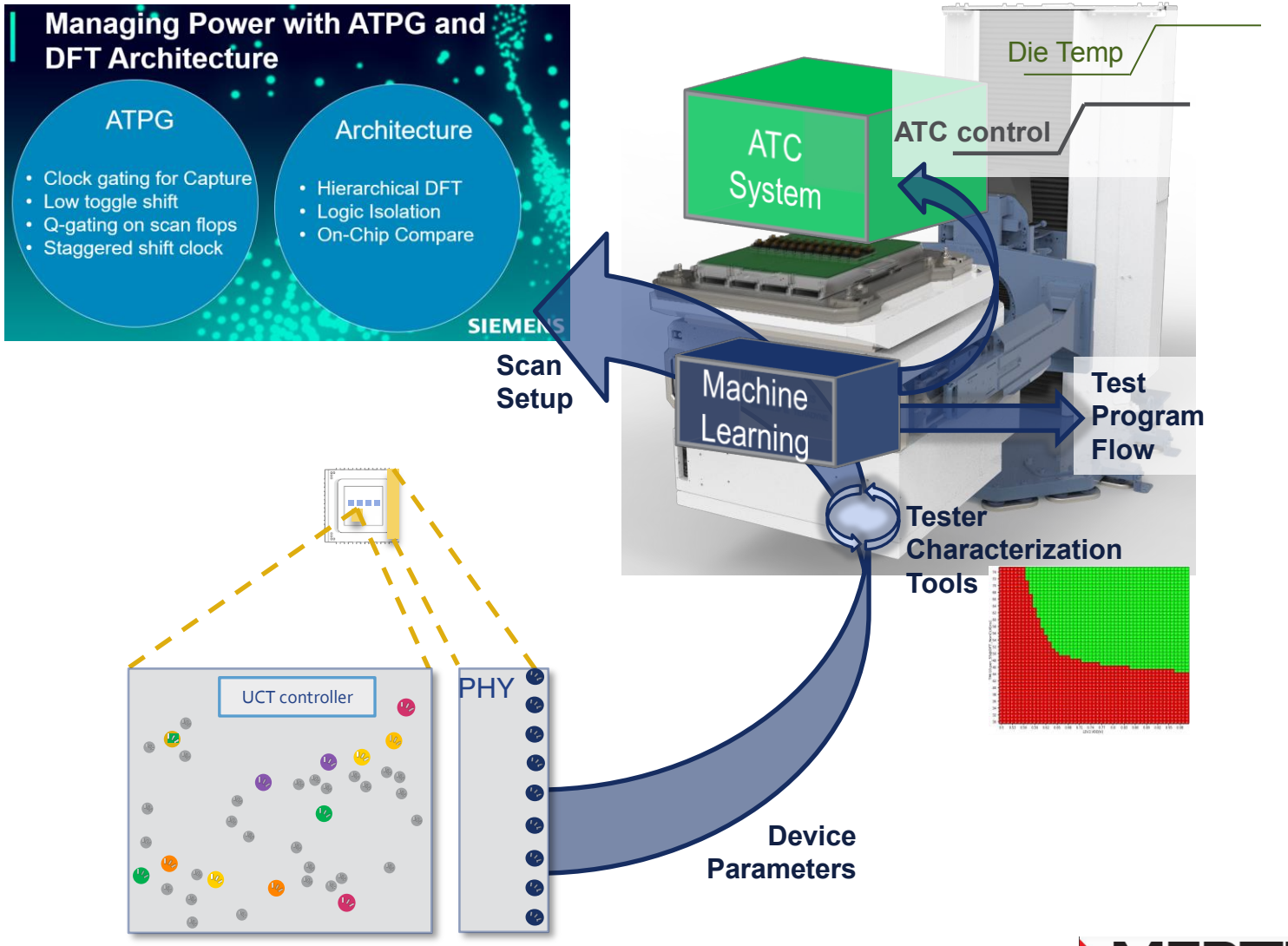
- Cloud-based analytics and visualization platform
- Machine learning and big-data analytics
- Automated actions and insights
- Edge computing on ATE for real-time execution

3

- ✓ Easy
- ✓ Exactly What you care about

Bringing It All together – What Can the Tester Do?

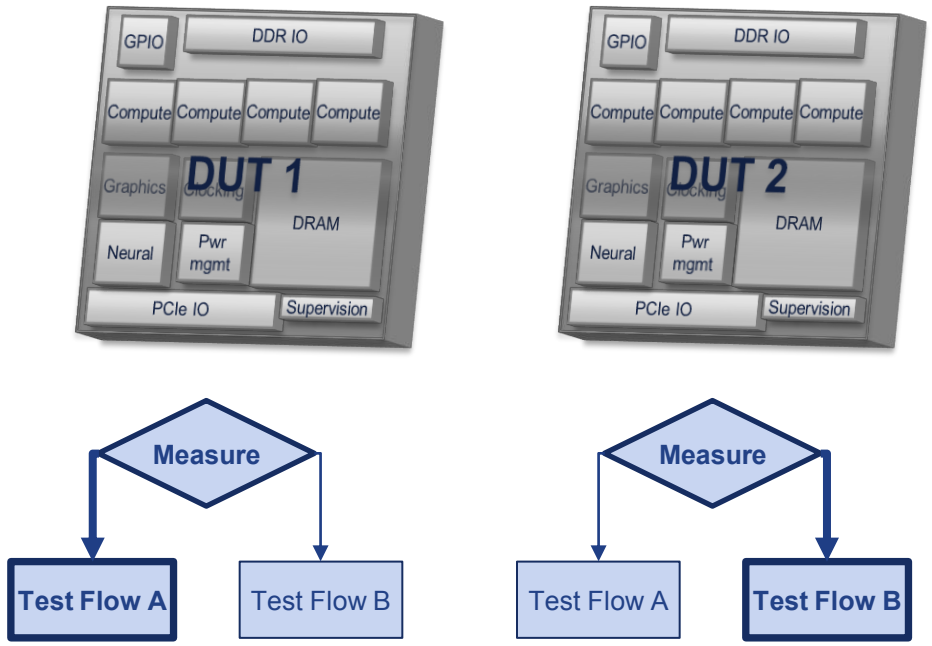
- Rapidly collect DUT response to
  - Pattern Content, speed and sequencing
  - Test Flow
  - Power supply
- Export Data for offline analysis
  - Test management between insertions
  - Optimize scan network settings
- Host real-time machine learning
  - Optimize test flow and conditions
- Use collected data to improve ATC response time
  - Make sure ATC system is activated before DUT temperature rises



Optimizing Test based on Device Temperature

What Are the Technical Challenges?

- Device test flows can change on the fly for other reasons
  - Device harvesting and down-grading
  - Retests
  - Trim and repair
- Will require more information from design
  - more meta-data
- Multisite testing compounds the issue
  - ATC must be site-aware
- All this combines to make predictive modeling more difficult



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So, Back to Cost….

- What may limit gains?
  - Test flows get too dynamic and there are too many permutations to deal with
  - Scan becomes a smaller portion of overall test time so throughput gains are limited
  - All the extra work increases time to market, which can have a larger business impact than either test time or yield
  - More data to deal with…

- **What are the opportunities?**
  - Faster test times
  - Better yields because die temperatures are better controlled
  - Optimization of test flows
  - Methodology can be extended for other parameters like Vdd and reference voltages

Questions?

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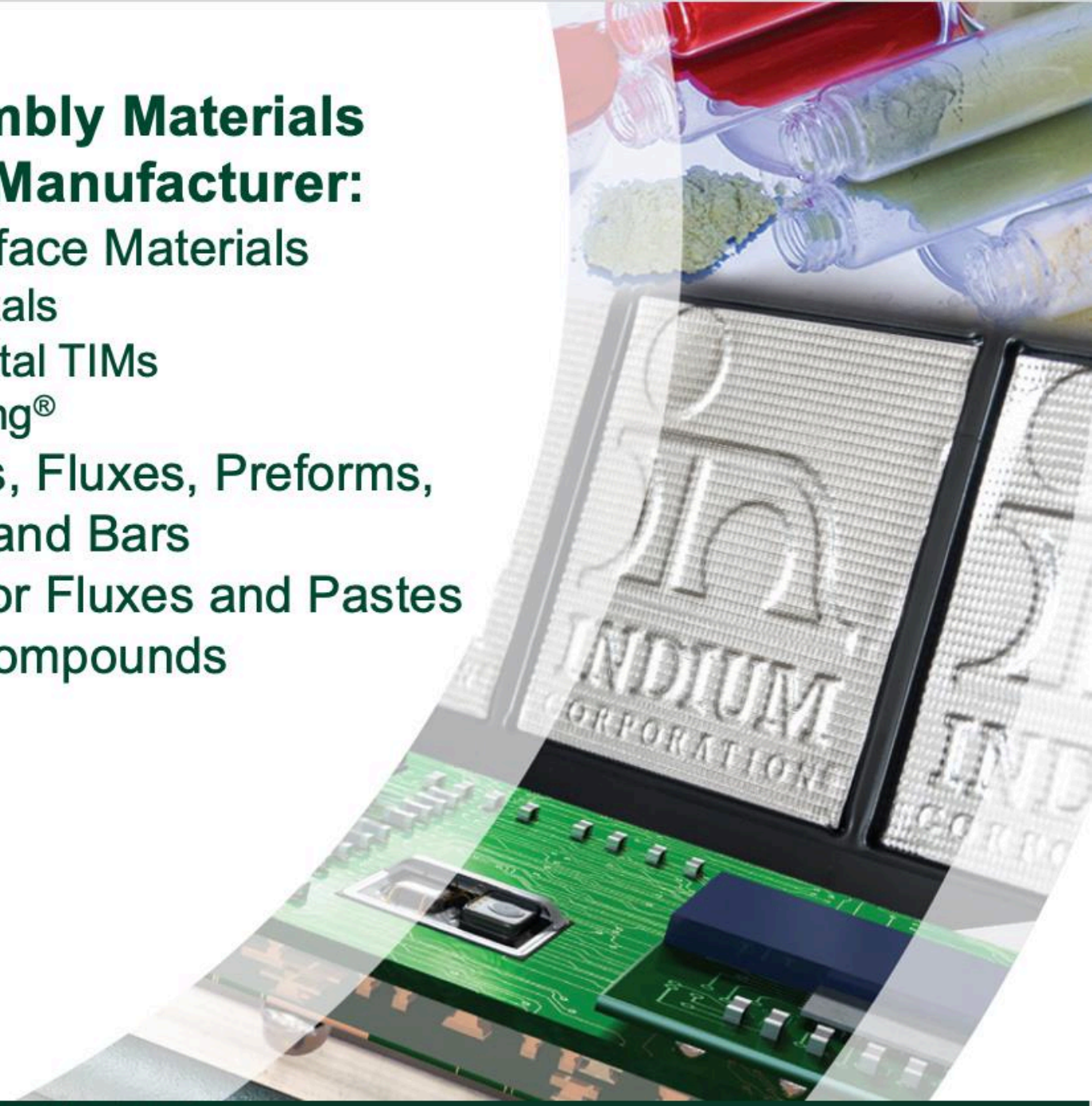

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