Too Hot To Test

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Thermal challenges during test of High-Performance CPUs for client and server segments

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Agenda

- Introduction to general problem Product Dev Engineers face
- Tester thermal challenges vis-à-vis System
- Hotspots and power density trends
- Tests: Scan, Array, Functional
- Look deep into the guts of the tests
- Mitigations: Not solutions
- Future : What is needed to solve this problem.

When you are chasing the Top Bin/Speed …

- No one is happy about this shmoo ☹

```
5GHz shmoo at 100C
-----------------------------------------
1.5500V              |      AABBBBBBBBBBBB
1.5000V              |      AAABBBBCDDDDDD
1.4500V              +      AAAABBBCDEDFDF
1.4000V             >|      AAABBBBCGDHHFF
1.3500V              |      AAAABBBBCDBHBB
1.3000V              |      AAAAABBBBCDB*H
1.2500V              |      AAAAAABBBBCC**
1.2000V              +      AAAAAAAIBBBCJ*
1.1500V              |      AAAAAAAAABBBBC
1.1000V              |      AAAAAAAAAABBB
1.0500V              |      AAAAAAAAAAAAB
1.0000V              |      AAAAAAAAAAAAA
950.00mV             +      AAAAAAAAAAAAA
900.00mV             |      AAAAAAAAAAAAA
850.00mV             |      AAAAAAAAAAAAA
800.00mV             |      AAAAAAAAAAAAA
750.00mV             |      AAAAAAAAAAAAA
700.00mV             +      AAAAAAAAAAAAA
                     +      ------^-------+
                     9nS          10nS  11nS
```

…. and some engineer comes and shows this

```
5GHz shmoo at 100C
-------------------------------------
1.5500V              |      AABBBBBBBBBBBB
1.5000V              |      AAABBBBCDDDDDD
1.4500V              +      AAAABBBCDEDFDF
1.4000V             >|      AAABBBBCGDHHFF
1.3500V              |      AAAABBBBCDBHBB
1.3000V              |      AAAAABBBBCDB*H
1.2500V              |      AAAAAABBBBCC**
1.2000V              +      AAAAAAAIBBBCJ*
1.1500V              |      AAAAAAAAABBBBC
1.1000V              |      AAAAAAAAAABBB
1.0500V              |      AAAAAAAAAAAAB
1.0000V              |      AAAAAAAAAAAAA
950.00mV             +      AAAAAAAAAAAAA
900.00mV             |      AAAAAAAAAAAAA
850.00mV             |      AAAAAAAAAAAAA
800.00mV             |      AAAAAAAAAAAAA
750.00mV             |      AAAAAAAAAAAAA
700.00mV             +      AAAAAAAAAAAAA
                     +      ------^-------+
                    9nS          10nS   11nS
```

@ 17C lower

```
-------------------------------------
1.5500V              |      **************
1.5000V              |      A*************
1.4500V              +      A*************
1.4000V             >|      A*************
1.3500V              |      AB************
1.3000V              |      BA************
1.2500V              |      CBA***********
1.2000V              +      CCCBA*********
1.1500V              |      DCCCBA********
1.1000V              |      DDDCCCBA******
1.0500V              |      DDDDDCCCBE****
1.0000V              |      DDDDDDDCCCBAAE
950.00mV             +      DDDDDDDDDDDCCB
900.00mV             |      DDDDDDDDDDDDD
850.00mV             |      DDDDDDDDDDDDD
800.00mV             |      DDDDDDDDDDDDD
750.00mV             |      DDDDDDDDDDDDD
700.00mV             +      DDDDDDDDDDDDD
                     +      ------^-------+
                    9nS          10nS   11nS
```

…the start of the nightmare for the “thermal guy”

All hell breaks loose….

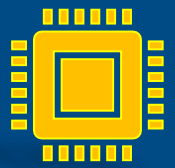
- Arch: . . . it is architected to run at the top speed; even higher!!! . . .
- Design: . . . we PVT-ed it correctly!!! Why is HVM having problem? .
- Validation: . . . It is (*often one unit*) running okay on the system , Right?
- DFx: . . . Test vectors are correct, passing simulation and emulation; heck even passing on the tester. Run it at the top speed please . .
- Fab/Assembly: . . . Pretty silicon, nice package too. Don't burn it up please . . .
- Q&R: . . . No relaxation in any specs, TDP, Tj etc. No . No.. No…
- Planning: . . . We need minimum15% top speed Binsplit and by next week please … and don't increase test time and crater my factory capacity. Thanks.

. . . *and* . .

- Me, the Product Development Engineer : . . . but, but, but . . .

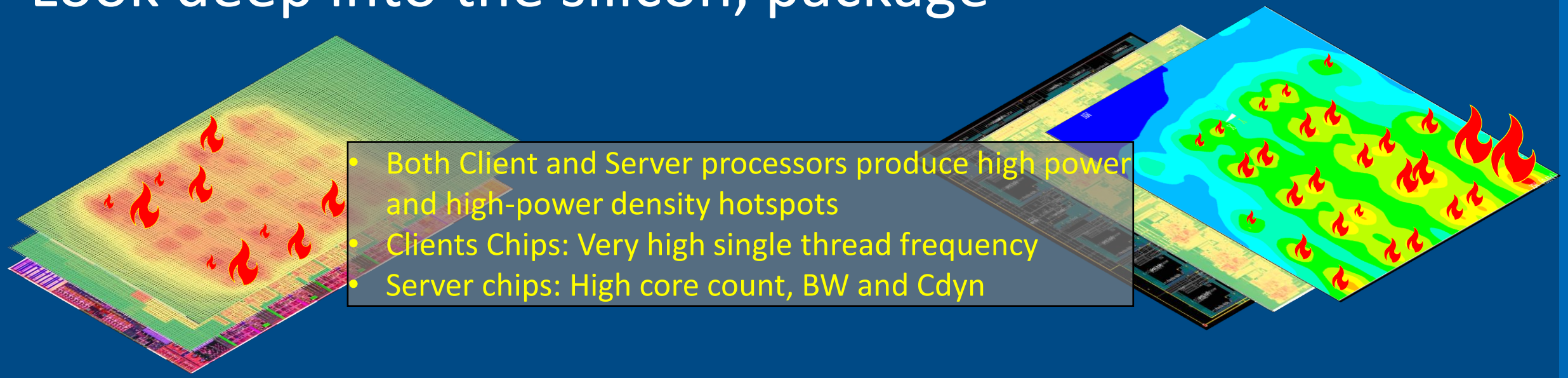
. . . It is too Hot to test !!!!

Tester vs System



Tester	System
Almost all tests are in DFx Mode and bypass the on-die Power/Thermal control loops.	On-die Power, Thermal management: Throttling kicks-in → Power ↓, Tj-rise ↓
Test patterns are short and repetitive. Short bursts→ sharp transients → Tj-rise ↑↑	System tests are long enough for Power and thermal controls / feedback loops to kick-in
Cores, for test efficiency, are mostly lock-step /clock synchronous leading to power spikes as well as droop	Cores and Threads are mostly asynchronous; power peaks do not line up
Maximize # of Cores / IP that can be run together → Test Time ↓ → higher power ↑ → Tj-rise↑	# of cores / IP running at the same time at max freq is restricted by SKU config / architecture definition.
Test power can be 2x-10x than the spec power. Often tested above / outside of spec envelop. > Tj-throttle	System tests seldom consume more power than specification; within thermal envelope. < Tj-throttle
Temporary thermal interface: Dry, Liquid TIM, poor / inconsistent thermal conductivity, Not always the best flatness, warpage make heat transfer worse. Tj-rise↑	Robust thermal interfaces: Compliant or semi-permanent TIM, almost flat surfaces, no warpage etc.

Look deep into the silicon, package

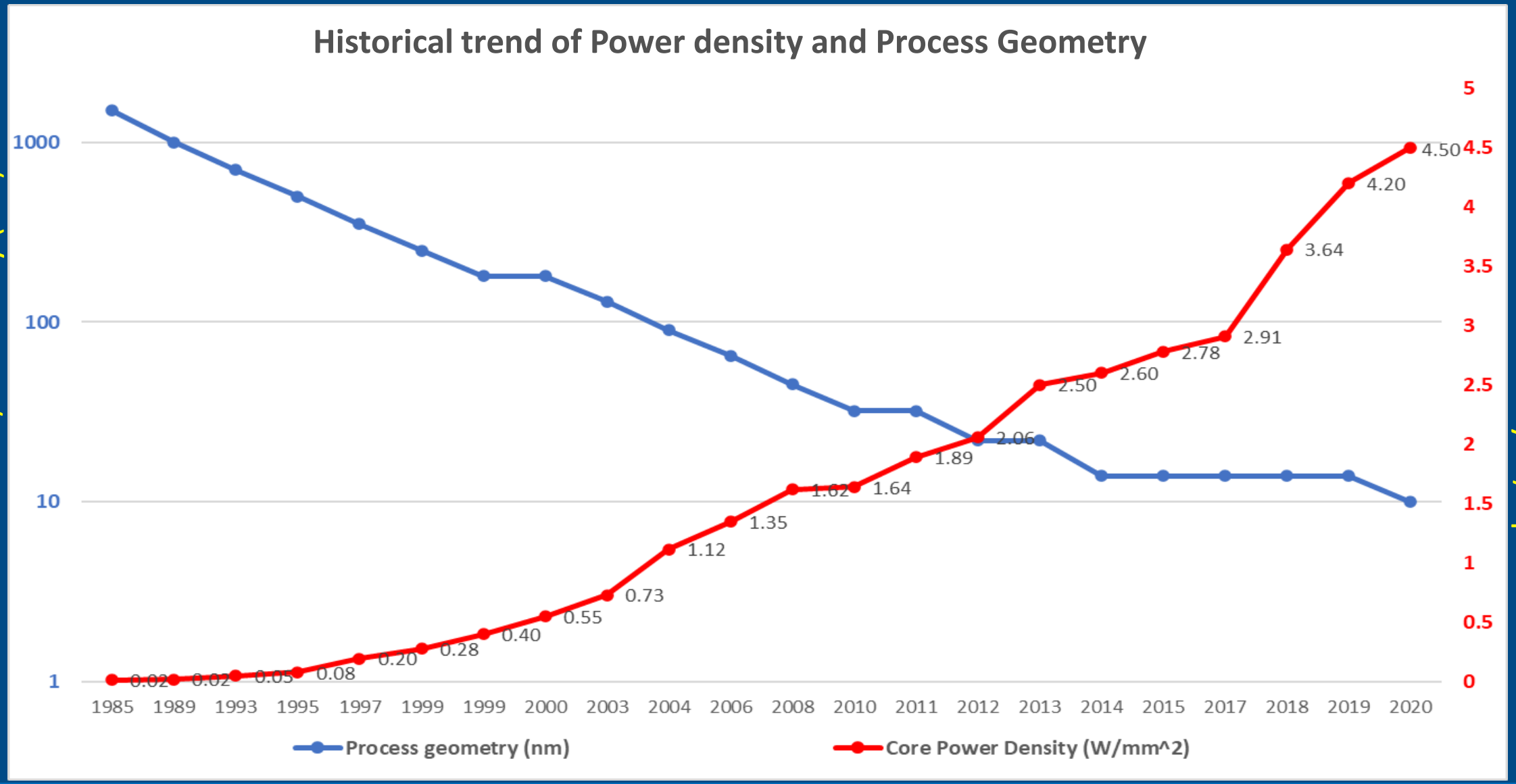


- Both Client and Server processors produce high power and high-power density hotspots
- Clients Chips: Very high single thread frequency
- Server chips: High core count, BW and Cdyn

- Many hotspots, and they move around per WL , application or test type
- Edge , corner effects, crowding of hotspots → Tj-rise ↑
- TIM1, TIM2 , packaging aspects induced impacts influence Tj-rise
- Thermal mass diff between Bare die, Lidded part introduce unique challenges
  - Bare die: low thermal mass →Fast Tj-rise. Too fast for handlers to respond
  - Lidded part: high thermal mass→ sluggish cooling, unable to keep up with test flow
- Chip layout / floor plan, IP design greatly influences power distribution

Power Densities of WLs / tests along with total power are the key

Power density is the villain! Look at the trend



Coming back to test….

- Types of tests we are worried about ….
  - Array testing: MBIST, Repair, Redundancy, kitchen sink
  - Scan testing: Stuck @ and @Speed
  - Functional: Cache Load / SBFT, System ported tests
  - IO tests
  - Analog calibrations

Tj-rise sensitive
Speed binning tests
dFmax/dT, dVmin/dT, dF/dV

Static temp sensitive tests
Mostly defect modes, leakage

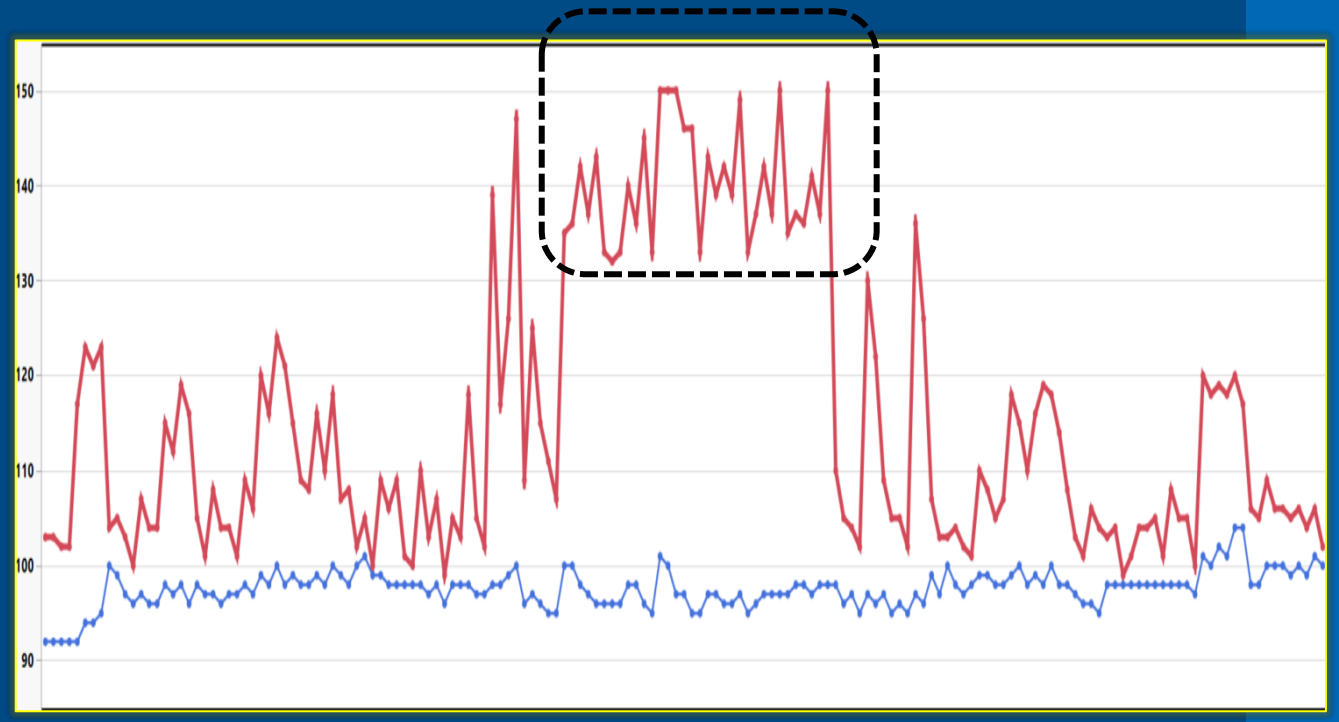
- Test operations:
  - Sort
  - Burn-In/Stress
  - Final test (class)
  - System Level Test (SLT/PPV)

Which tests and how they exasperate the condition:

Scan

- Scan: (S@ and @S)
  - Shift In:
    - Speed is low only few 100s of MHz, but many chains : High Cdyn → Moderate density / High Total power
  - Capture:
    - Short period, couple of cycle at several GHz of speed → severe droop, High power density /High power
    - Activity factor aka number of simultaneous captures → Tunable (complex) High power density.
  - Shift out: Low speed: Not speed critical.
  - Test time vs. Tj rise is a constant battle

Scan content: Huge switching capacitance /power → Thermal runaway

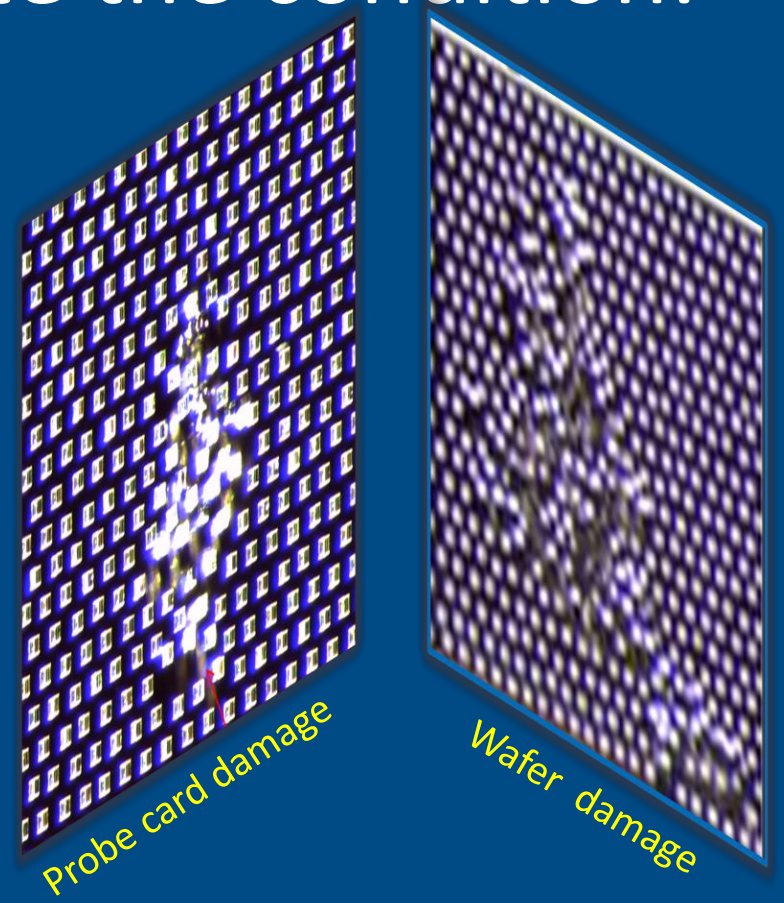


- Tuning scan test switching capacitance is complex.
- Test Cdyn could be as high as 3-10x to a real-world application
- Scan @S (dF,V)/dT) needs correlation with system Fmax, Vmin of the IP

Which tests and how they exasperate the condition:

Array

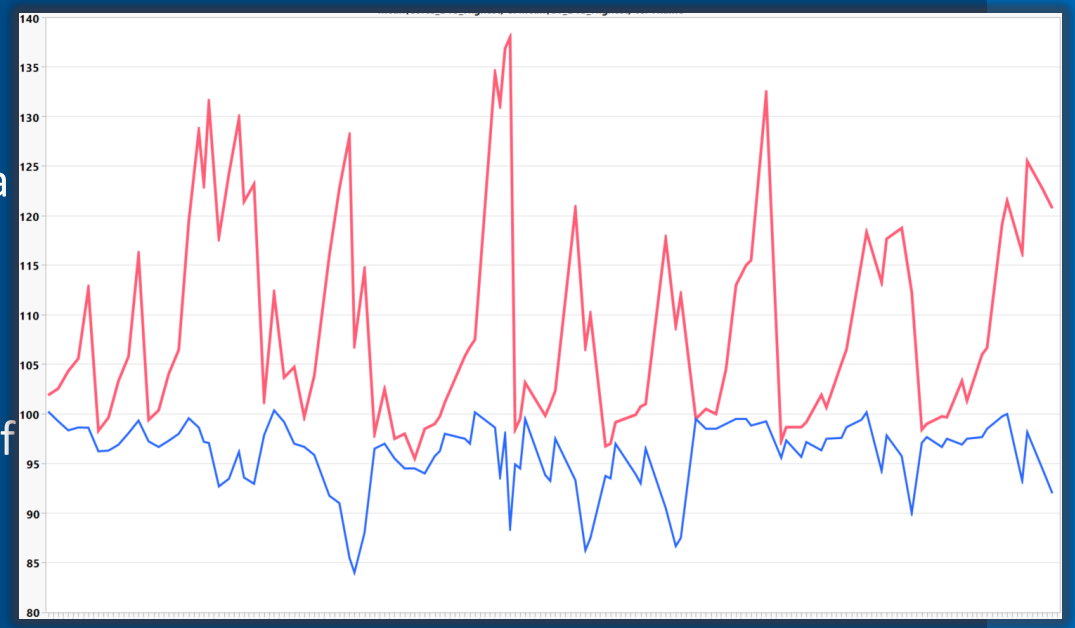
- Array: BIST / Mbist / Kitchen sink
  - "Fire and Forget" Bist Engine is good for test time but very bad for thermal control / monitoring.
  - Fast local Tj-rise Hotspots leading to thermal runaway.
  - Running many Bist engines in parallel in the chip to save test time often results in severely limiting Fmax (Freq wall) or even burnt chips, damaging probe cards
  - Pattern lists are often too long (kitchen sinks) to realize temp has increased.
  - Server chips have HUGE caches, very long tests.
  - Low power modes can be deceiving; may give false fmax/ vmin, DPM risk; correlation needed.



- Very difficult to model pre-silicon the BIST power consumption.
- Test efficiency (TT) vs Fmax (or Vmin) vs quality is a constant battle.

Which tests and how they exasperate the condition: Functional. (Cache load, Mission Mode)

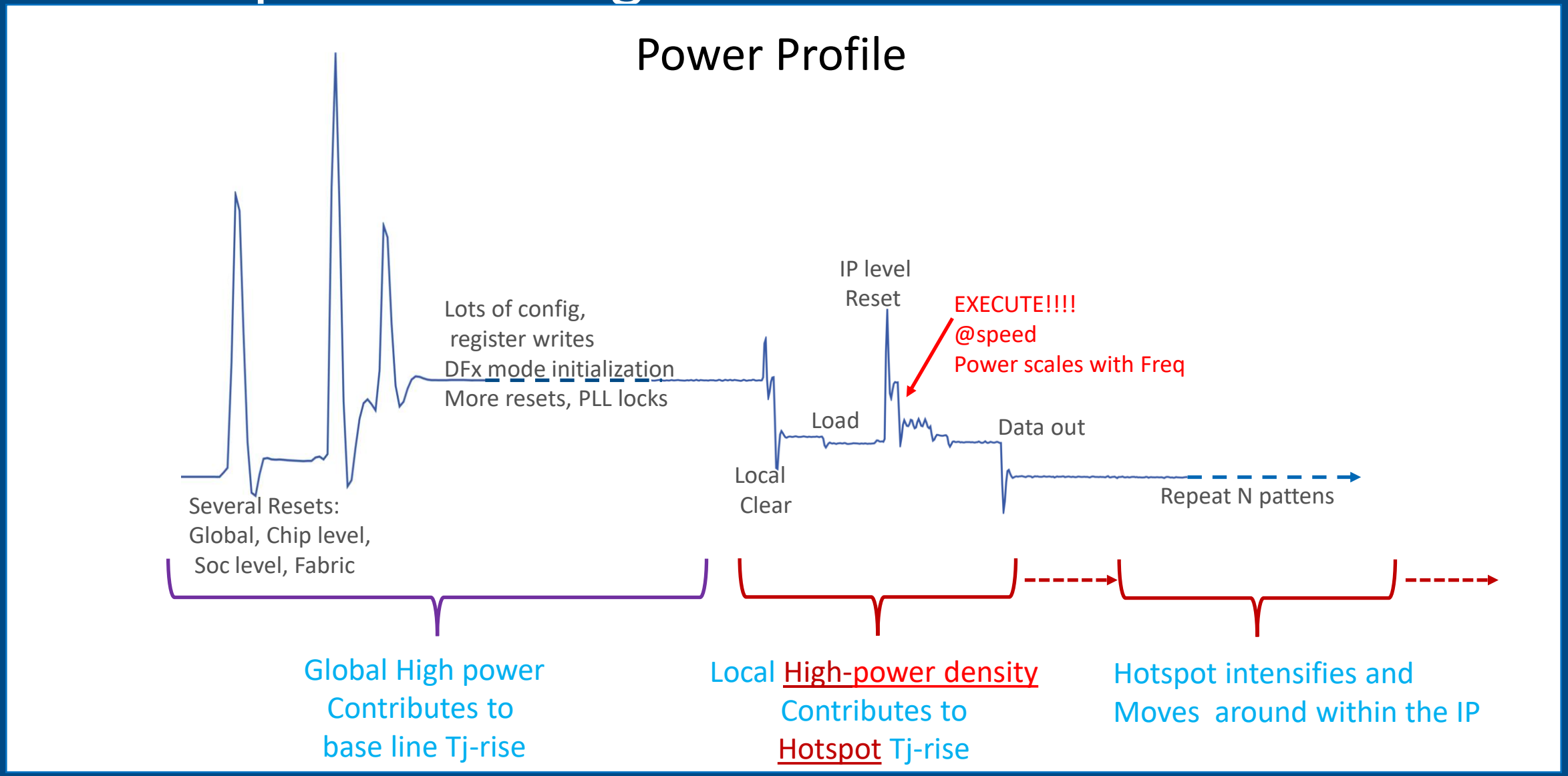
- Cache Load / Structural Based Functional Tests:
  - "Must Have" tests for precise Fmax vs Vmin and coverage / top-off etc.
  - Usually have several functional resets, clocked with normal PLL-locks, Fuse-register configurations to mimic real IP-execution via RTL simulation / test generation.
  - Thousands of patterns each of <0.5-1milli sec but each packs a punch !!!
  - Huge localized power density + high total raw base line power of other clusters
  - Double Whammy!!!
    - Super sensitive to temperature / Tj-rise
    - Super sensitive to local droop.



Unoptimized Functional patterns leading to huge transients

- Highly transient power spikes make it hard to temp control.
- Often all cores are lock step compounding the problem

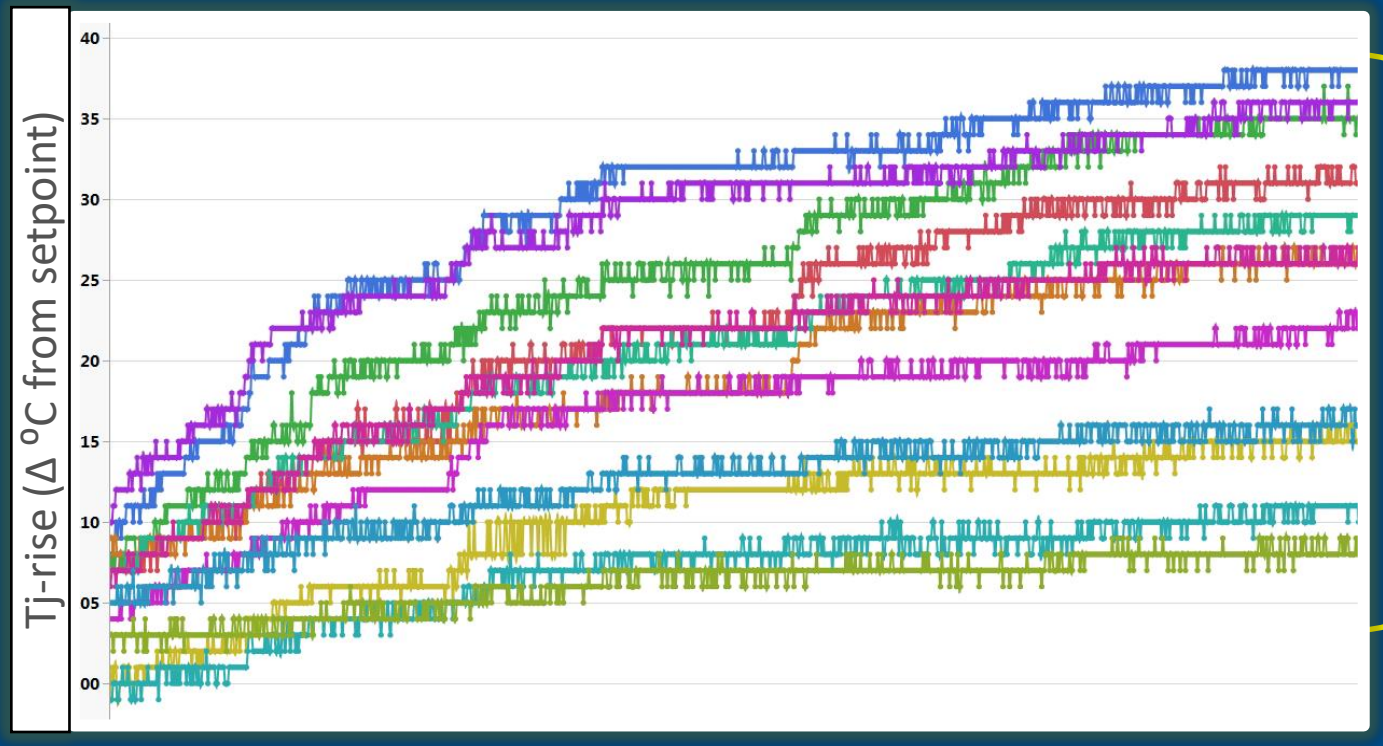
Look deeper into the generic structure of a test

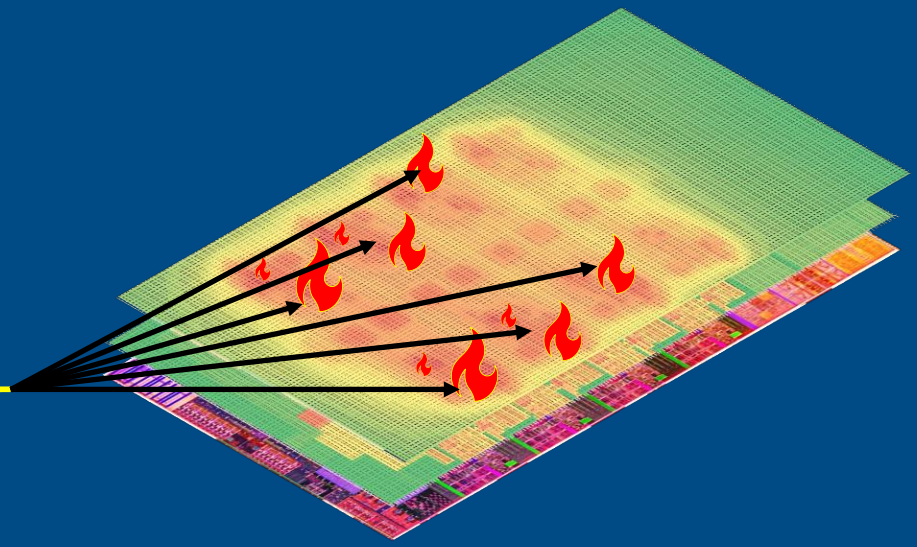


Power density and Hotspot Tj-rise is worse in Compute intense IPs like AVX2/3 (256 / 512bit operations)

Tj-rise due to transient High power density operation

Unoptimized Tj-control → very high Tj-rise





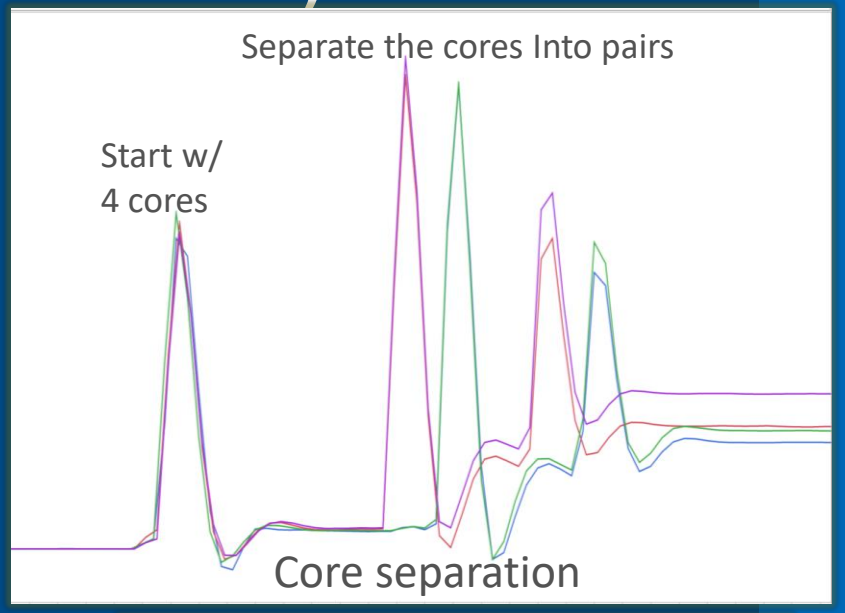
Many hotspots in the chip and they differ in power density and Tj-rise

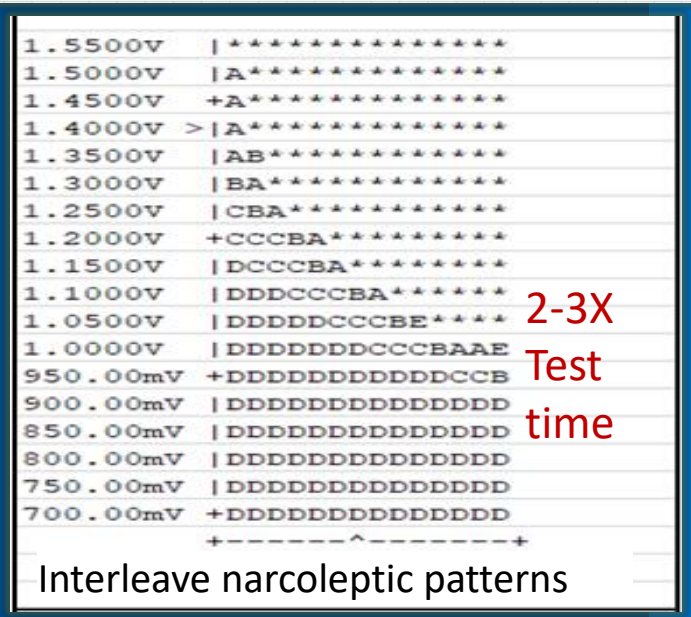
What can we do?

- Thermal control equipment alone will NOT solve the problem
  - Often , the temperature feedback alone is insufficient.
  - Heater, Thermal Diode feedback are very slow and far away from hotspots
  - Bare die products, due to lack of thermal mass will heat up too fast
  - Thermal mass of the Lidded parts, though good for smoothening transients, also acts as a ballast against the thermal control equipment response to cool the DUT.
- We need to address the source of the problem: Heat generation, reduce power density

Some mitigations (Not always viable for HVM)

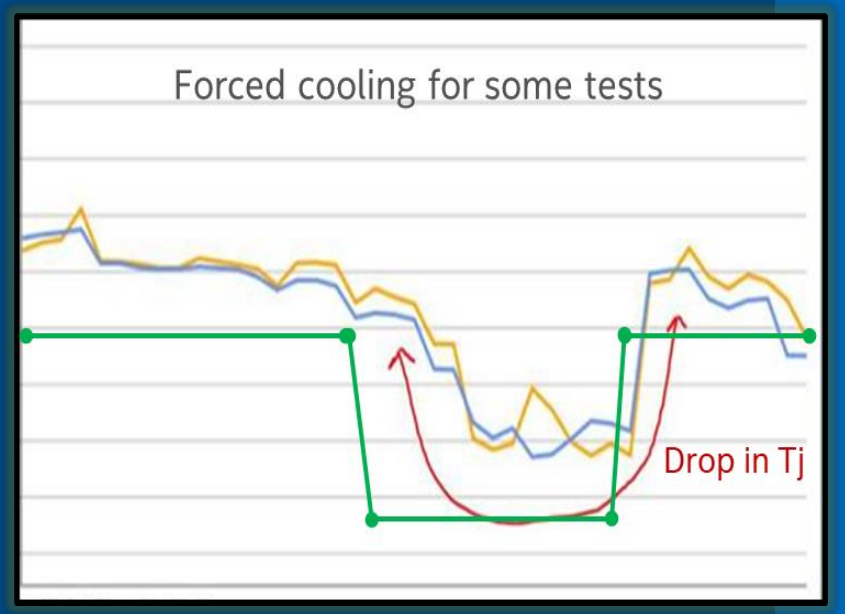
- Core separation / staggering: Spreading the heat temporally and reducing the peak
  - Not intuitive and not seamless to test generation.
  - Complex to build a Test program flow and confusing execution.
  - Fmax/Vmin, binning concerns due pairing / combinations
  - Not all type of content in the same bin / flow requires this.
  - Server chips have large area too many cores, many combinations.
  - Sometimes gives better Fmax/Vmin than real : a DPM problem
  - Not economical for Test time.
- Interleave Narcoleptic / cooling patterns:
  - Not easy to characterize length vs cooling.
  - Not all patterns need cooling / same amount of cooling.
  - No consistent results. (clocks are still running to avoid PLL re-locks)
  - Not all bins / flows produce same Tj-rise hence do not need same amount of cooling
  - Often end up with conservative length. (1 or 2 narco patterns to fit-all)
  - Confuses pattern re-ordering and test time reduction efforts.
  - Manual effort, lots of hand-holding required.
  - Blows test time budgets by 1.5X-4X, not economical.



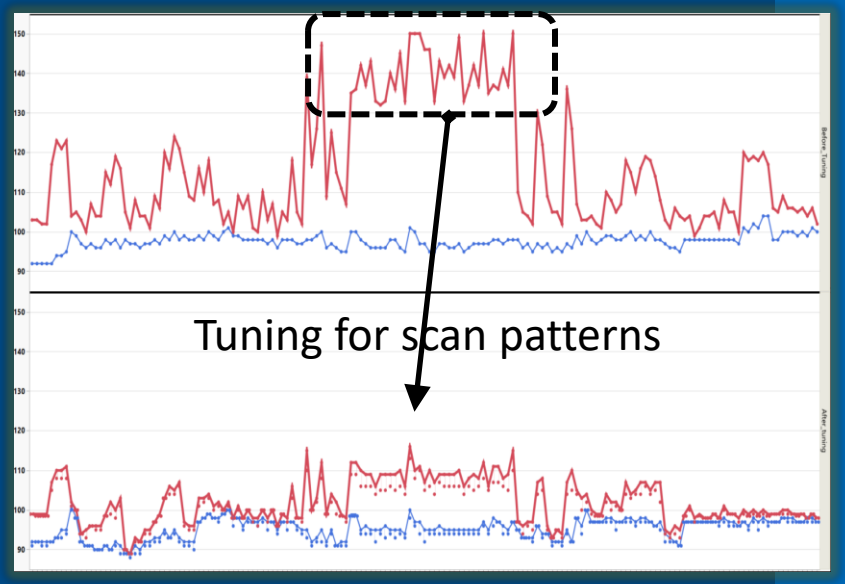


Some mitigations (continued)

- Forced cooling / stepping:
  - Stopping the test flow and temporarily increase cooling / force cooling by adjusting the handler for select tests. Only.
  - Usually needs a full powering down of the DUT before and after.
  - Very disruptive to speed binning flows.
  - May have to do these few times in the test flow for multiple content.
  - Predicting where in the flow to do this and revert after is not easy.
  - Very tricky for the thermal control feedback loops.
  - May be even bad for thermal control equipment's MTBF.
  - Not a HVM viable option.



- Tuning for scan patterns:
  - Provision (DFx) for tuning must be present in design.
  - Chopping chains as an alternative is counter productive.
  - Confuses coverage, yield signature analysis tools.
  - Thermal Tuning only for scan tests is labor intensive.
  - Needs to be repeated for every test program generation.



Reducing power density at floor plan stage is the best option

Future: What is needed to solve this problem.

- Design Architecture: (Industry wide adoption)
  - Power density / Temperature aware IP design, Layout and floor plan tools. ROI analysis Tools at IP design /SOC integration stage: For e.g. xx sq um of whitespace→ Tj↓, Fmax ↑, Vmin ↓, Power ↓
- DFx / Test:
  - Scan power density modulation :DFx for dynamic, on the fly, in-tester seamless @S power,/Cdyn/AF change.
  - Array Mbist power reduction / simultaneous execution (w/o breaking the bank). Low power Mbist
  - Easier tools for core separation / staggering at test generation state with simulation / emulation.
- Telemetry:
  - DFx / test mode surviving on-die thermal managements.
  - More sensors on the SOC, closer to the hotspots with easy access during test
  - Research Needed: Area efficient / ultra-small DTS /nano-remote sensors. Tools for automatic plumbing of sensors in 3rd party IPs
- Tester / thermal control equipment:
  - Better thermal, power feedbacks, hotspot monitoring, test program and handler handshakes
  - Better TIM, higher thermal capacity, faster response, Intelligent control algorithms.

Q&A

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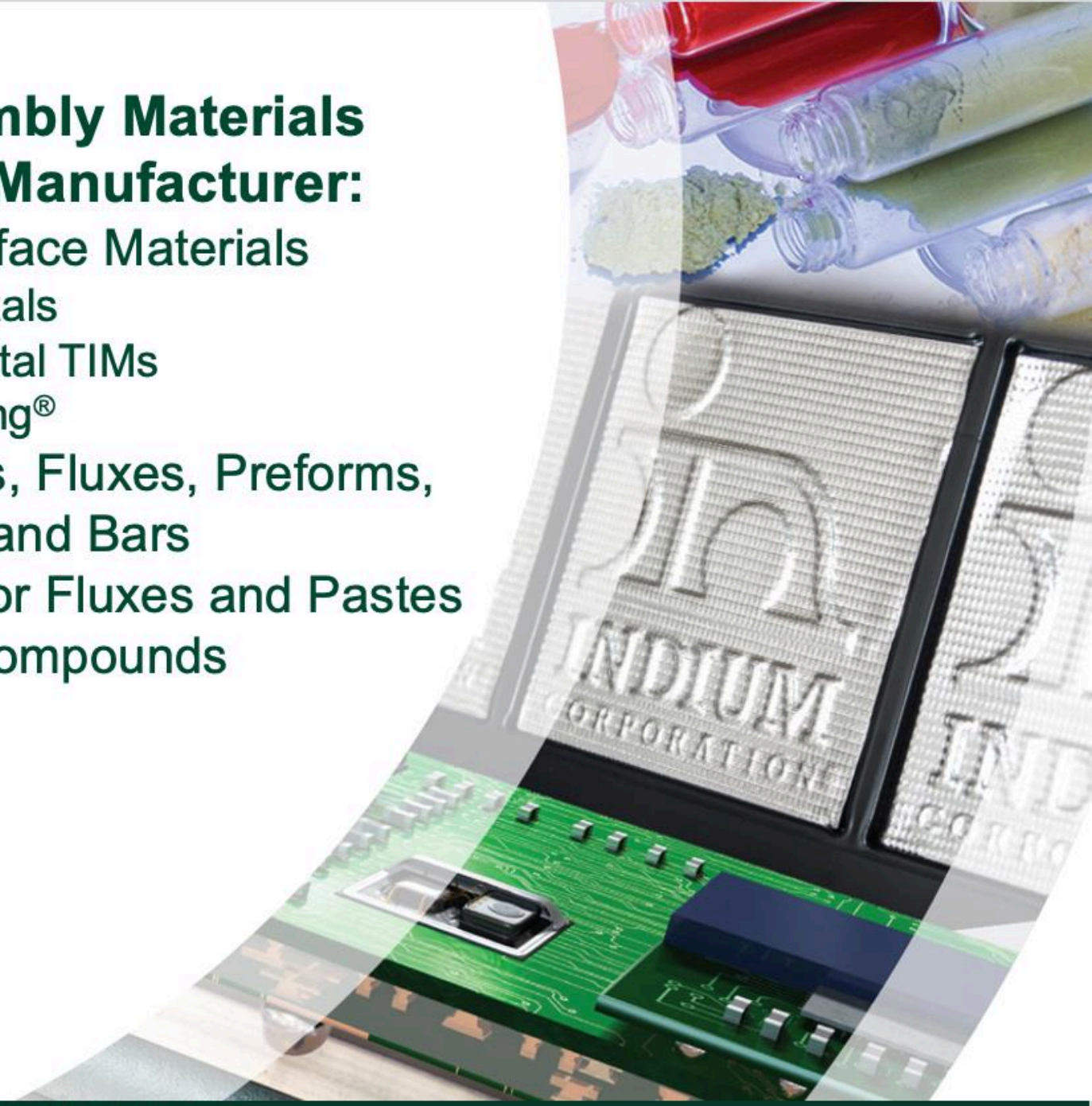

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