



KGx – Known Good x

September 7, 2022

Today's Presenters



Tom Katsioulas
GSA Global



Marc Hutner
ProteanTecs



Jay Rathert
KLA

Technical Program Committee (TPC)



Abram Detofsky
Intel



Neal Edwards
AMD



Zoe Conroy
Cisco



Dave Armstrong
Advantest



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Feldman Engineering

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Quality Screening

Concepts and Advances for using IC
Manufacturing Defect Data to assess Known Good
Die

Jay Rathert

September 2022

The MEPTEC logo, consisting of a red diamond shape followed by the word 'MEPTEC' in white capital letters.

KGX
Known Good x

ONLINE SESSION
September 7, 2022

www.meptec.org

Who is KLA?

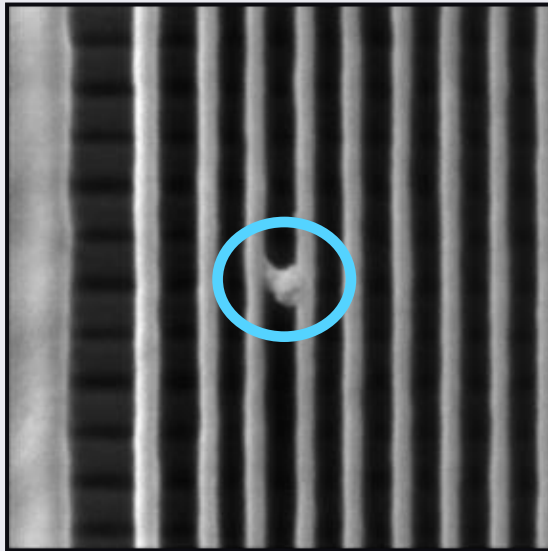
And why are they in a Known Good Die discussion?



KLA in the chip fab

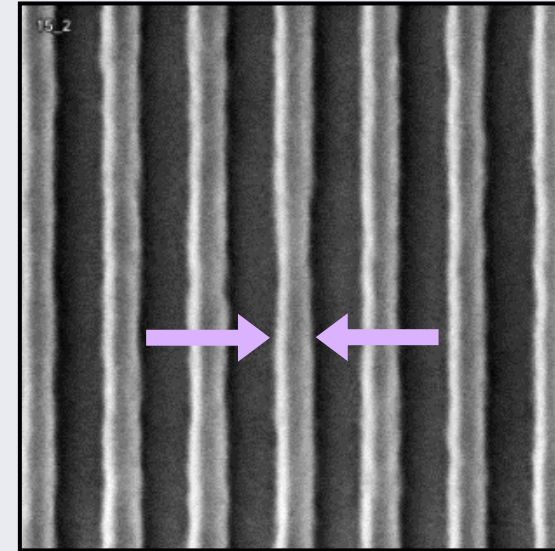
Two Areas to Control

Inspection



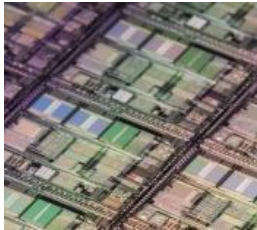
Find Defects

Metrology

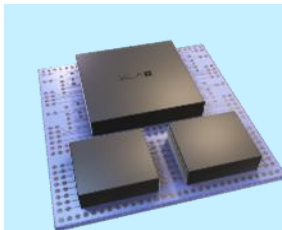


Measure Parameters

KLA at a Glance



Semiconductor
Process Control



Electronic Packaging
& Components (EPC)



KLA Services

1976

A stylized blue icon of a multi-story building with the KLA+ logo on top.

Founded

>60,000

A stylized blue icon representing a bar chart or data visualization.

installed base
(tools)

>14,000

A stylized blue icon showing three people silhouettes with a globe in the background.

Employees

\$8.2B

A stylized blue icon of a line graph with an upward arrow and a dollar sign.

Revenue

\$1.0B / y

A stylized blue icon of a lightbulb with a gear inside, symbolizing innovation and research.

R&D

KLA+ Beyond yield

Our growing role in Quality

Is this die fit for purpose?

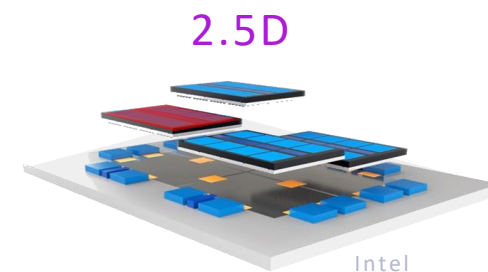
- Automotive
- 5G
- HPC
- Industrial & IOT

Will it be reliable? Is this a known good die?

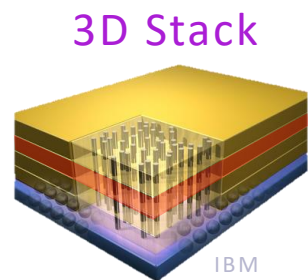
- Increasingly complex packages
- Test uncertainty



Boston Globe

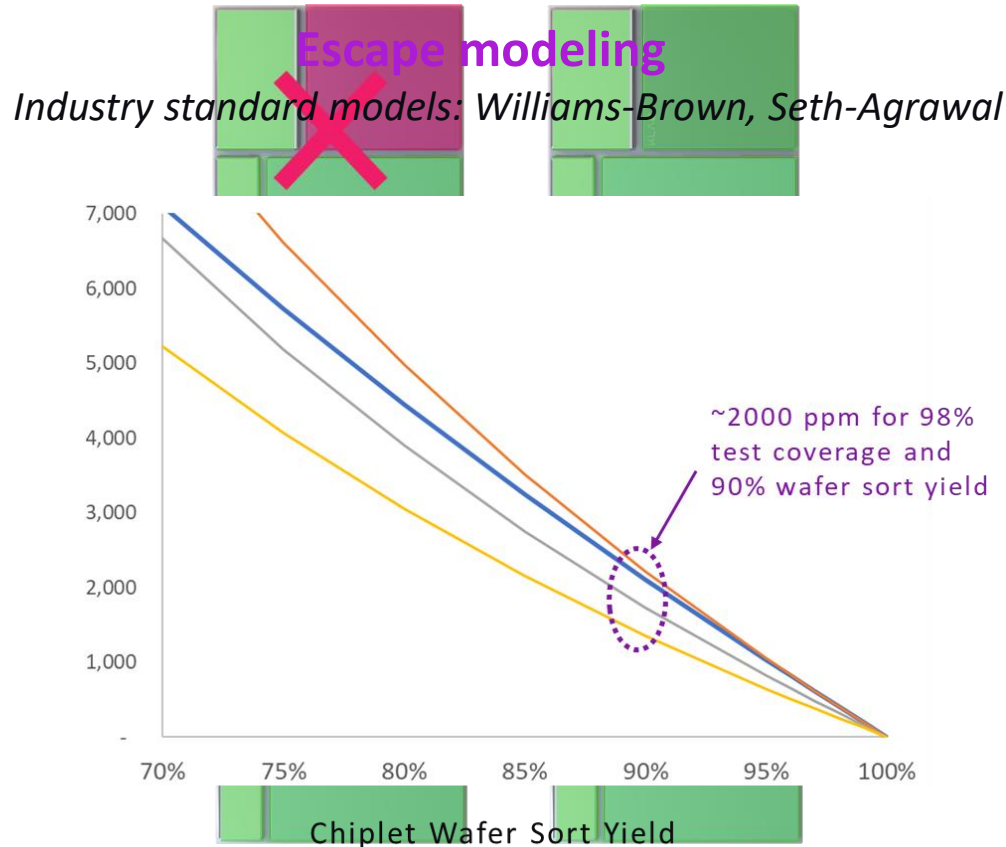


Intel



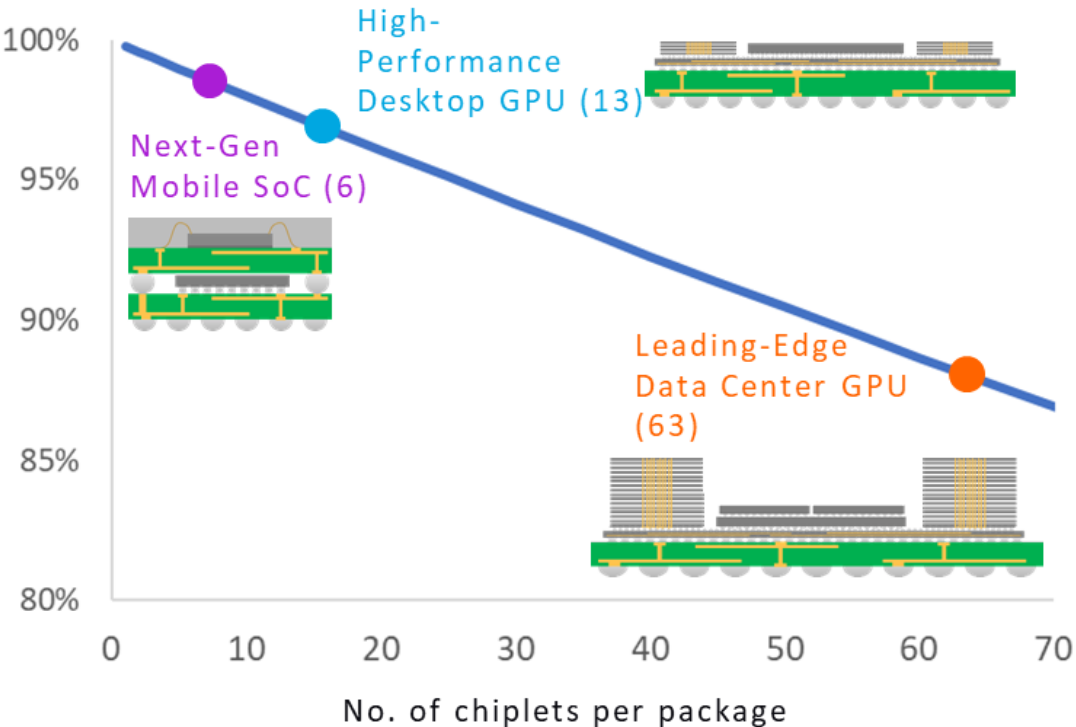
IBM

Known Good Die: Increasing importance



Package Yield Loss from Escapes

Yield @ 2000 DPPM avg chiplet escape rate



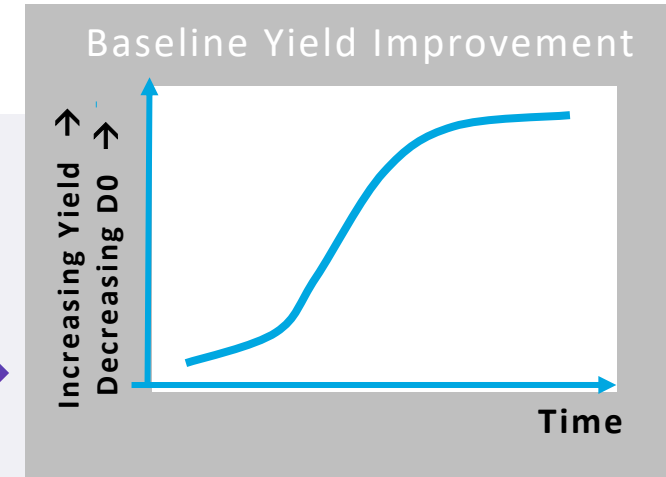
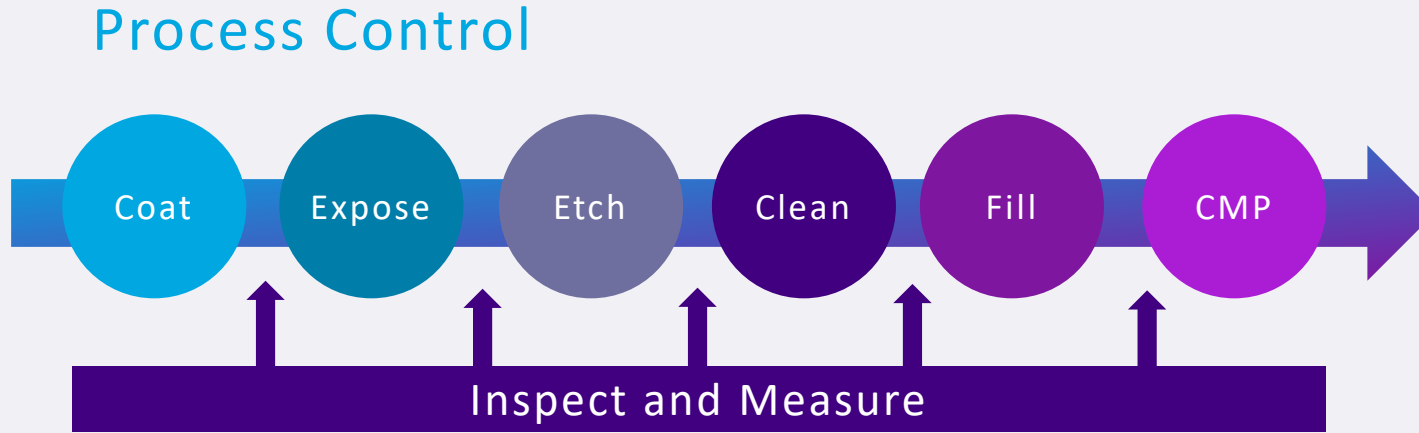
One Bad Die or Interface Kills All

Current methods



Existing Fab Methods for Quality and Reliability

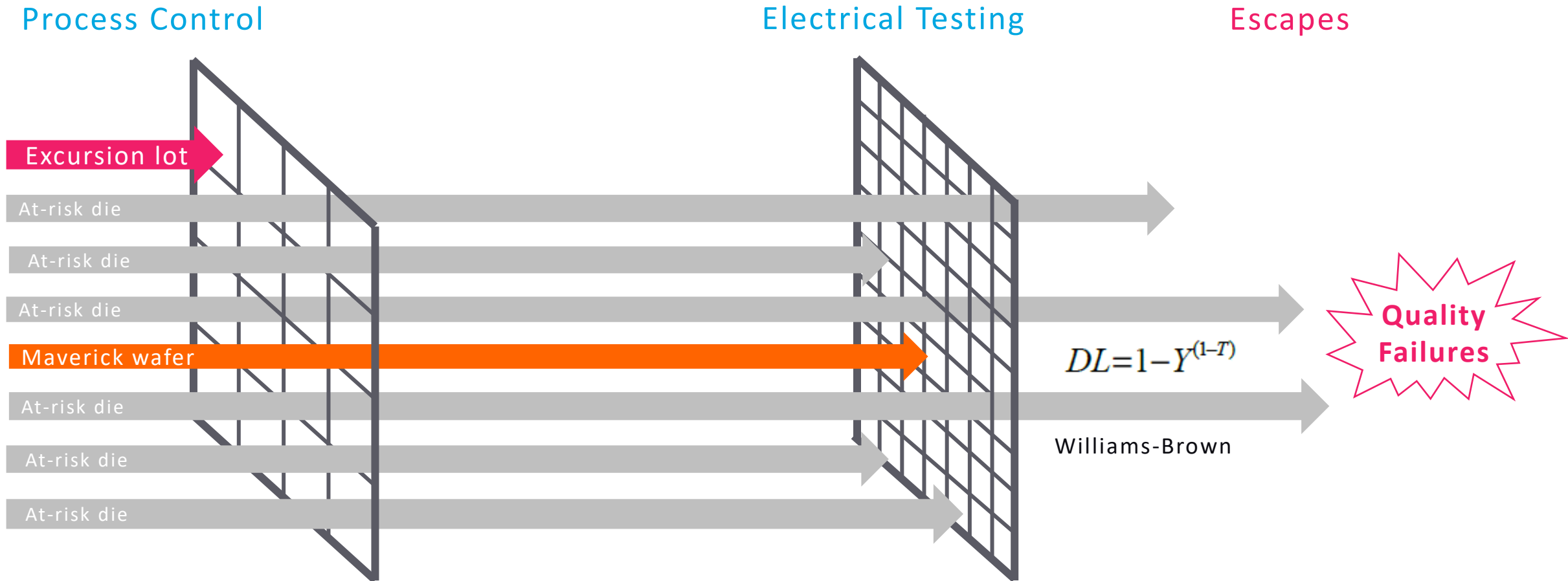
Fewer defects = higher yield = better quality



- Samples small percentage of wafers to identify defect types and sources
- Looks back to process: variation & excursions, systematic defects, random defects from tools & materials

Not all wafers or die will be measured

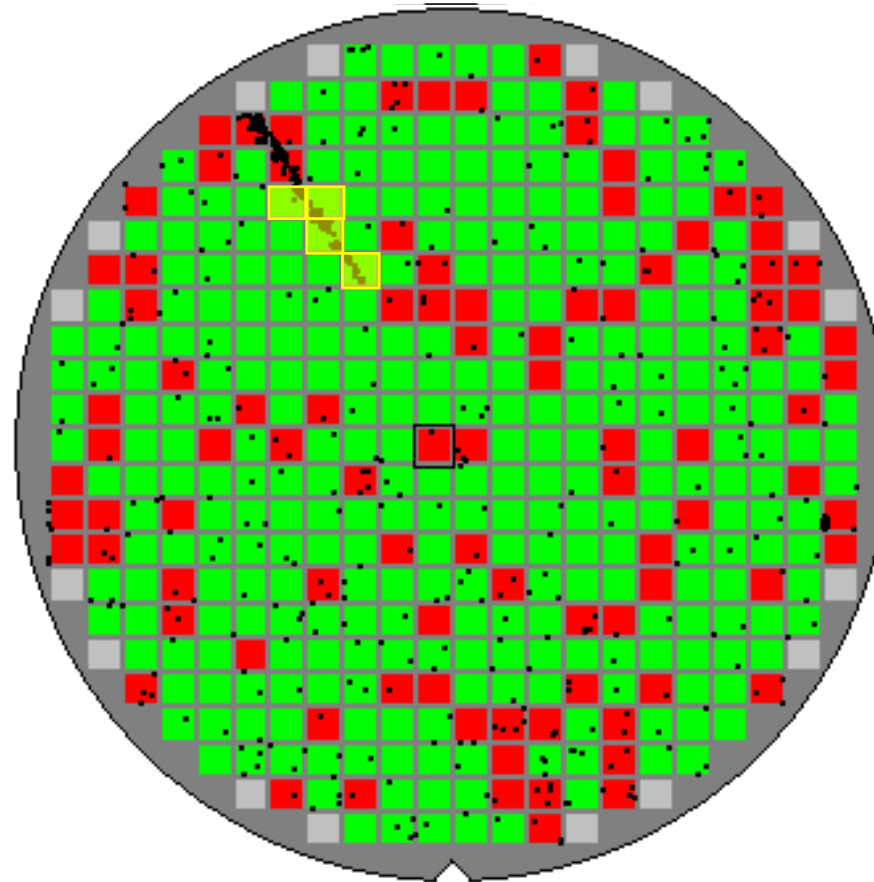
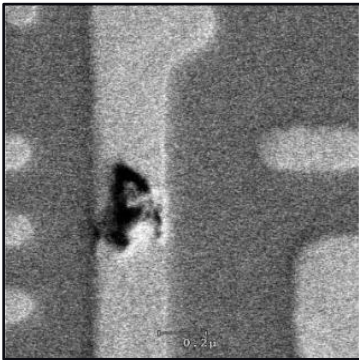
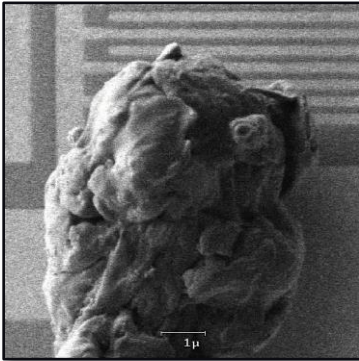
Current Method and Quality Escapes



Low yields and incomplete test coverage allow escapes

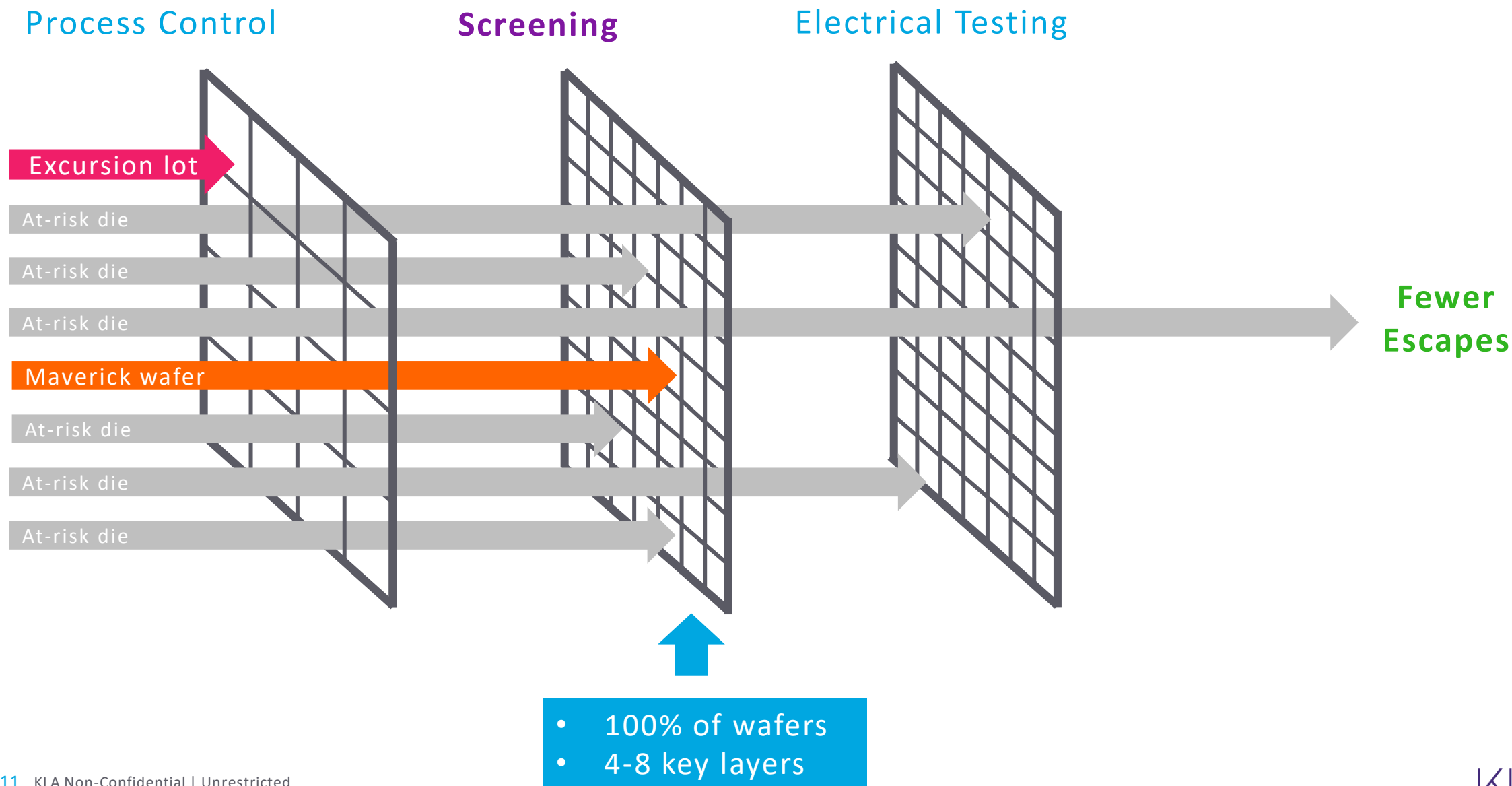
Manufacturing defect data

Stacked EWS and Defect Map



Useful KGD determination data

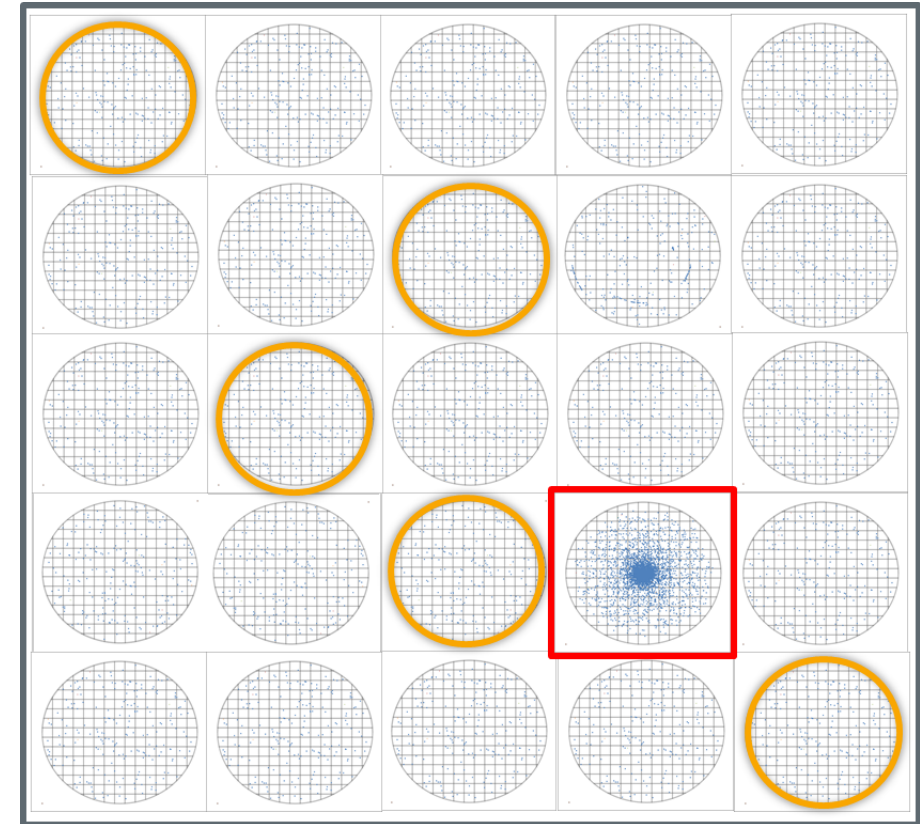
Optical Inspection Screening Adds Another Layer of Protection



Screening Challenges

- Economics
 - Fast enough to cover the WIP at multiple layers
 - Acceptable cost of ownership
- Data quality
 - **Underkill:** Sensitive enough to see the defects
 - **Overkill:** Runtime defect categorization
 - **Actionable:** Data volume cleaning, distillation and normalization. Customized limits. Open format.

Single Maverick Wafer Excursion

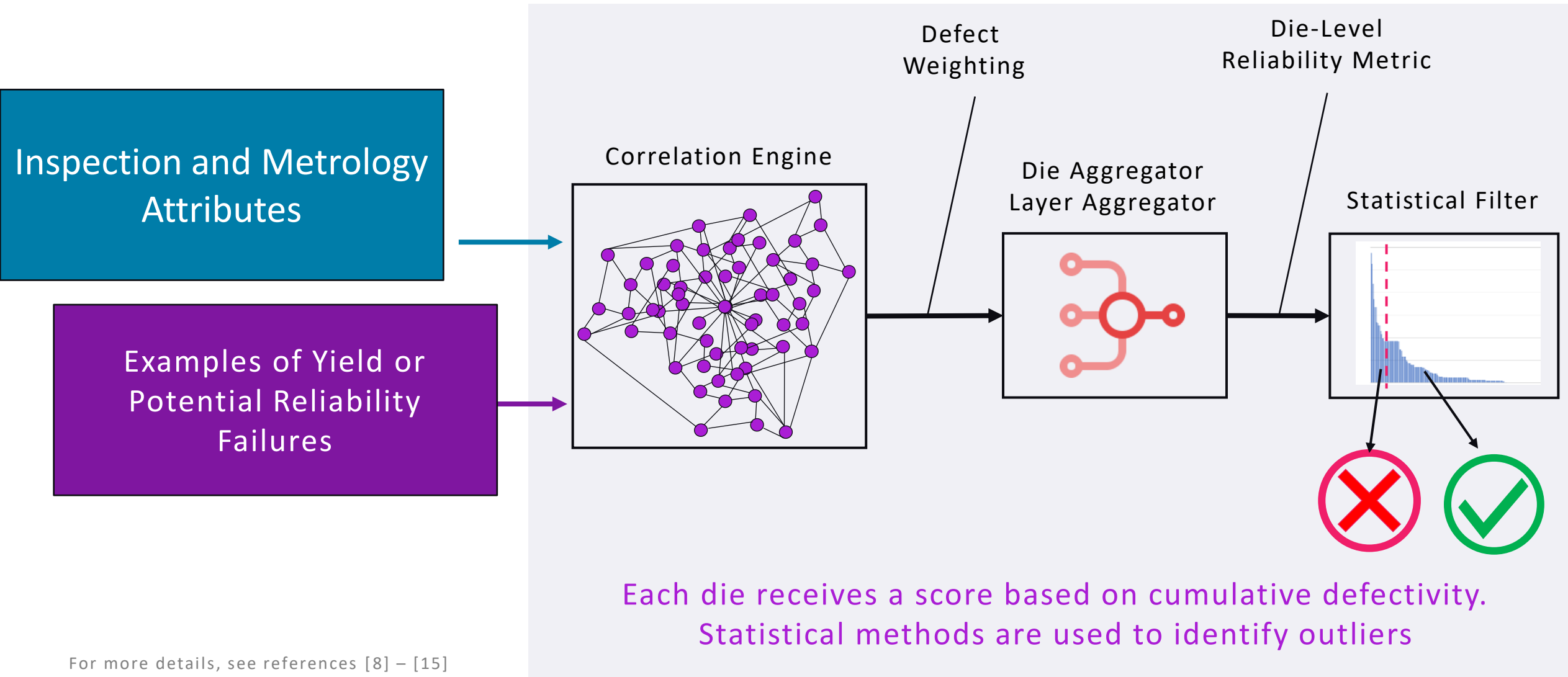


- Legacy 5 wafers per lot sample
- Single wafer excursion

Designing a solution



I-PAT[®]: Inline Defect Part Average Testing



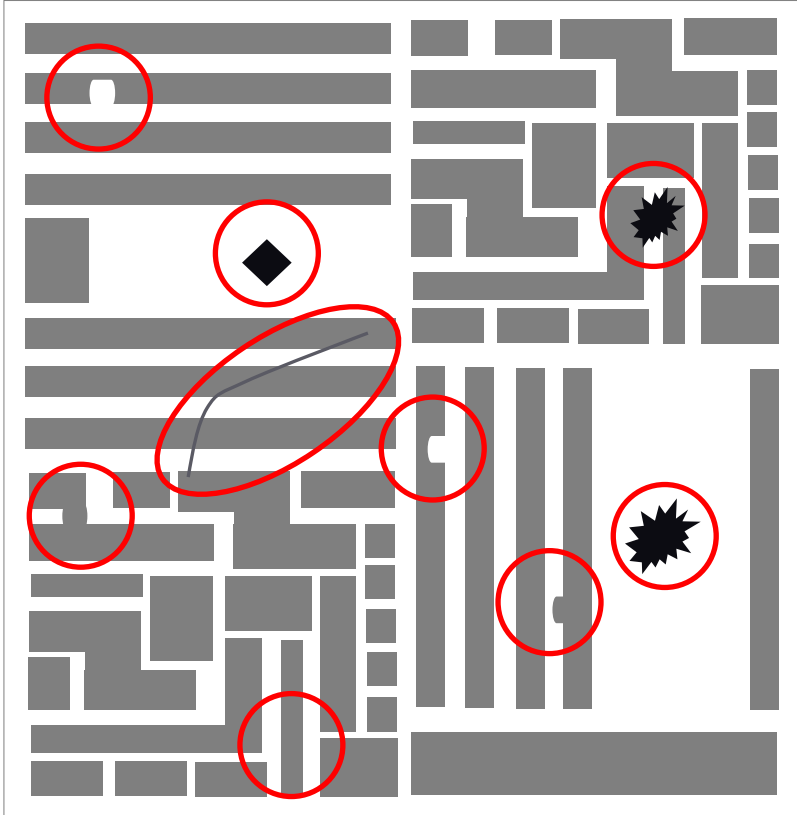
For more details, see references [8] – [15]

Categorize the defects

Runtime Information about each defect on the wafer



Not all defects are equal



User trainable categories or “bins”

■ Extract defect attributes (digital thumbprint)

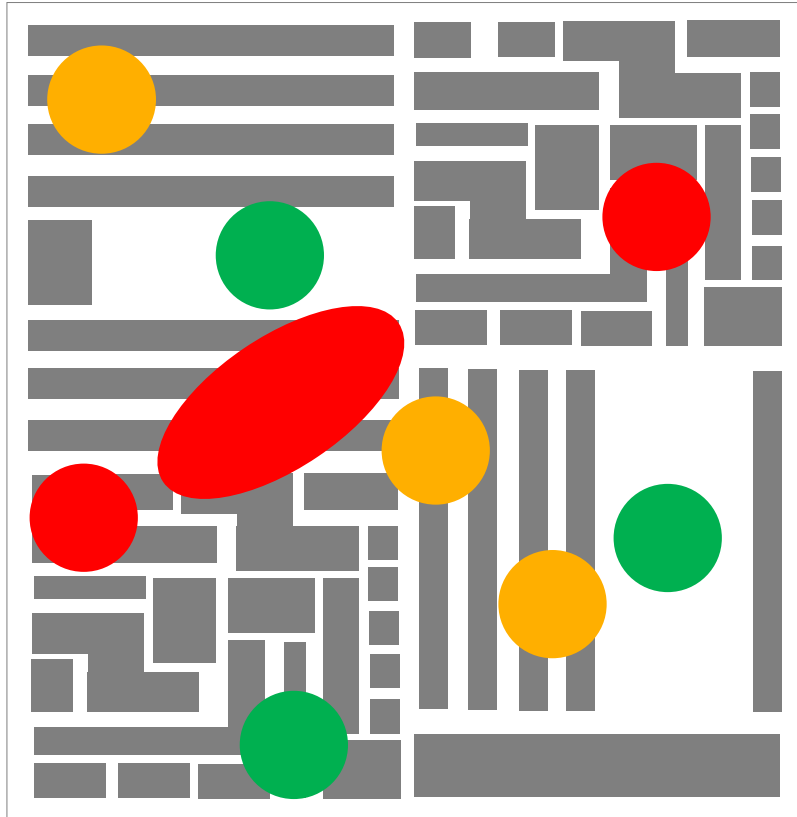
- System:
 - Sensor and channel data
- Physical
 - Embedded/surface
 - Size/aspect ratio
 - Location/region
 - Open vs. dense
 - Intensity/signal vs. background
 - Contrast/polarity
 -



■ Create expert training set with weightings

Assess their impact

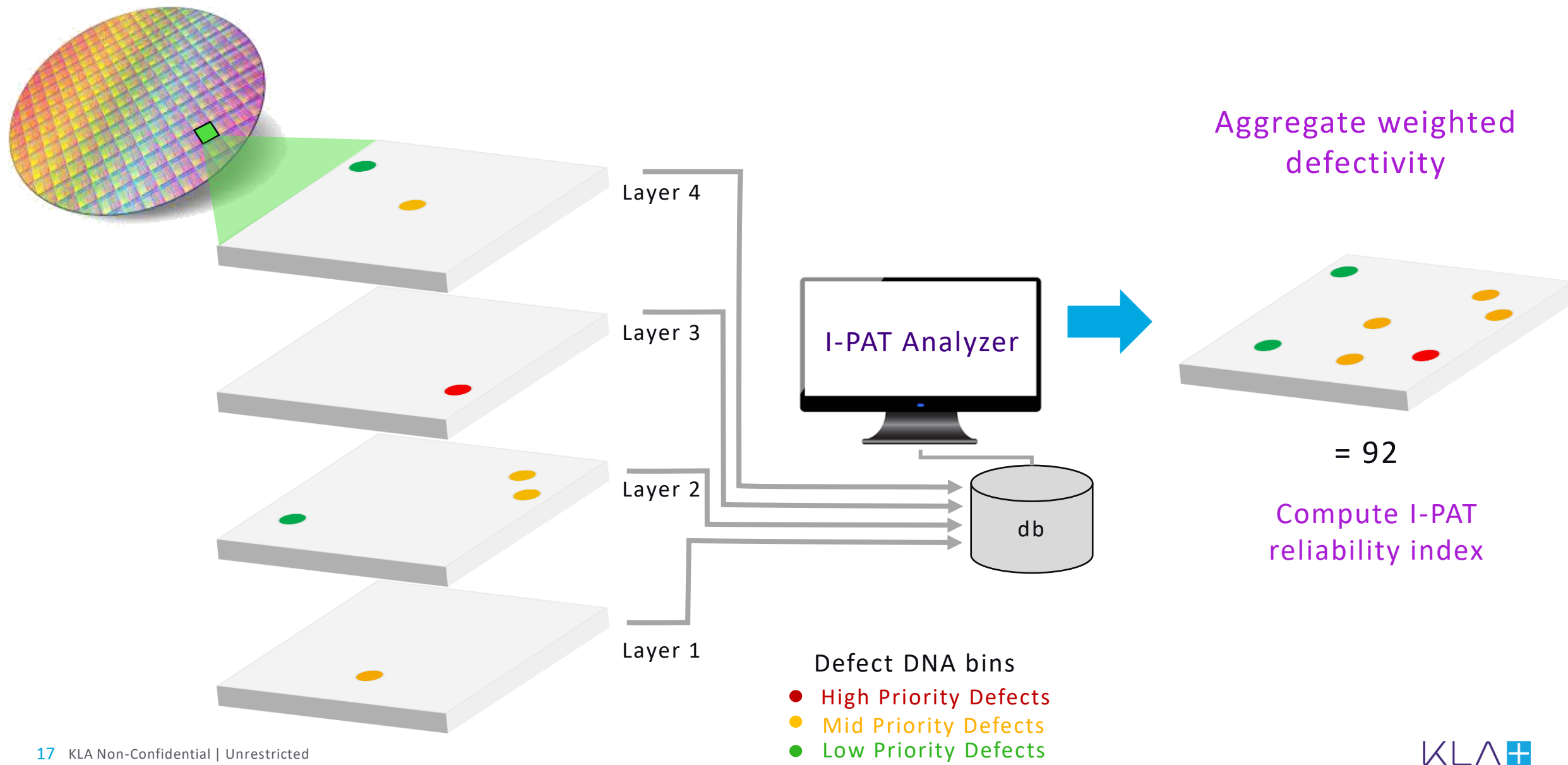
Information about Each Defect on the Wafer



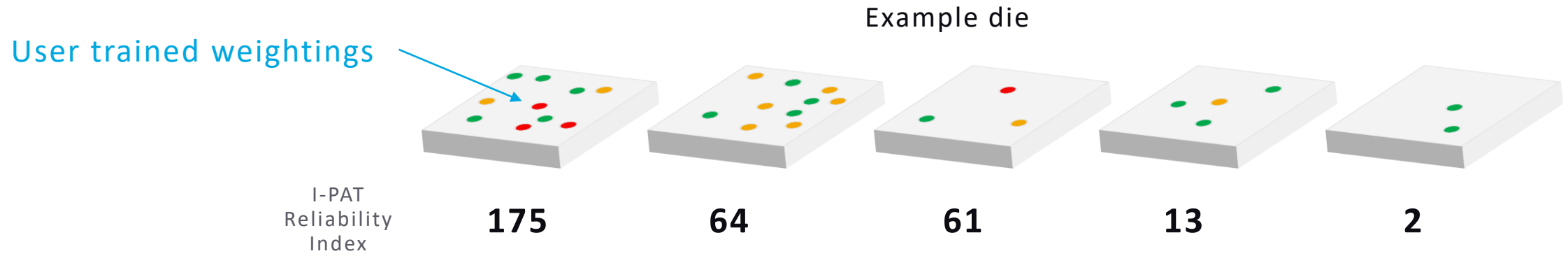
- High Priority Defects
- Mid Priority Defects
- Low Priority Defects

- Runtime Binning
- Machine vision + AI assigns defects to user-trained categories
 - Impact, not source
 - No SEM review

I-PAT: Aggregate score for every die

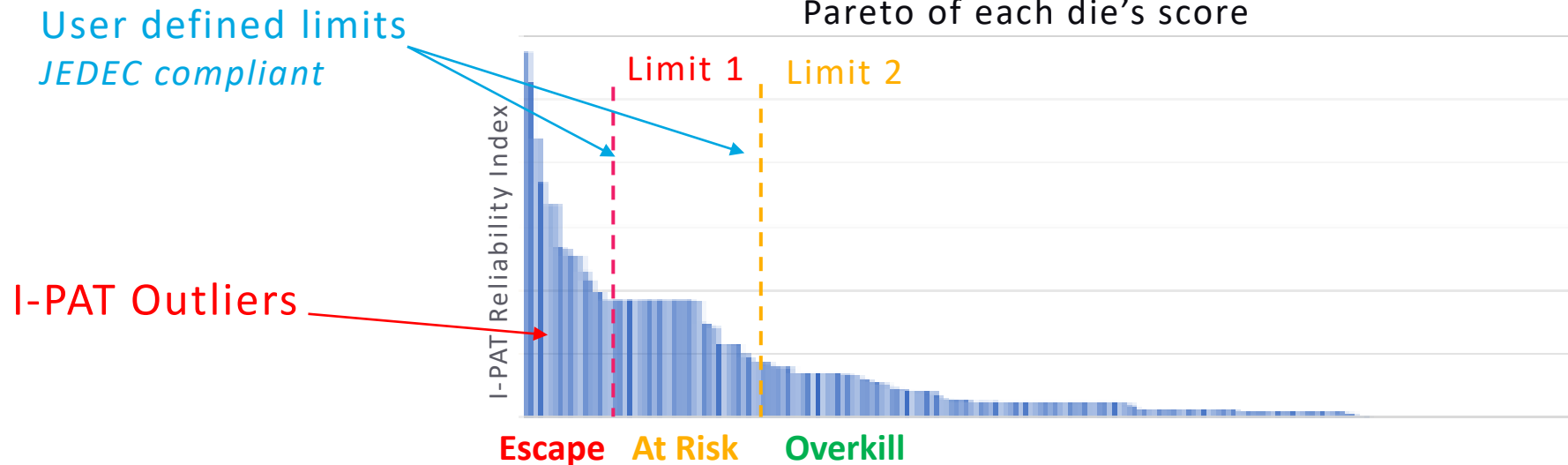


Analyze the Population

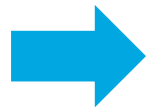


Statistically Filter population

Pareto of each die's score



I-PAT Analyzer:
Export data to fab
outlier reduction
system

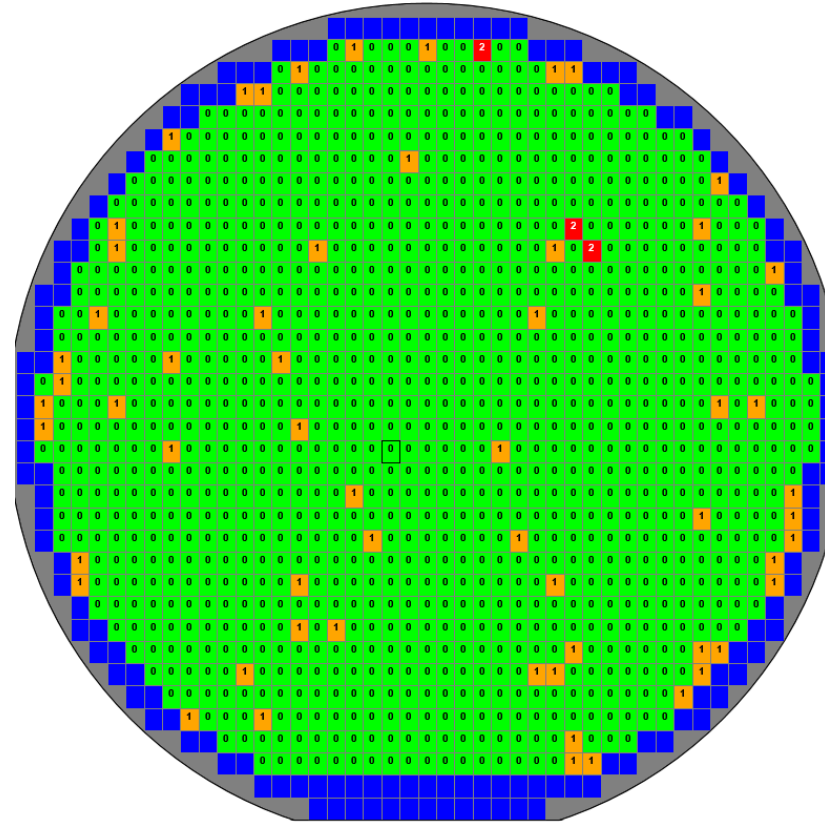


Open Format
KLARF 2.x

I-PAT data at the wafer level

- Numeric scoring by die
- User selectable limits
- Data granularity
 - Total score
 - FE vs BE
 - By layer
 - By die region
- Fab IP friendly

Reduces Noisy Fab Data to Actionable Information



- Low defectivity "Good" Die
- Moderate defectivity "At Risk" Die
- High defectivity. Inked out Die

Case Study



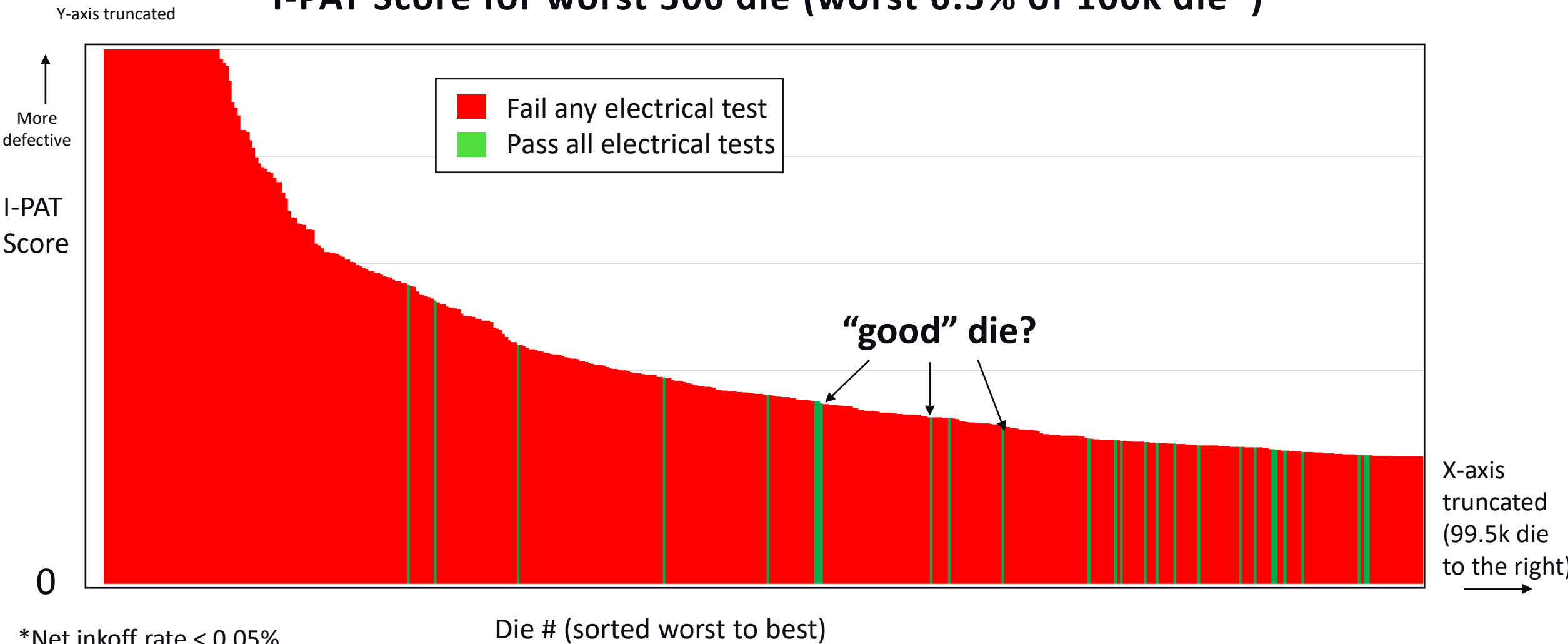
Escape Reduction: Recognizing Bad Die

I-PAT Score for worst 500 die (worst 0.5% of 100k die)



Escape Reduction: Recognizing Bad Die

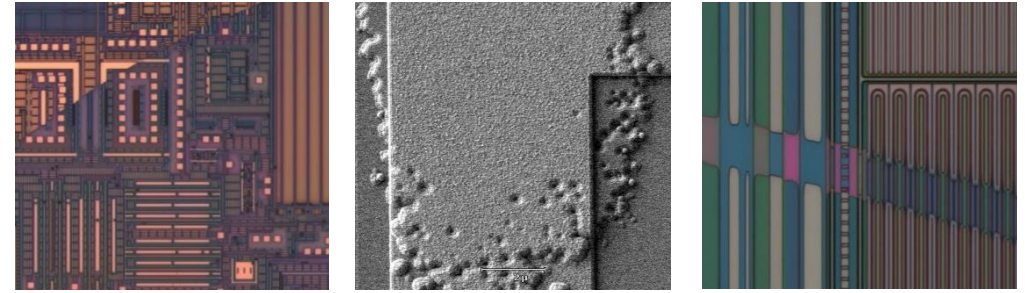
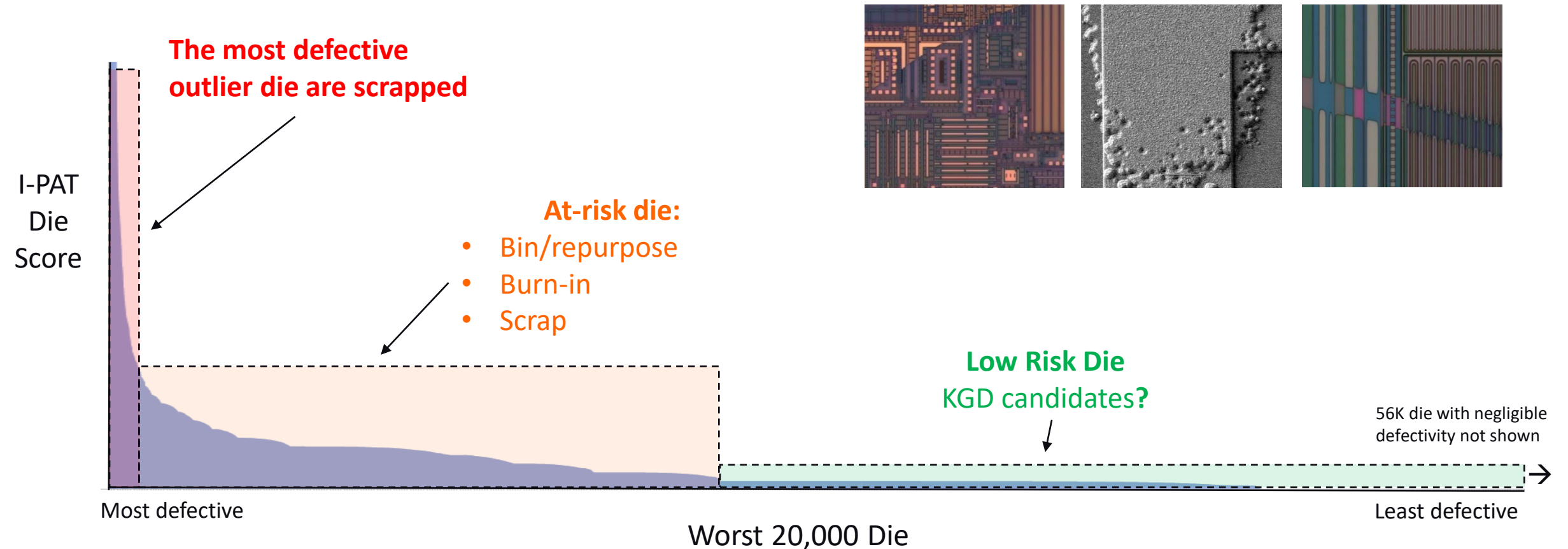
I-PAT Score for worst 500 die (worst 0.5% of 100k die*)



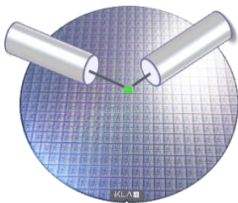
32 highly defective die pass all tests

Applying I-PAT to KGD: (large die population)

- 76,000 die HV Analog die, multi-layer inline defect (I-PAT) screening



I-PAT + Test: Better KGD decisions together

Test score 	I-PAT score 	
✓	✓	Confident good. KGD? Skip burn-in?
	X	Known Bad Die. Scrap sooner to save package, FT costs.
?	✓	Possibly good. Burn-in?
	?	Probably bad. Bin/Scrap
	X	Scrap

Communication challenge: Connecting/incentivizing stakeholders

Thank you

Questions?



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