KGx – Known Good x

September 7, 2022

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Today's Presenters

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ProteanTecs

Jay Rathert
KLA

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Abram Detofsky
Intel

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Zoe Conroy
Cisco

Dave Armstrong
Advantest

Ira Feldman
Feldman Engineering

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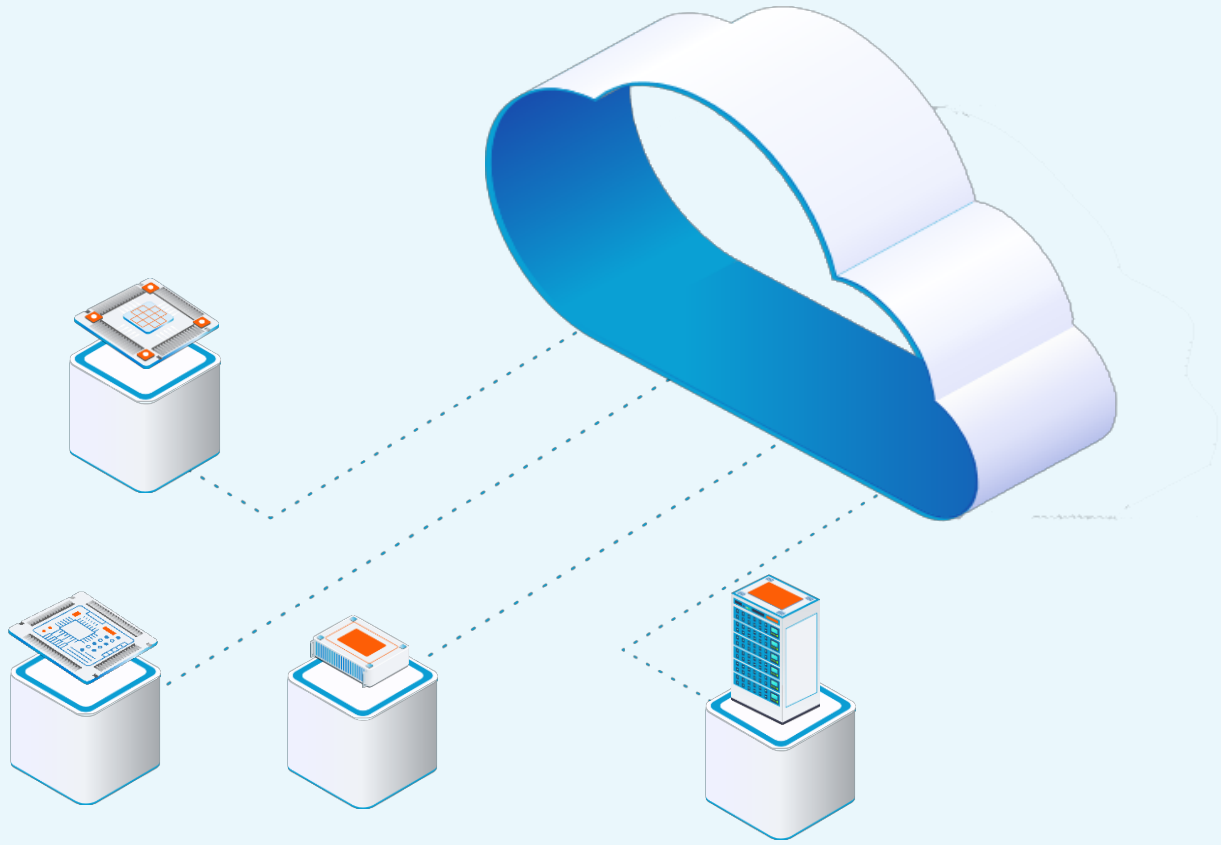
proteanTecs

Electronics visibility. From within

Elevating KGD with Deep Data Analytics



Sept 2022

Marc Hutner, Sr. Director of Product Marketing

proteanTecs Leading a New Category

Deep data health & performance monitoring for advanced electronics

Founded in 2017 by industry leaders and **co-founders of Mellanox**

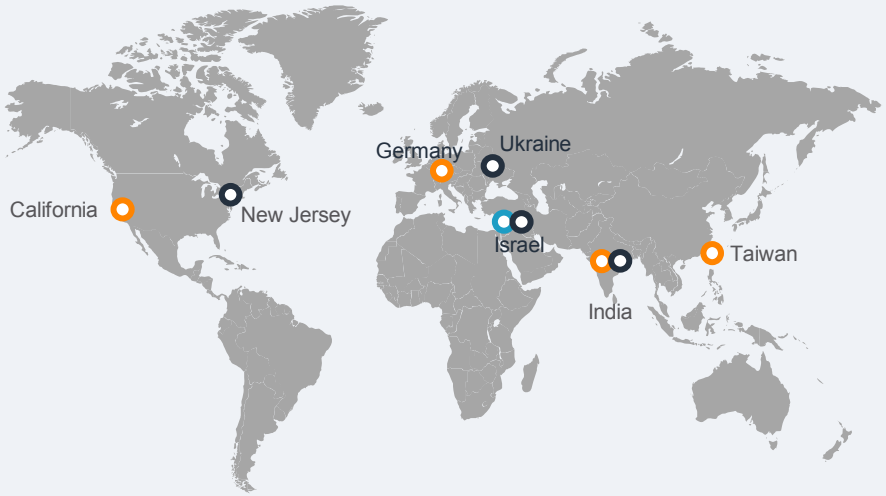
Addressing industry-wide challenges of **scale**

In use and proven in 50+ Design wins

Customers in multiple key segments including **Datacenter, Automotive, Communications, and Mobile**

New category with a **multi-disciplinary** approach

Global Footprint



Backed by worldwide leading investors with a proven track record in the Electronics and SaaS industries

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Responsibility moves to the machine

- Electronics everywhere
- 24/7 availability
- As-a-service

A siloed industry unprepared for scale

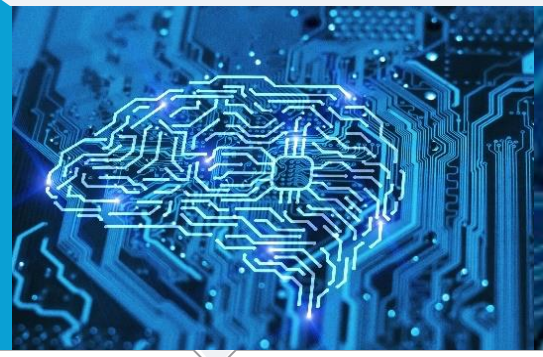
12-18 months of chip **debugging**

Warranty claim rates **2.7%** of **product revenue**

50% of fault investigations **inconclusive**

1 **car failure** per hour

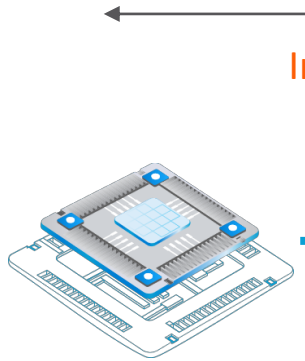
Mega functionality



- Advanced technologies
- Quality/ performance tradeoffs
- Surging costs

Sources:
1. McKinsey & Company, Advanced Analytics in Semiconductor Manufacturing; 2017
2. Warranty Week, Warranty Claims Rates by Industry; 2019
3. Internal calculations
4. Audi, DVCon Munich, 2017

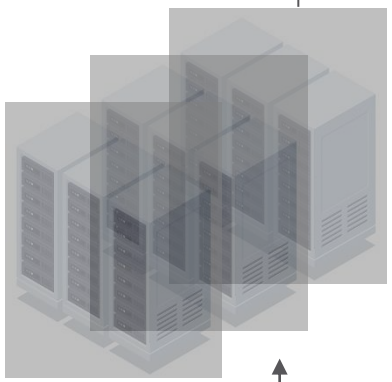
Challenges in High Performance Computing Resilience



Advanced Electronics

Inconclusive Investigations

Undetected defects



- HW failures and service disruption
- No in-mission monitoring solution
- Expensive redundancies
- Constant replacements
- Lifetime reliability and safety concerns

Market leaders are looking for answers from the industry

facebook

"Silent data corruption due to silicon latent defects and aging. (1,000 DPPM!)"

Microsoft

"Frequent unexplained HW failures with "No Issue Found" at high rates"

Google

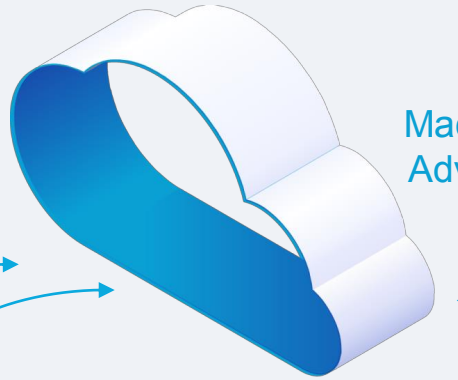
"Rare, short-term computational errors on systems that passed all manufacturing tests successfully"

CARIAD

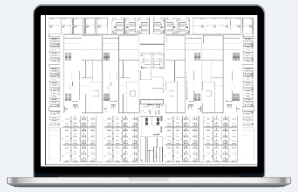
"Current FuSa guidelines do not cover HW/system reliability during the operational lifetime"

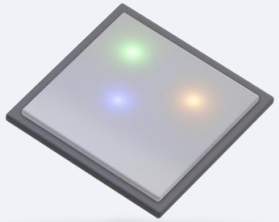
1. "Silent Data Corruptions at Scale"; Harish Dattatraya Dixit Et. Al., Facebook, arxiv.org/abs/2102.11245, Feb. 2021
2. "Cores that Don't Count"; Peter H. Hochschild Et. Al., Google Research, Jun. 2021
3. "Circuit Reliability Mitigation Techniques & EDA Requirements", Georgios Konstadinidis, Google, EDPS 2019
4. "Improving Cloud Scale Hardware Fault Diagnostics", Neeraj Ladkani, Rama Bhimanadhuni, Microsoft, Mar. 2020 OCP Virtual Summit
5. "Automotive semiconductor reliability and its changed importance for complex system engineering, Andreas Aal, Volkswagen, Dr. Oliver Aubel, Globalfoundries, IRPS 2021

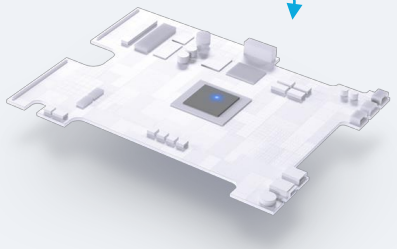
Visibility at Every Stage

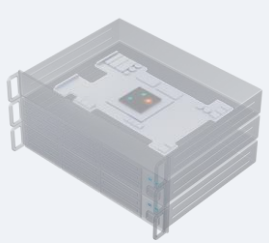


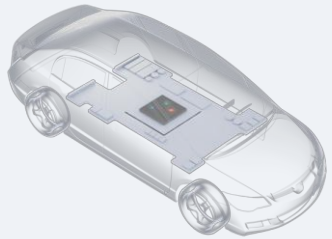
Machine Learning &
Advanced Analytics











Chip Design

Variability Analysis
Production Visibility

Chip Production

Higher Confidence Volume Ramp
Outlier Detection
Performance Yield

System Production

Performance Optimization
Workload Analysis
Environmental Monitoring

In-Field

Performance Monitoring
Alert on Faults before Failures
Predictive Maintenance

Faster Time to Market **10X Lower DPPM** **Reduced Costs** **Failure Prevention**

Multi-Pillar Solution

Deep Data

Universal Chip Telemetry™ (UCT) with on-chip Agents

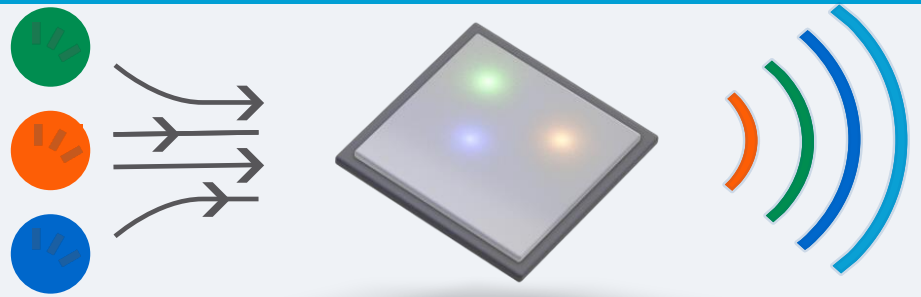
Machine Learning

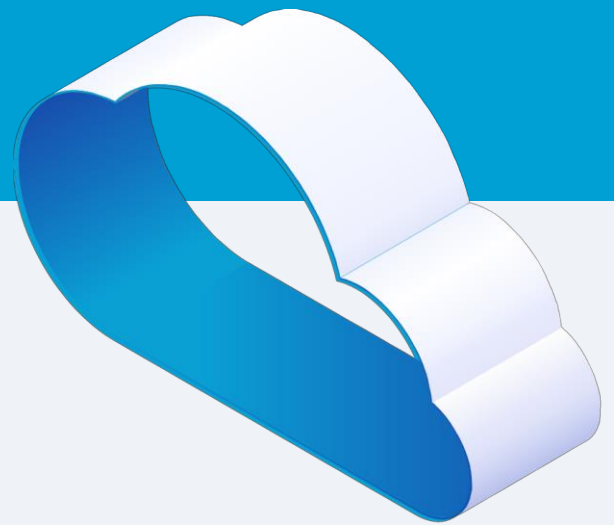
Agent fusion and inference with ML algorithms

Cloud & Edge Analytics

Advanced analytics for actionable insights

Automated insertion tools

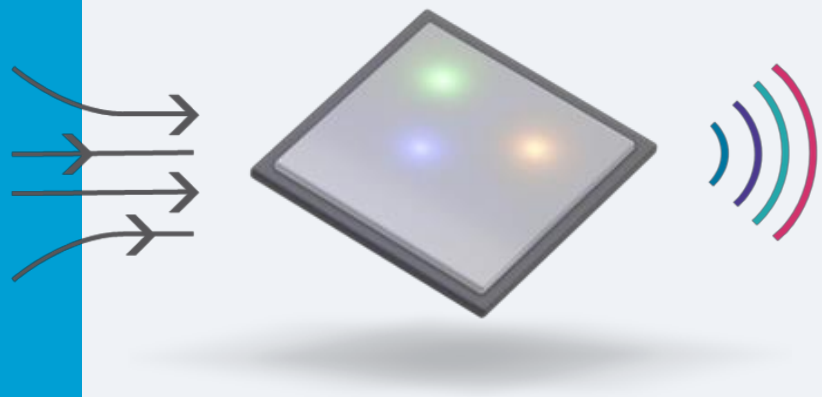


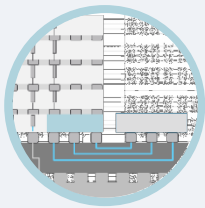


Universal Chip Telemetry™ (UCT)

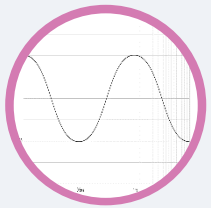
On-chip Agents built for analytics

- Parametric measurements
- High coverage & high resolution
- Minimal PPA penalty
- Operate in mission-mode
- Sense the surrounding electronics
- Application optimization to HW

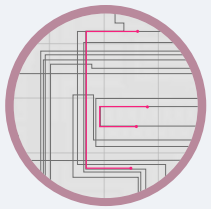




Interconnect Performance Monitoring



Operational Monitoring

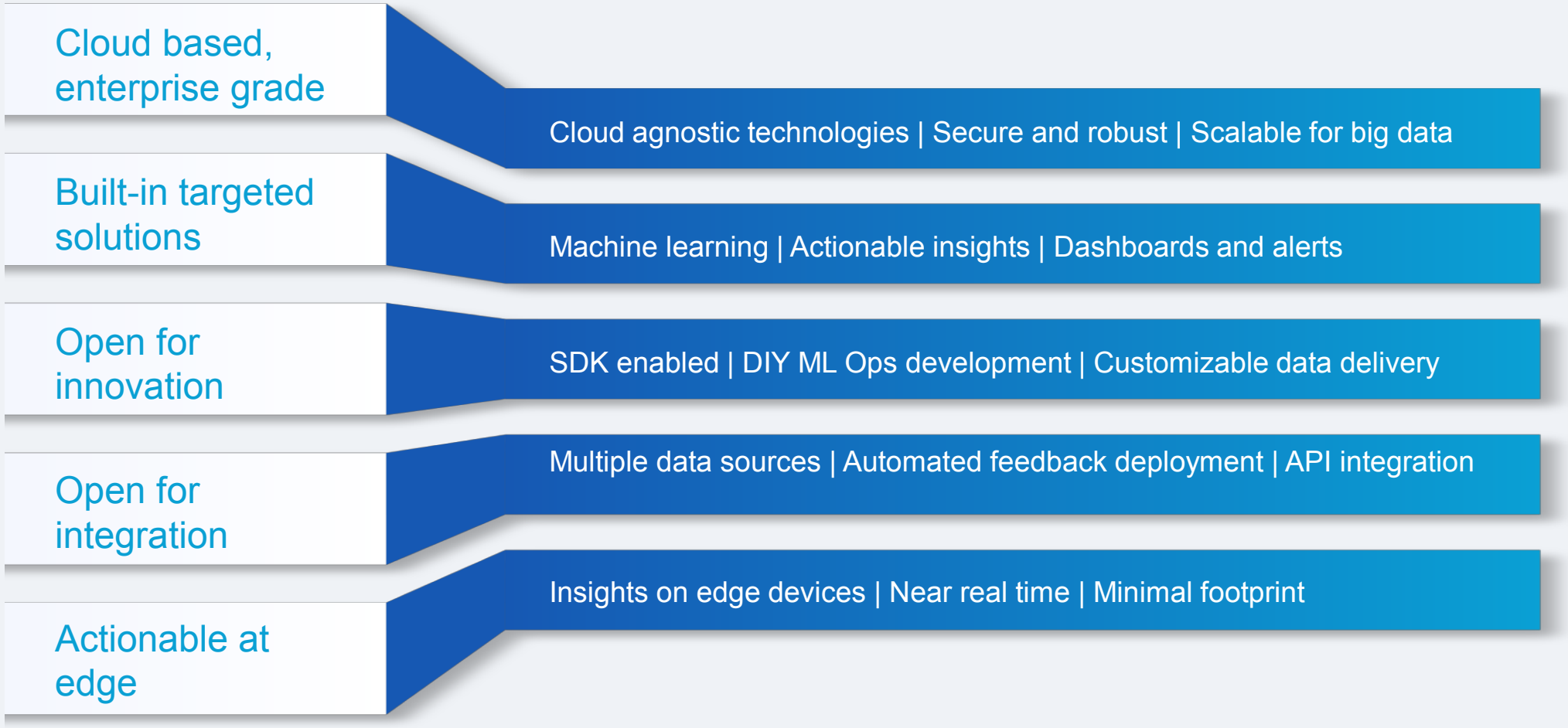


Performance and Degradation Monitoring

Classification and Profiling

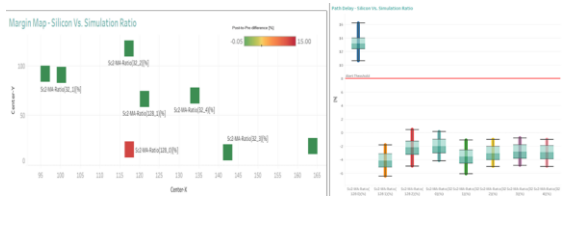
Introducing Proteus™ Platform

Flexible, easy-to-use and deep lifecycle analytics for advanced electronics



Proteus Targeted Analytics

Chip NPI



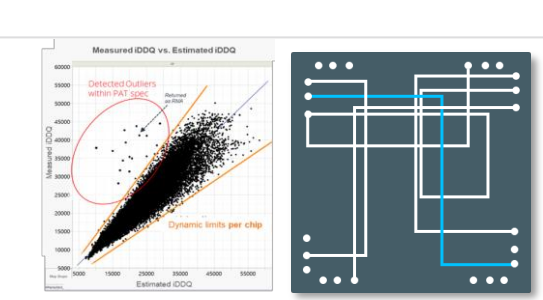
Post to Pre silicon correlation

Correlation between value chain stages

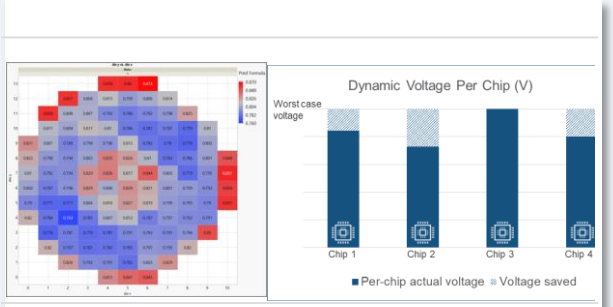
Performance Tuning

Degradation monitoring in qualification

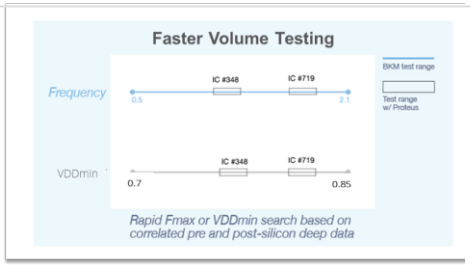
Chip Production



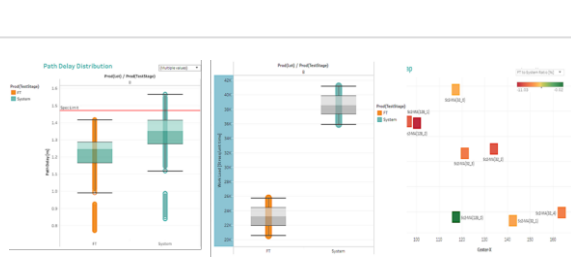
DPPM Reduction (Fine grain latent defects screening)



Power reduction



Test time reduction

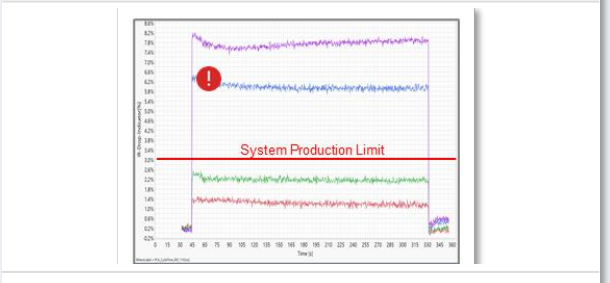


Lower RMAs and Fast Time-to-Resolution

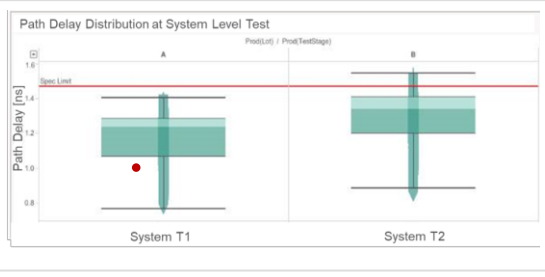
Proteus Targeted Analytics

System NPI & Production

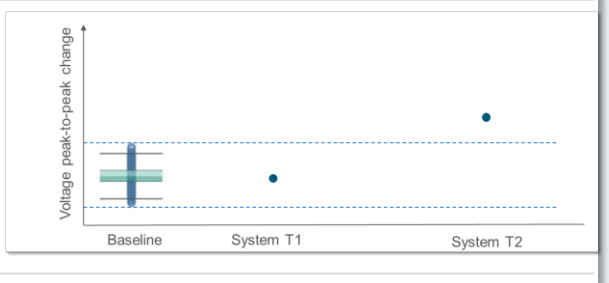
Performance Optimization (HW-SW)



Quality: Chip as system monitor

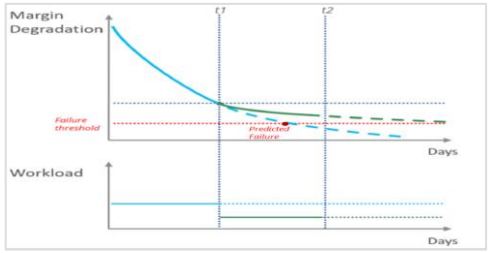


System performance early predictions for TTR

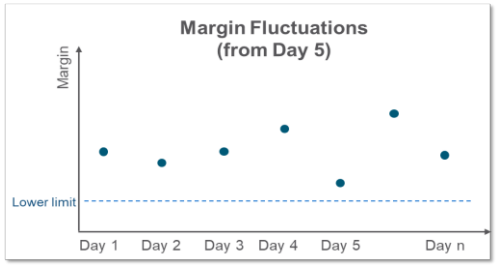


Debug & root cause analysis

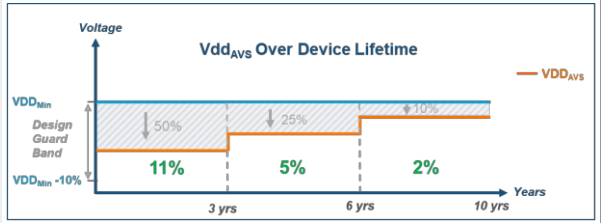
In-Field



Predictive Maintenance



Continuous performance monitoring



Real time applications
(Power, Performance & Reliability)

RMA Reduction with Fast Time-to-Resolution

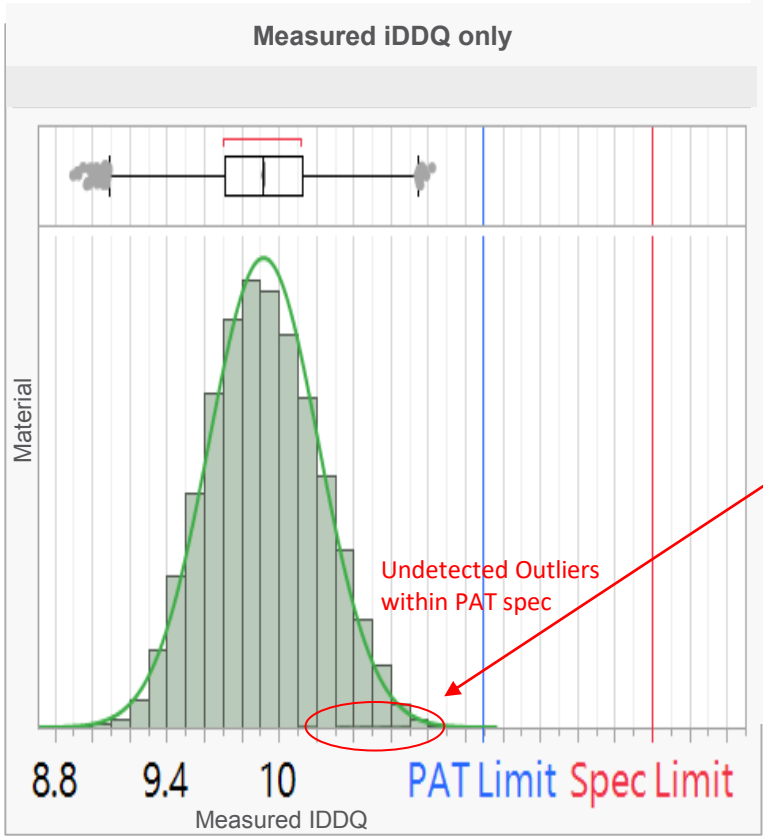
Use Cases

Estimator Based Outlier Detection

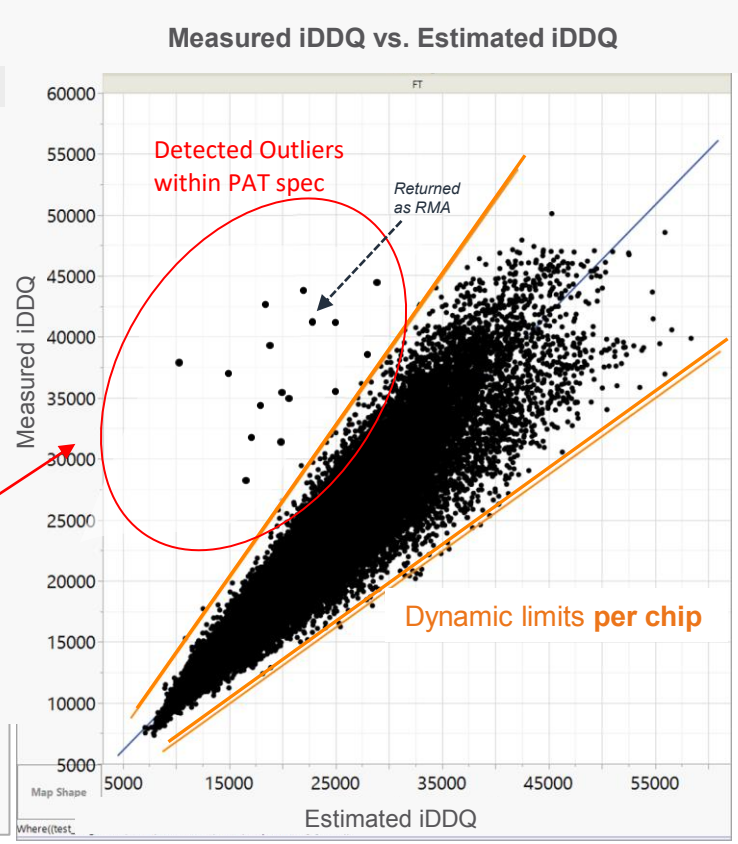
- Personalized chip assessment
- Multi dimensional outlier detection
- Yield reclamation
- Fast RMA with pinpoint Root Cause Analysis

BKM: Population based

proteanTecs: Dynamic limit per chip



One dimension only identifies outliers ***outside*** of PAT spec limits (circled in red – unidentified outliers)



Additional dimension to identify outliers ***within*** PAT spec limits (circled in red – identified outliers)

Correlation Across Stages

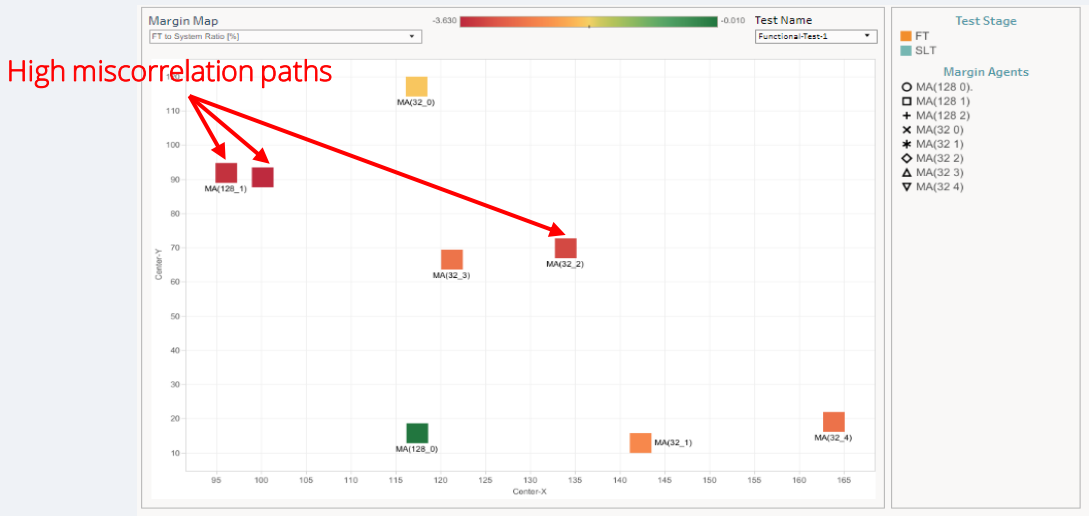
Accurate correlation & validation between test stages: setup and test stress

Optimization of test conditions across all test stages (WS, FT, SLT, ST)

- Test limits and guard-bands, test equipment validation, etc.
- Accurate characterization of operational, environmental and stress effects

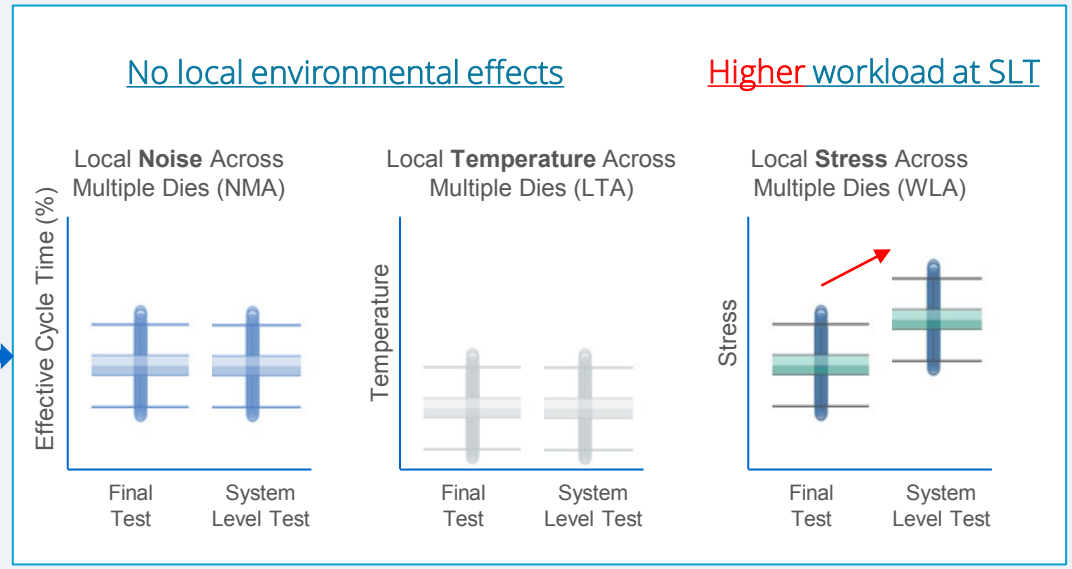
- ATPG structural test tuning - correlative to real application at system
  - Common data ‘language’ between ATE and system test

System Level Test to ATE Miscorrelation



IC spatial view: Lower margin detected at SLT

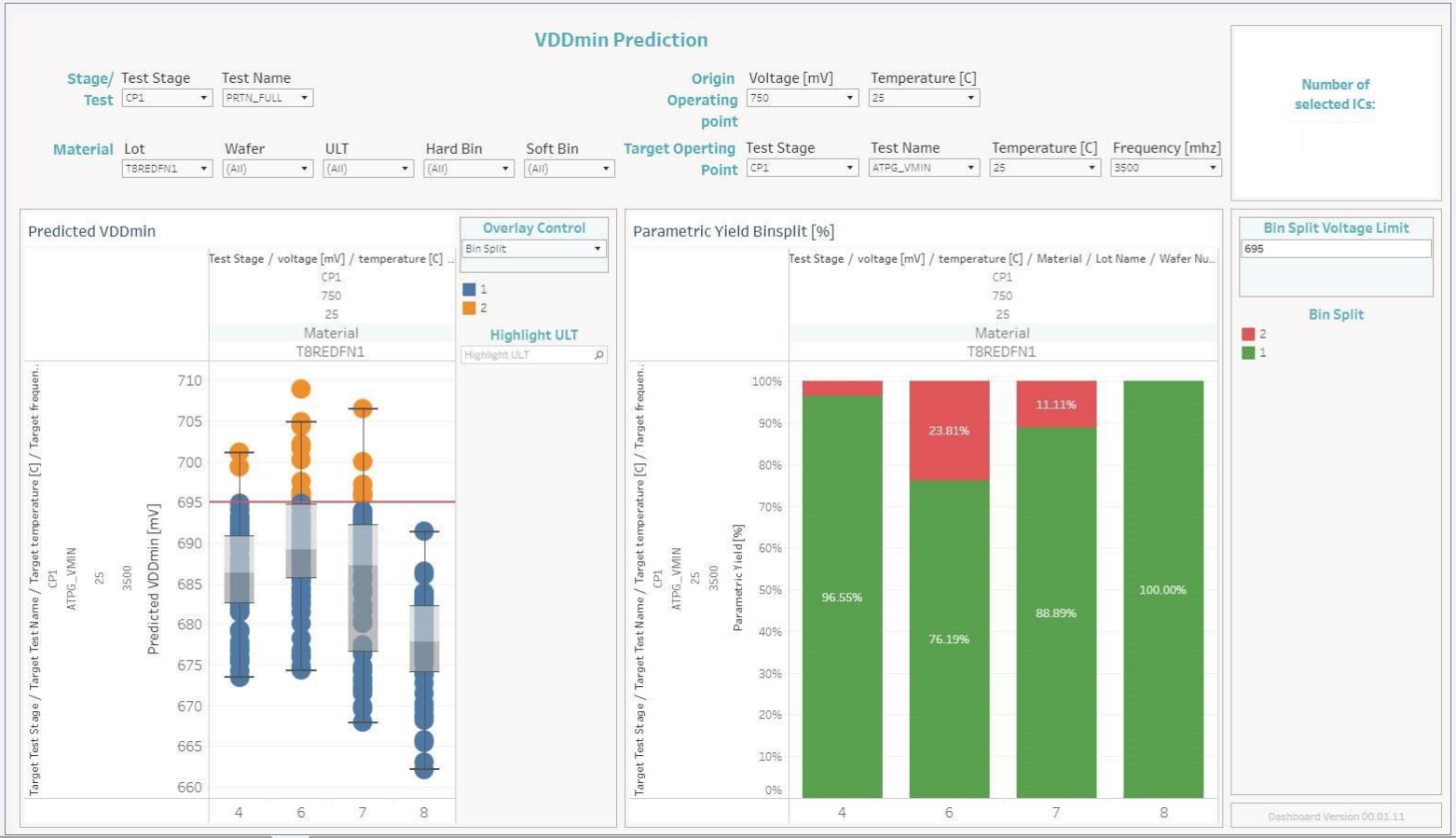
RCA



Example source of issues: Poor Performance Coverage at ATE

Operational Savings Vddmin predictor at HVM

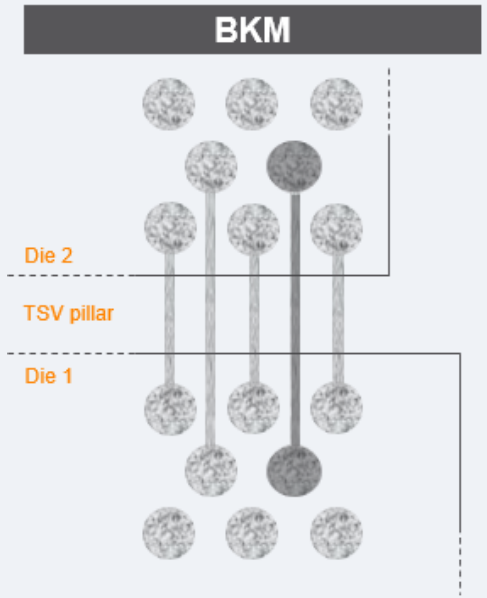
Early & accurate binning assessment for Final test or System @Wafer Sort: Cost reduction, operational efficiencies
Test time reduction: Avoid doing Vddmin search in Wafer sort and/or Final Test



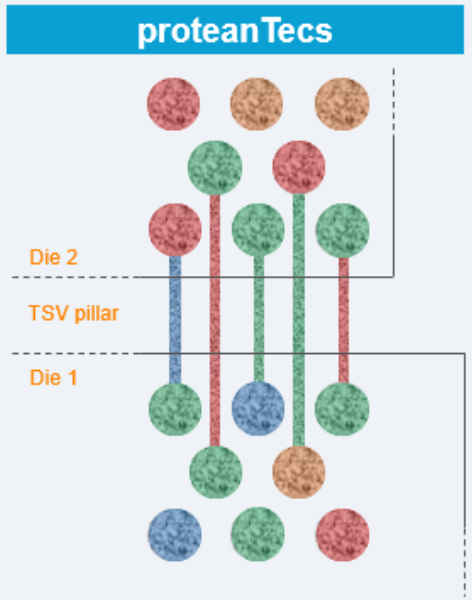
- Models built in proteanTecs Platform and deployed at the Test floor
- Multiple Vddmin predictors @Freq (or many Freqs) for different tests
- Similar application for Fmax prediction @ V (or different Vs)
- Predictions for different tests and test stages

Characterization and Test for D2D interfaces

- Comprehensive parametric lane grading
- 100% lane coverage
- During test and in-mission
- Data analytics capabilities



Pass or Fail for the entire lane

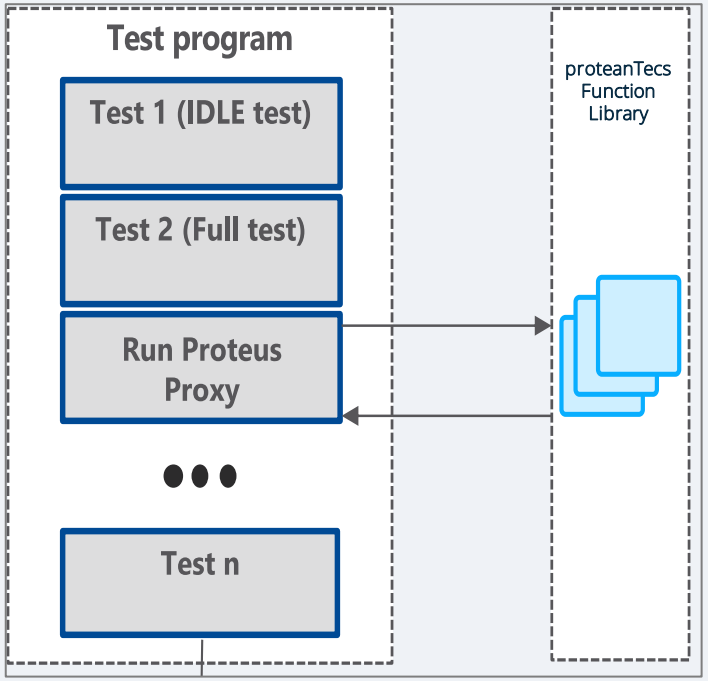


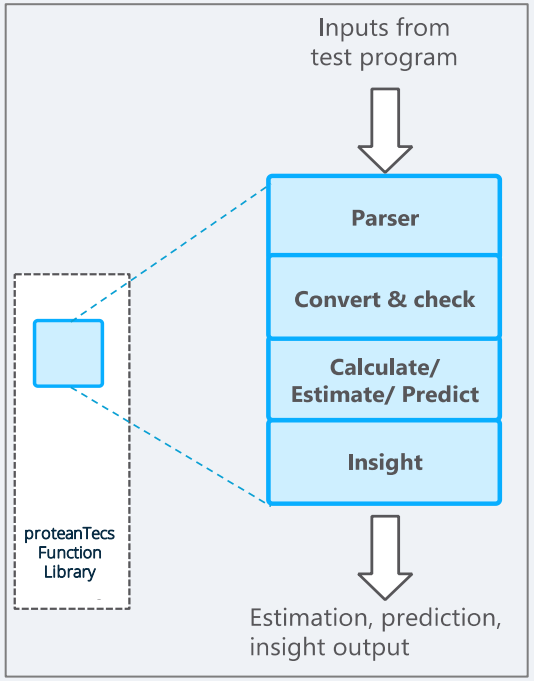
Grade of Marginality per specific component

- **Go beyond just Pass/Fail testing**
- **Complementary to proteanTecs comprehensive chip performance and health monitoring solutions**

proteanTecs at the Edge:
Models deployed for wafer sort or final product

- A subset of the proteanTecs capabilities, called the proteanTecs Library, can be run at the test floor for low latency, “real time” decisions and insight
- A proteanTecs function library is called from within the test program. This function library is integrated as a *dll* as part of the test release





System Performance Monitoring

Agent data recorded throughout multiple phases of system operation:

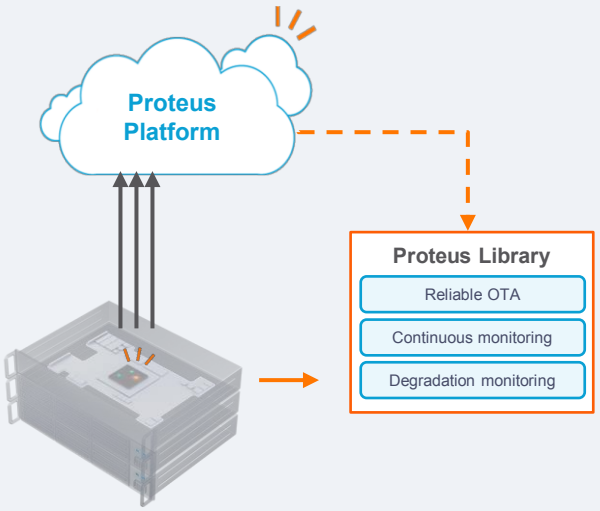
- Configure
- Operation Start 1
- Operation End 1
- Idle 1
- Idle 2
- Operation Start 2
- Operation End 2
- Idle 3
- Idle 4

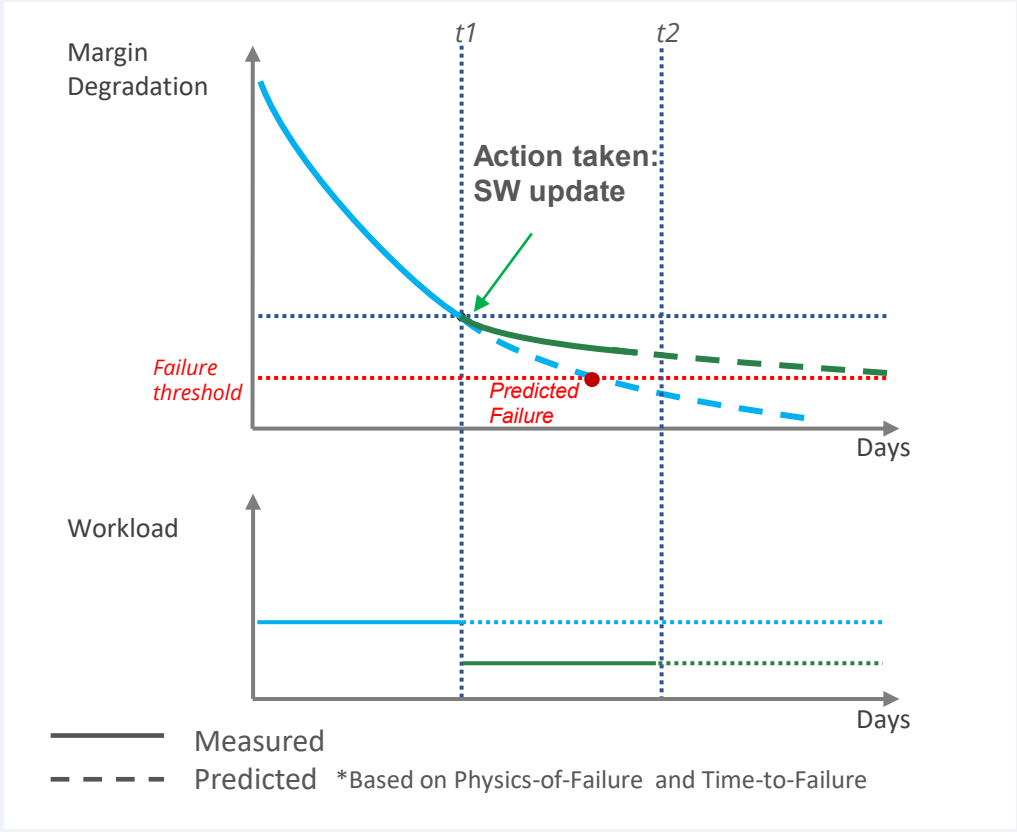
- Correlating and merging different Agent measurements
- Margins of millions of paths
- IR drop
- Workload/stress: V*T*Toggle rate
- Cycle to cycle clock jitter

Bring up & Production EOL software optimization and performance tuning

Health Monitoring with Alerts on Faults Before Failure

- UCT-based continuous performance and health monitoring
  - In mission-mode
  - High coverage critical path monitoring based on millions of internal paths and low margin alert
  - Correlated to system environment and application induced stress
- Workload management for achieving longer product lifetime
- High reliability through personalized Predictive Maintenance





Customer Success Stories

FORTUNE 50 NETWORKING COMPANY

18% power reduction in chip

IR drop recovery at SLT

"The average voltage improvement is around 6~7steps and this is significant since it's such a big chip"

LEADING FABLESS SEMICONDUCTOR COMPANY

2% yield improvement due to feed back to the fab of design sensitivity to process

Inferred process parameters per die detected sensitivity of yield to process

"The proteanTecs analysis helps us to prove the correctness of external circuit modification and the chip design quality"

LEADING ASIC VENDOR

Detection of silicon-to-simulation miscorrelation in 5nm testchip

Post-to-pre parametric correlation

"proteanTecs speeds chip and system bring-up, significantly reducing time-to-market"

FORTUNE 50 NETWORKING COMPANY

5% system outlier rate detected at System Test

Latent defect detection of thermal effects

"Solid and leverageable data flows"

AUTOMOTIVE STARTUP

Board redesign due to detection of PDN issue

IR drop detection at SLT

"They made us look like a 15 year semi company"

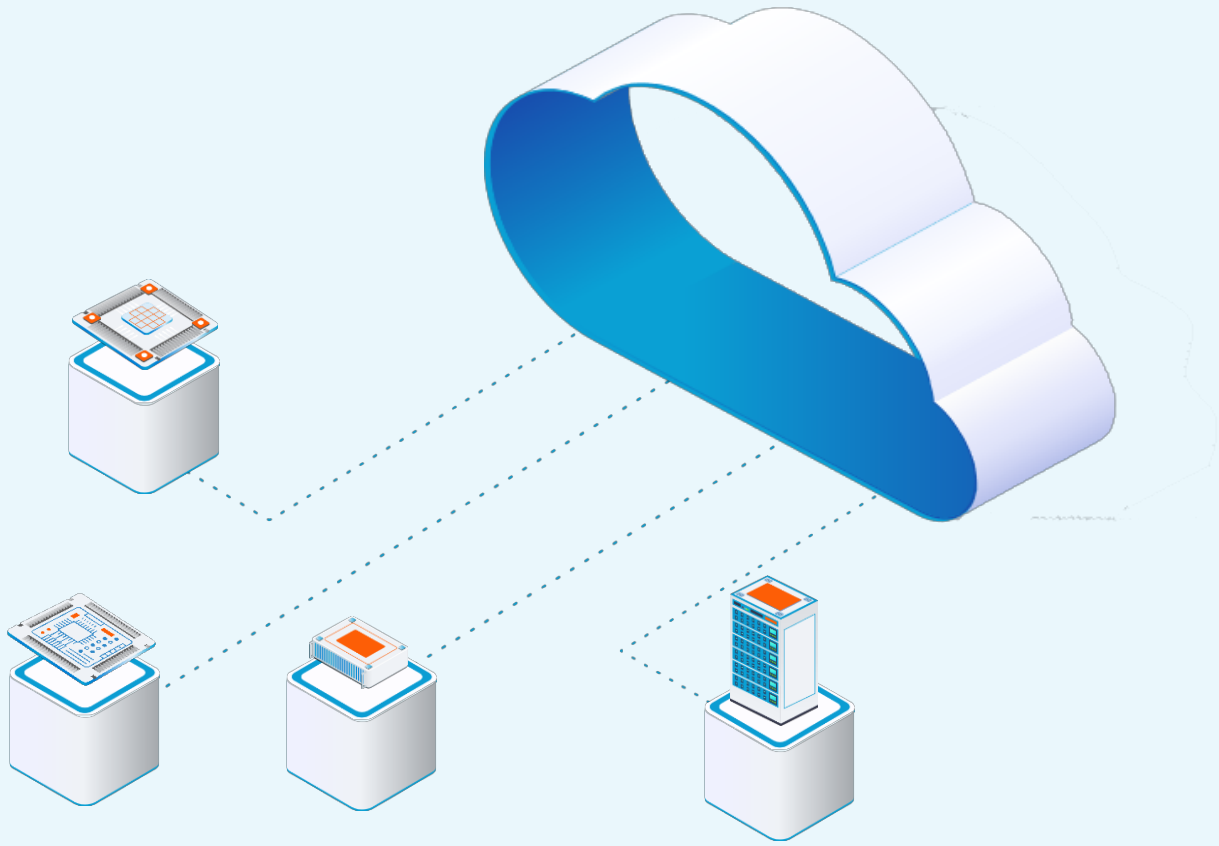
Concluding Thoughts

Deep Data Analytics is required for KGD

- New level of silicon and system understanding
- Enables shift left for wafer sort
- Provides visibility for interaction of chiplets within package
- Diagnoses interaction of SW with HW
- Methods can be used at every stage from Wafer Sort to in-field

Thank you.

marc.hutner@proteanTecs.com



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