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3D IC Test Strategy

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March 10, 2023

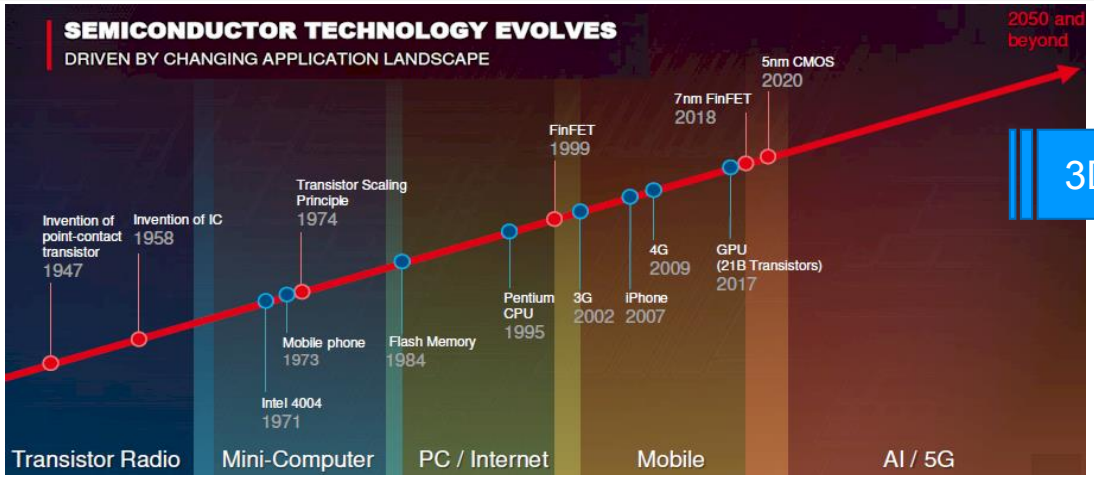
Abstract

- ✓ 3D IC development from true 3D monolithic integration or through diversified advanced packaging technologies that include 3D WLP, 2.5X/3D interposer/substrate-based integration, 3D heterogeneous integration, or Chiplet has emerged as a faster alternative and more feasible strategy than planar transistors scaling as predicted in Moore's law.

- ✓ OSATs and Foundries have been the major players taking the initiative by offering 3D IC turnkey solutions that include the Test Strategy. However, 3D IC Test Methodologies and DFT solutions have still not been explored much in the global Packaging and Test Research community.

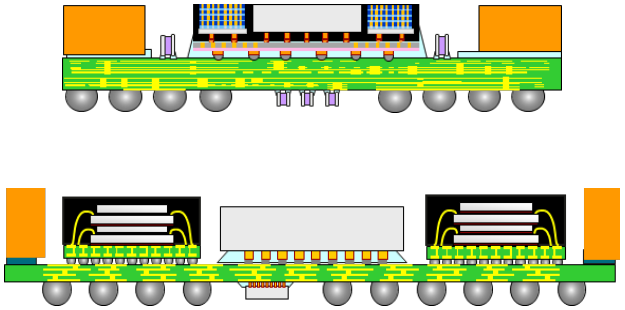
- ✓ Test challenges are obviously still complicated in certain aspects including specific function or parameter testability, defects narrowed down debugging, complex test coverage, and test economics. Determining the appropriate DFT methodology, Boundary Scan Description Language (BSDL) implementation, and how IJTAG complements this 3D IC test strategy for each specific product function and application will be the focus of this concept-level discussion.

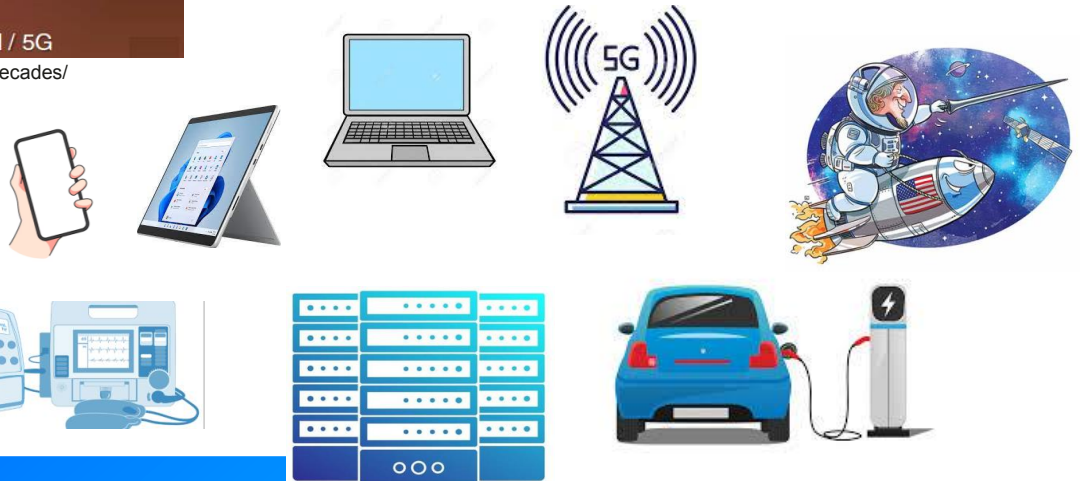
What Drives the 3D Integration?



Pictures Source: https://www.nextplatform.com/2019/09/13/tsmc-thinks-it-can-uphold-moores-law-for-decades/

3D IC

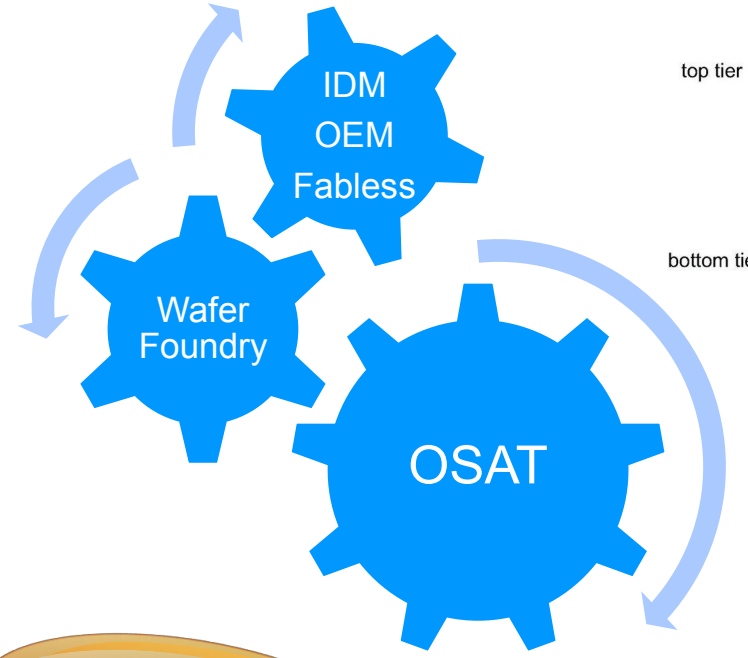


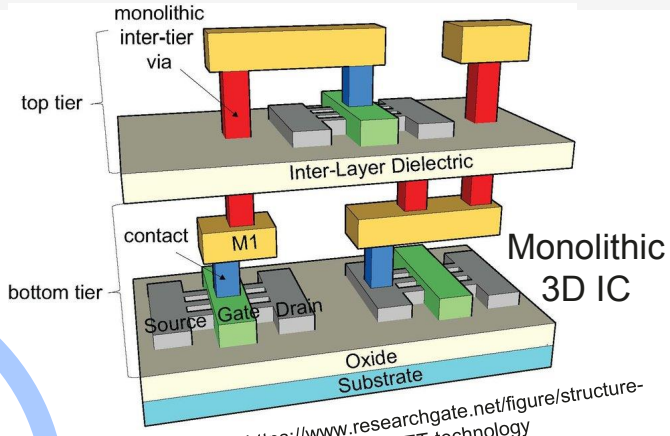


3D Market Drivers:

- Consumer: mobile & gaming devices
- High-end Computing: Servers & Data Centers
- Communications and Telecom
- Automotive: EV
- Military and Aerospace
- Medical devices and Others

Who are the 3D IC Players?

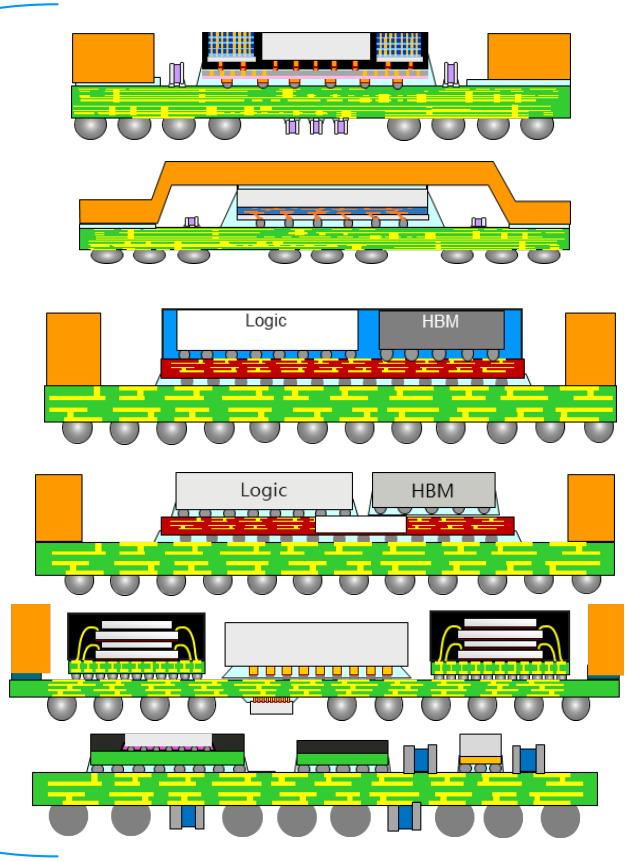




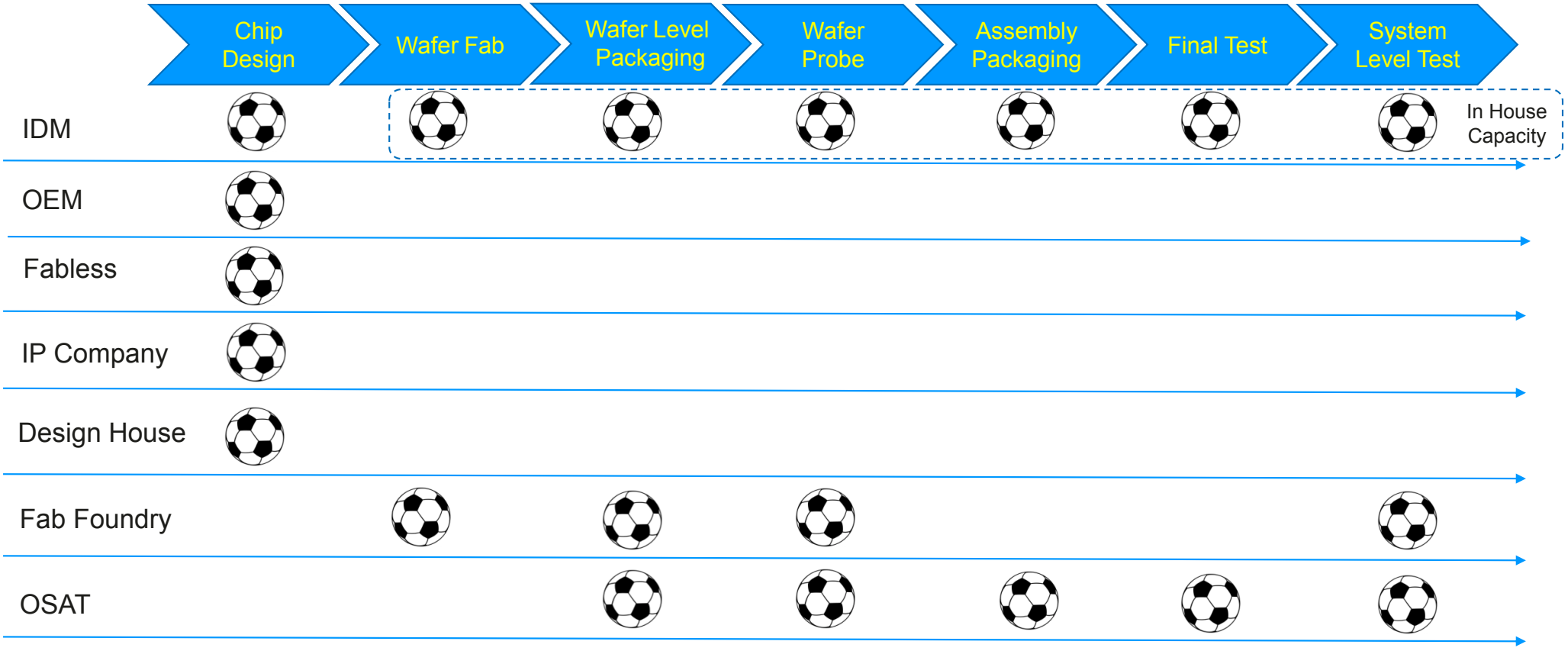
Monolithic 3D IC

Pictures Source: https://www.researchgate.net/figure/structure-of-monolithic-3D-IC-based-on-FinFET-technology

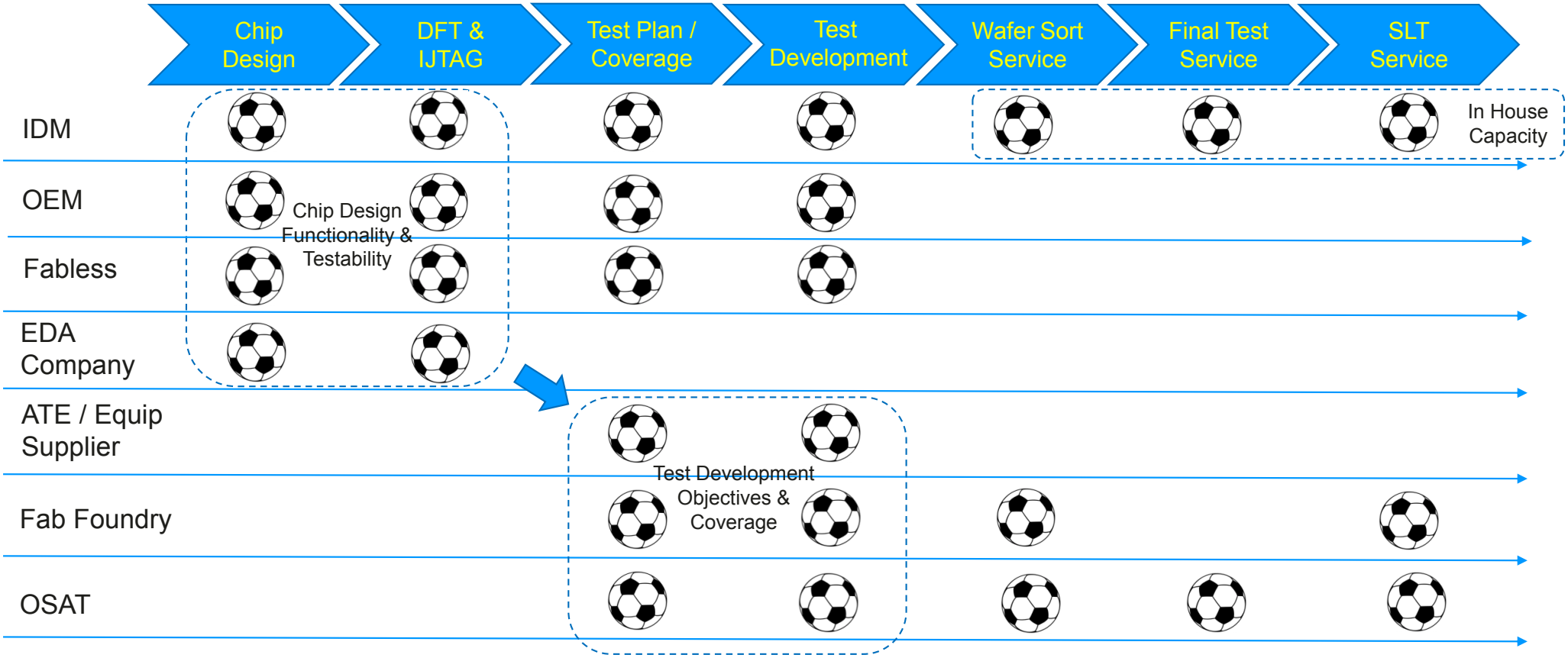
3D IC Packaging



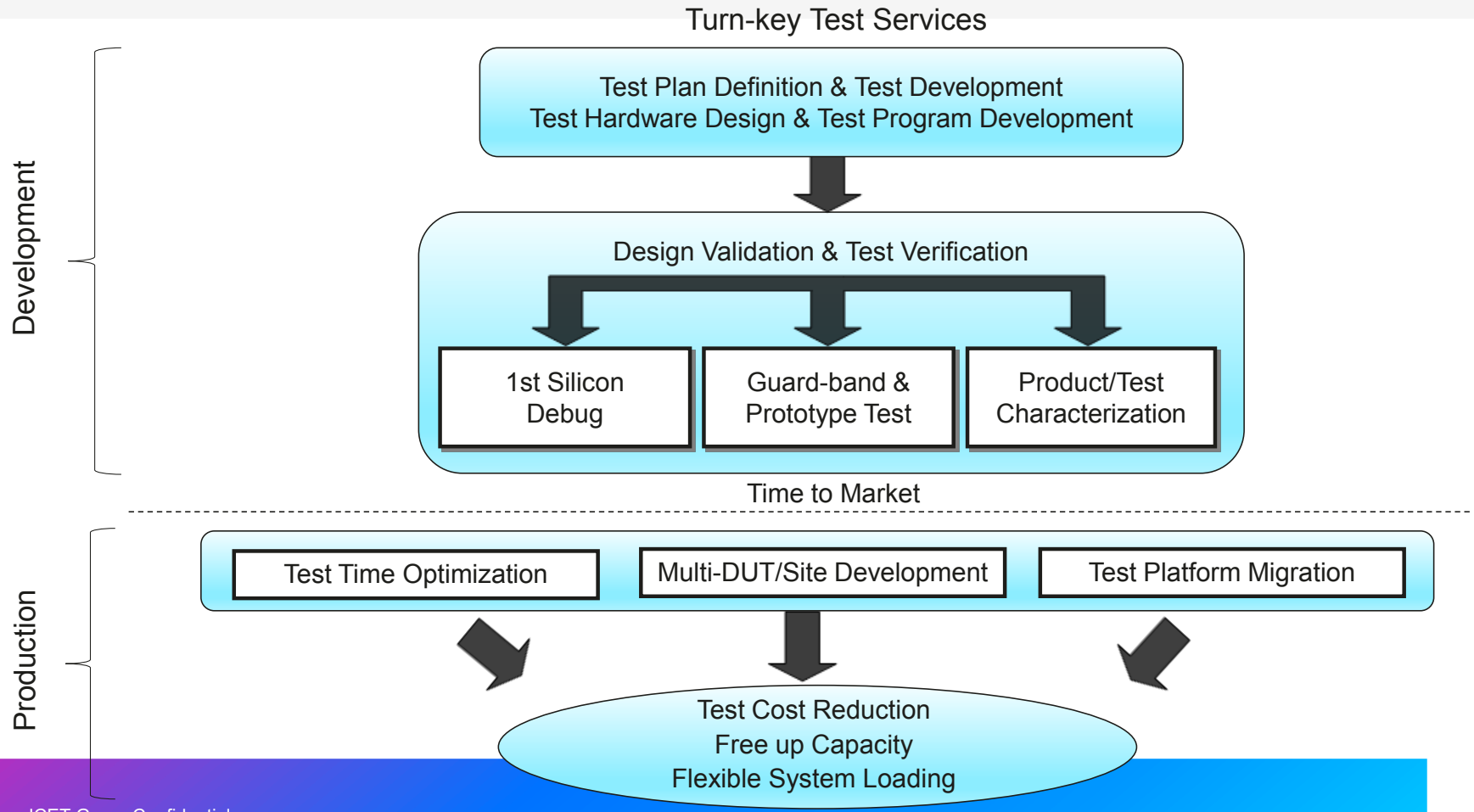
Semiconductor Ecosystem Mapping



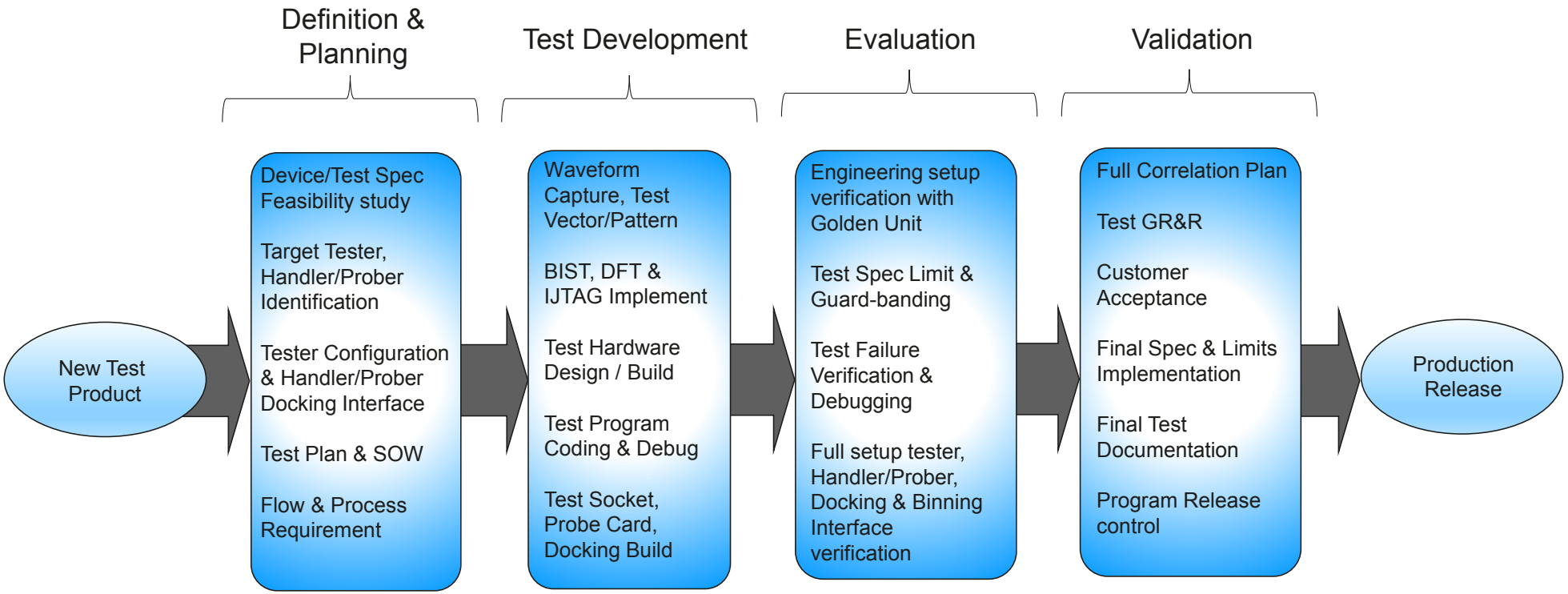
Semiconductor Test Players Mapping



OSAT: IC Packaging & Test Turnkey Solution



Test Development & NPI



IC Test Fundamental

Test Plan & SOW

Test Development

Test Hardware

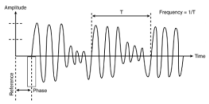
Test Program

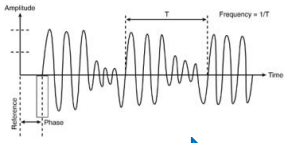
ATE
(Automatic Test
Equipment)

Test
Main Frame

Test
Head

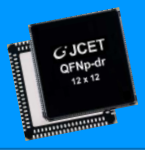
Test Correlation to validate
Test Setup





Test Stimulus

DUT
(Device Under Test)



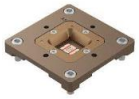
Test Response

Test Program

Test List

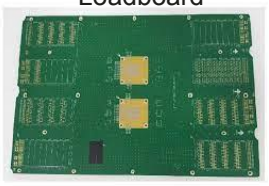
Test
Failure

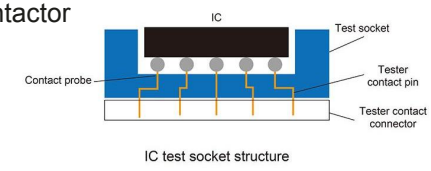
Test List	Test Failure
Open/Short	Bin 5
DC Parametric Test	Bin 6
IDD	Bin 7
Functional Test	Bin 8
AC Parametric Test	Bin 8
Bin 1	Test Pass



Socket /
Contactor

Loadboard



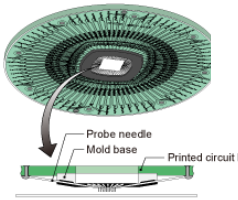


IC test socket structure

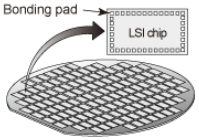
Handler

Prober

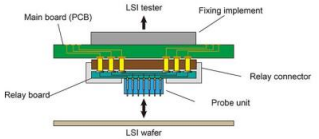
Probe Card



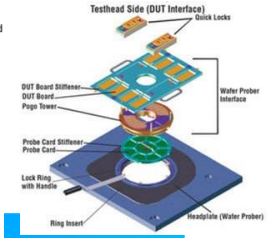
Wafer



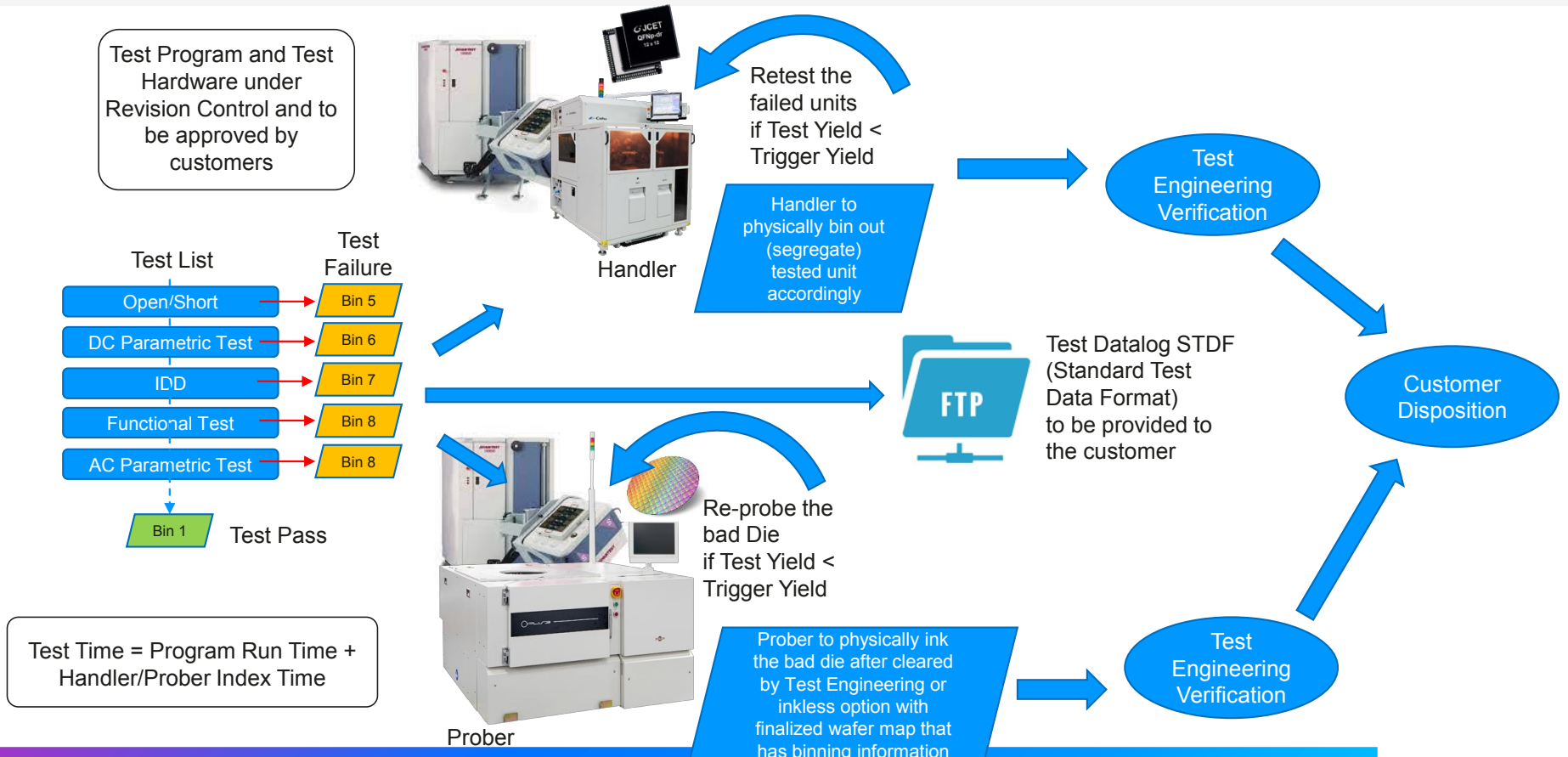
Wafer



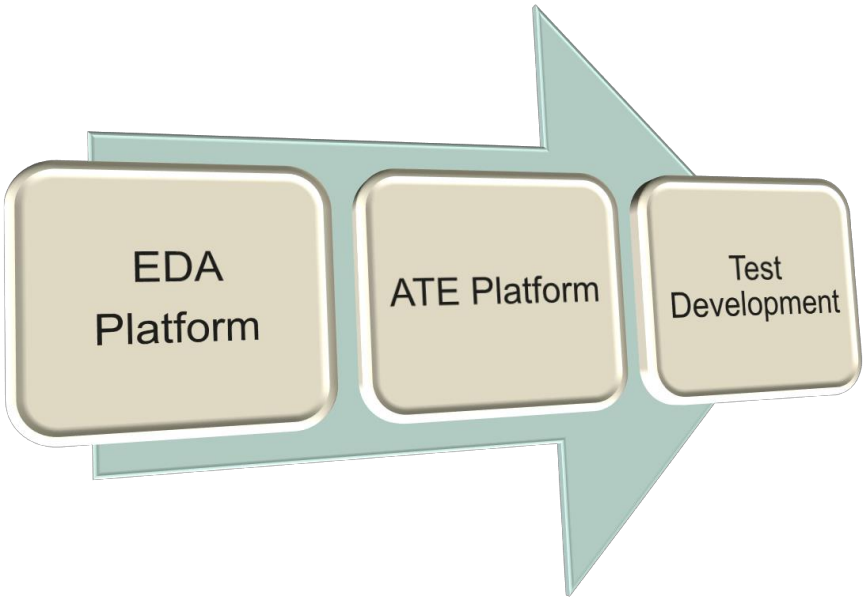
Probe card structure

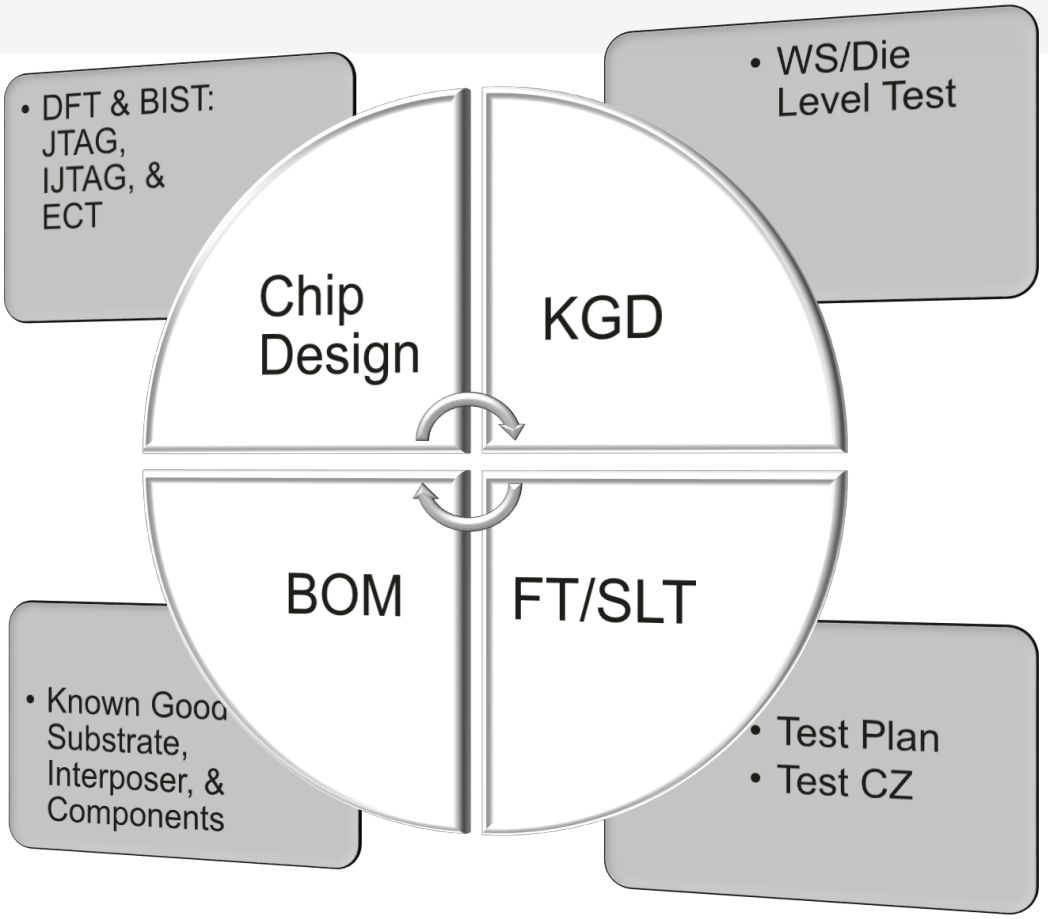


IC Test Manufacturing

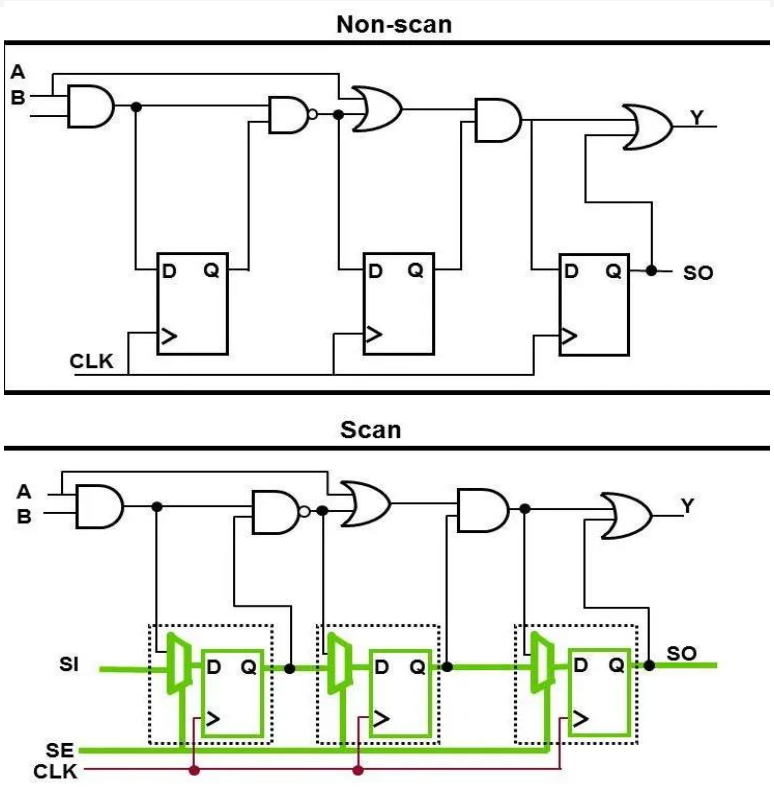


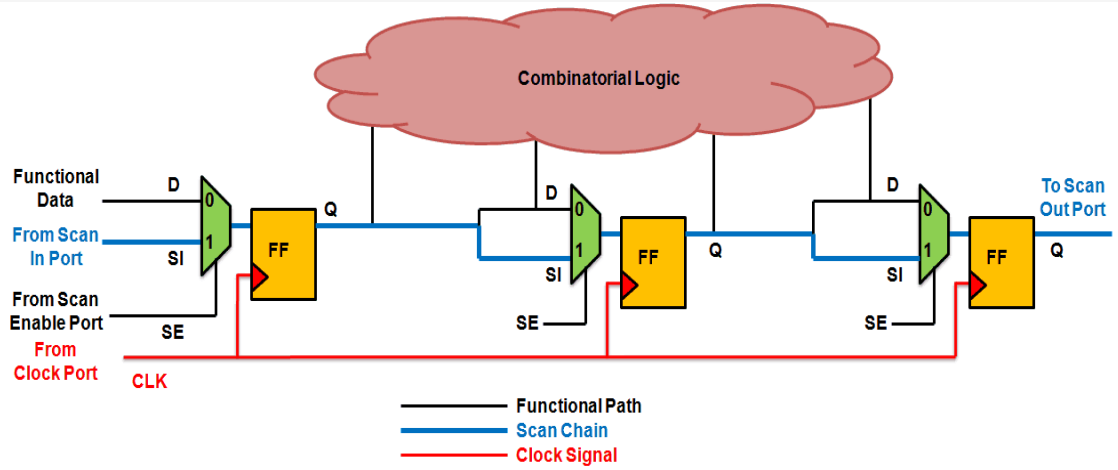
3D IC Testing

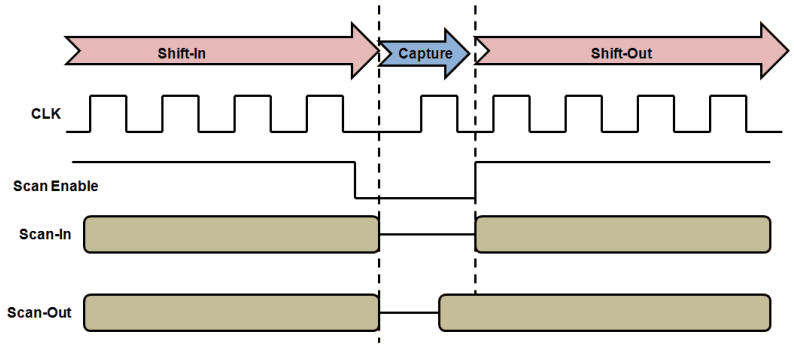




Scan Test



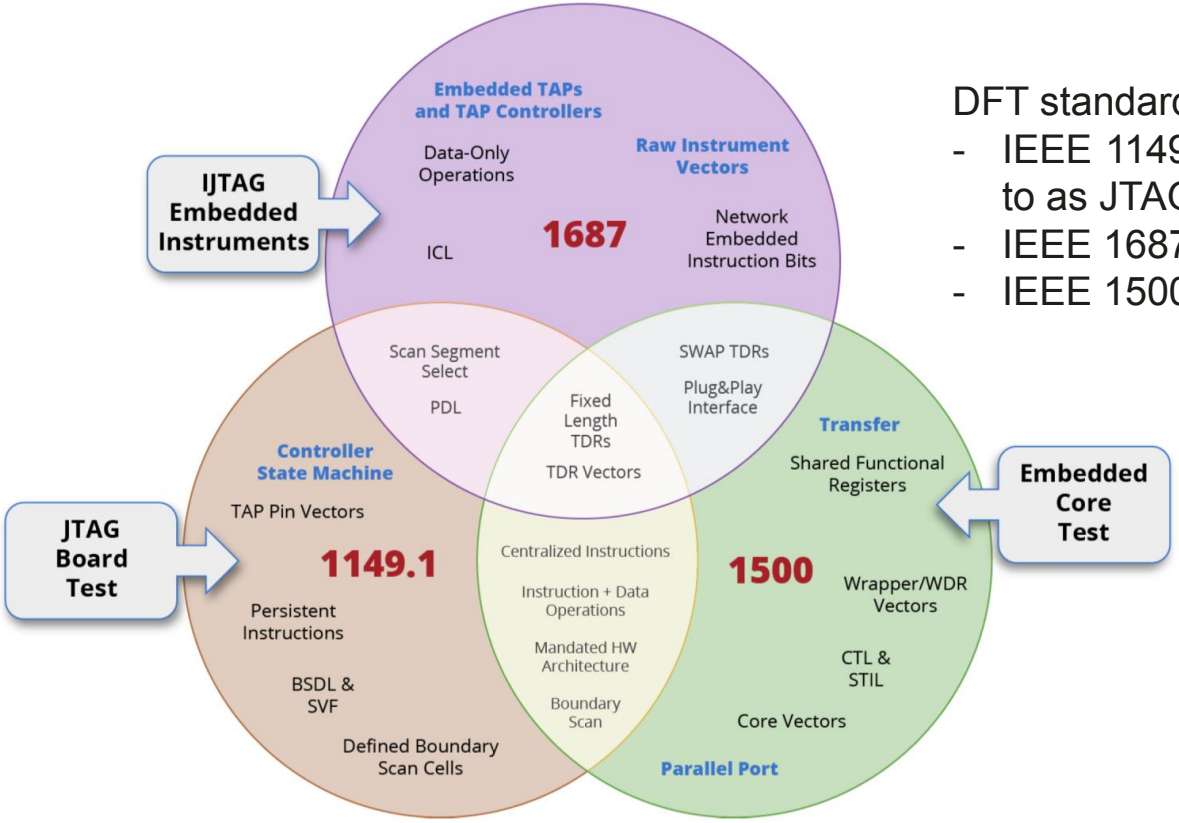




Source: Scan Test - Semiconductor Engineering (semiengineering.com)

Source: Introduction to Chip Scan Chain Testing (anysilicon.com)

DFT Standards



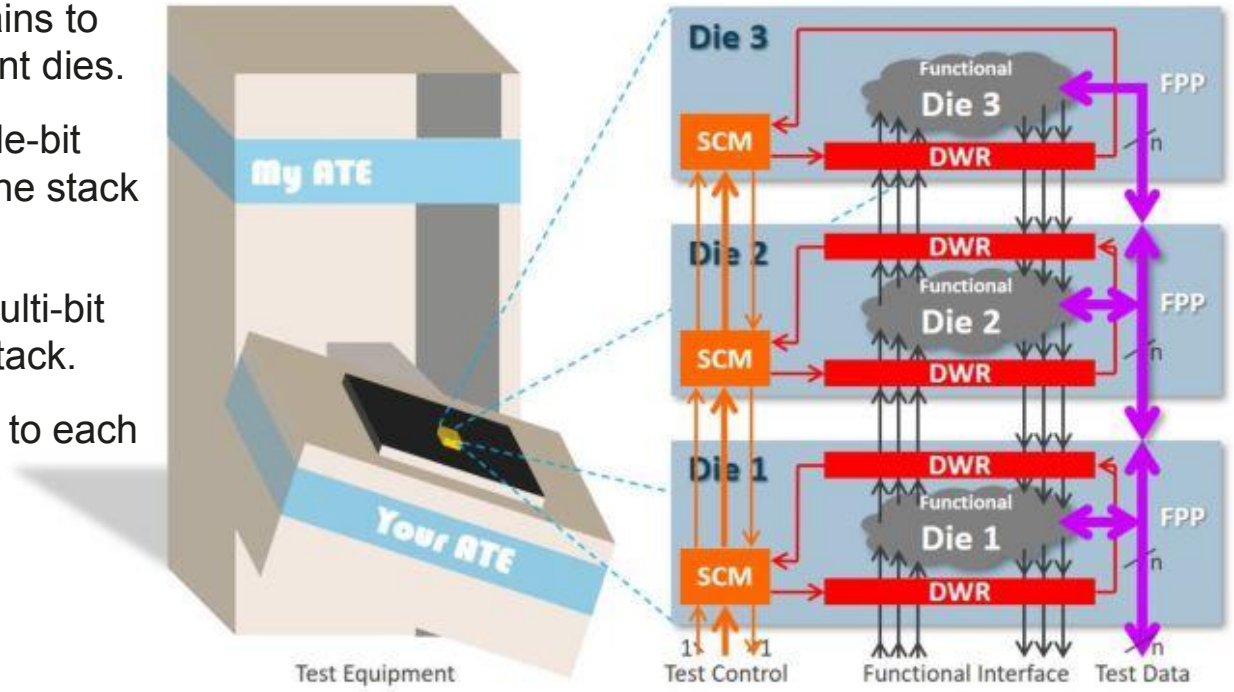
DFT standards:

- IEEE 1149.1 Boundary Scan, often simply referred to as JTAG (Joint Test Action Group)
- IEEE 1687-2014 IJTAG (Internal JTAG)
- IEEE 1500-2005 ECT (Embedded Core Test)

Source: IJTAG VS JTAG VS IEEE 1500 ECT | Technical Tutorial by Al Crouch, Vice-Chairman of the IEEE 1687 IJTAG Working Group

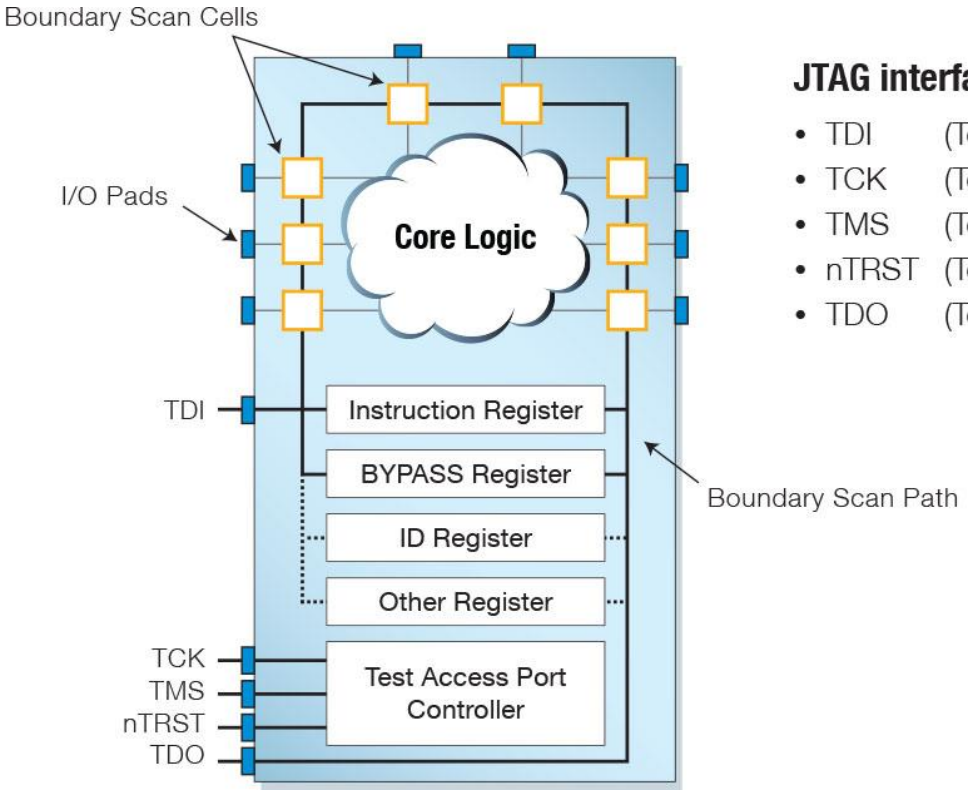
IEEE 1838 for 3D IC Stack

- ✓Stack-Level Test Access Architecture.
- ✓DWR (Die Wrapper Register): scan chains to enable modular testing between adjacent dies.
- ✓SCM (Serial Control Mechanism): single-bit test control to transport instructions to the stack test modes at various DWR.
- ✓FPP (Flexible Parallel Port): scalable multi-bit test access mechanism to access die stack.
- ✓3D IC Stack Integrator: enables access to each layer in the stack.



Source: https://www.eetimes.com/ieee-1838-allows-test-access-to-every-die-in-3d-ic-stack/

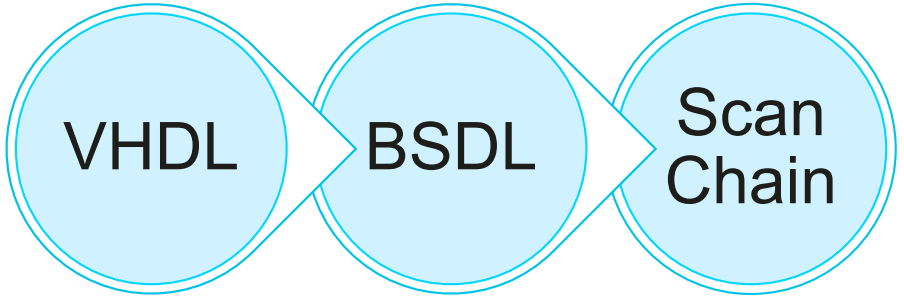
Boundary Scan Description Language



JTAG interface

- TDI (Test Data In)
- TCK (Test Clock)
- TMS (Test Mode Select)
- nTRST (Test Reset - optional)
- TDO (Test Data Out)

Boundary Scan Description Language (BSDL) has been established in JTAG since 1990.



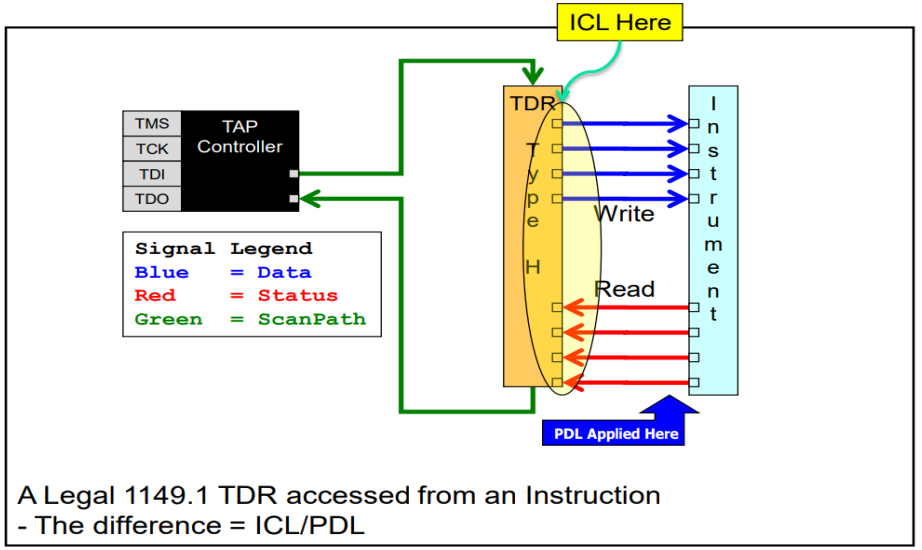
Source: https://www.xjtag.com/about-jtag/bsdl-files/bsdl-and-svf-file-formats/

IJTAG Description Languages

IEEE P1687 IJTAG Standards:
- Instrument Connectivity Language (ICL)
- Procedural Description Language (PDL).

ICL
- Describes the IJTAG hardware architecture on a chip, scan paths, and the instruction registers associated with each scan path.
- SIB (Segment Insertion Bit) to activate or deactivate segments of scan path.

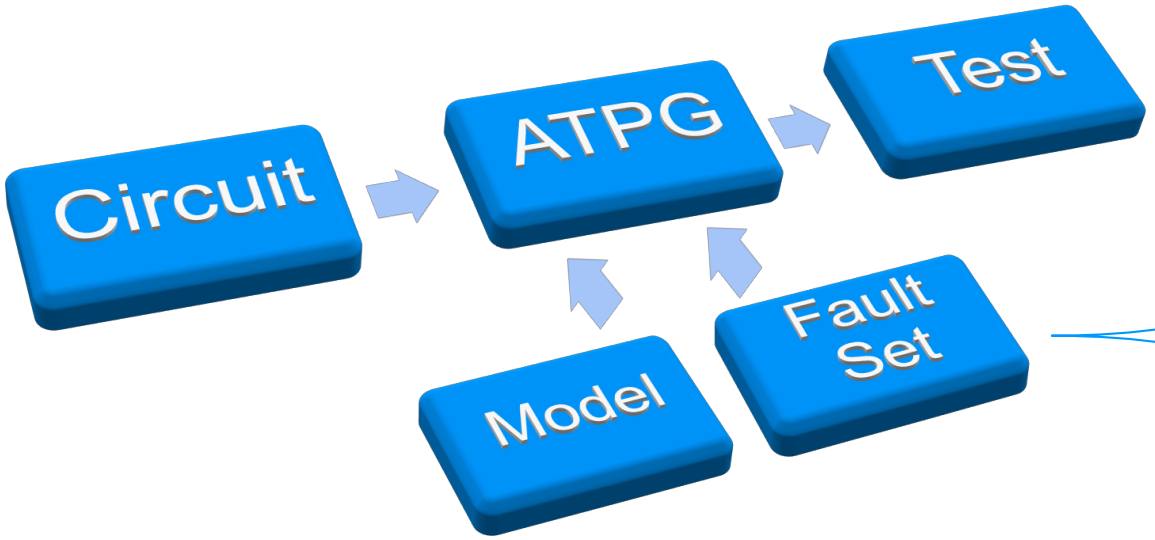
PDL
- Defines instrument's operations and functions that turns into test vectors associated with each IJTAG instrument embedded on a device.



A Legal 1149.1 TDR accessed from an Instruction
- The difference = ICL/PDL

Source: https://www.circuitnet.com/news/uploads/2/IJTAG_Tutorial_FINAL_circuitnet.pdf/

Automatic Test Pattern Generation (ATPG)

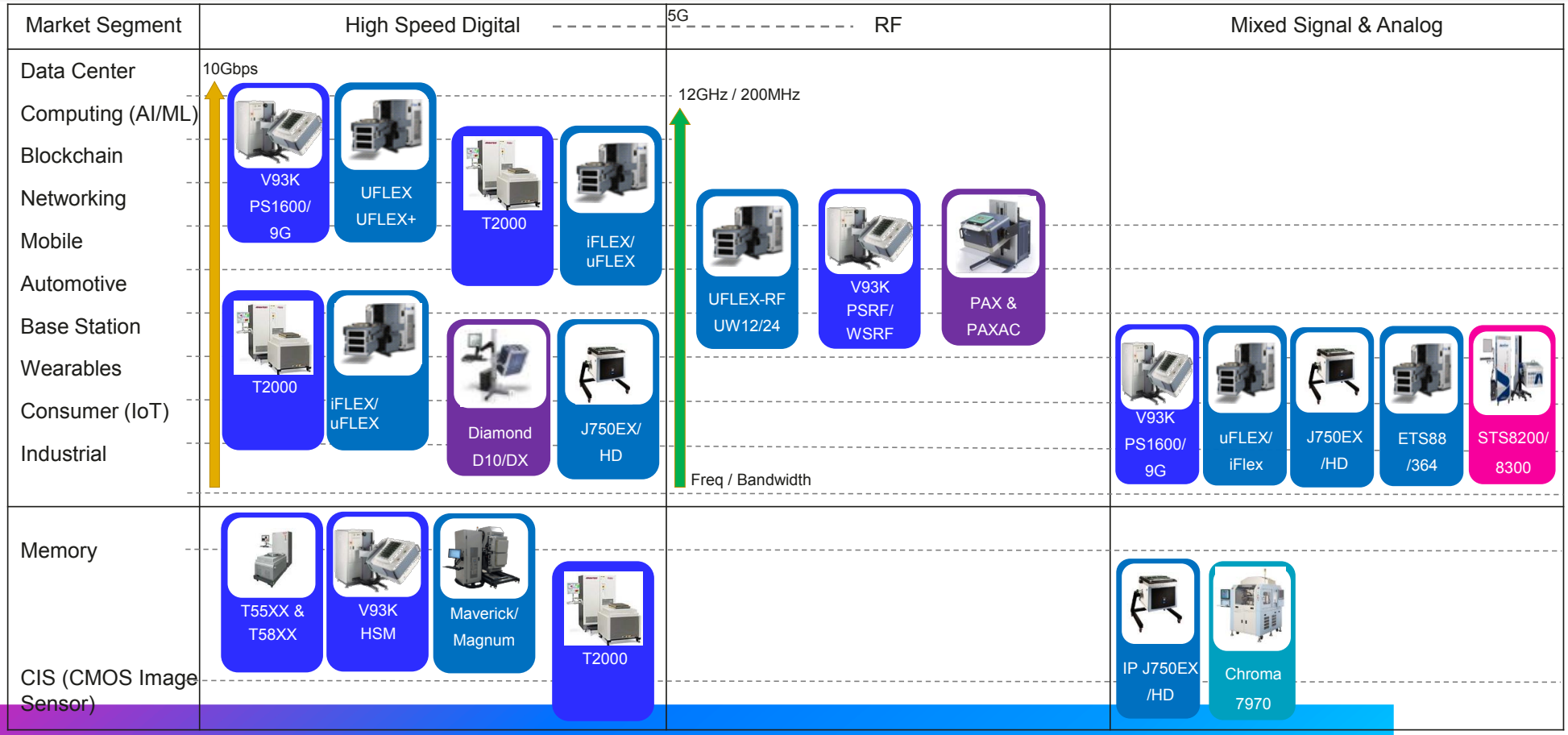


- Functional Defects : Stuck-at Fault Model
- Current Defects : Pseudo Stuck-at Fault Model (IDDQ)
- Speed Defects: At-speed Fault Model, Path Delay Fault Model

- ATPG Effectiveness: Modeled defects, Faults detection, and Patterns size.
- ATPG Efficiency: Full Scan, Synchronous Sequential, or Asynchronous Sequential, Level of Abstraction to represent gate, register-transfer, switch, and Test Quality.

Source: https://semiengineering.com/knowledge_centers/test/automatic-test-pattern-generation/

ATE Platform Selection



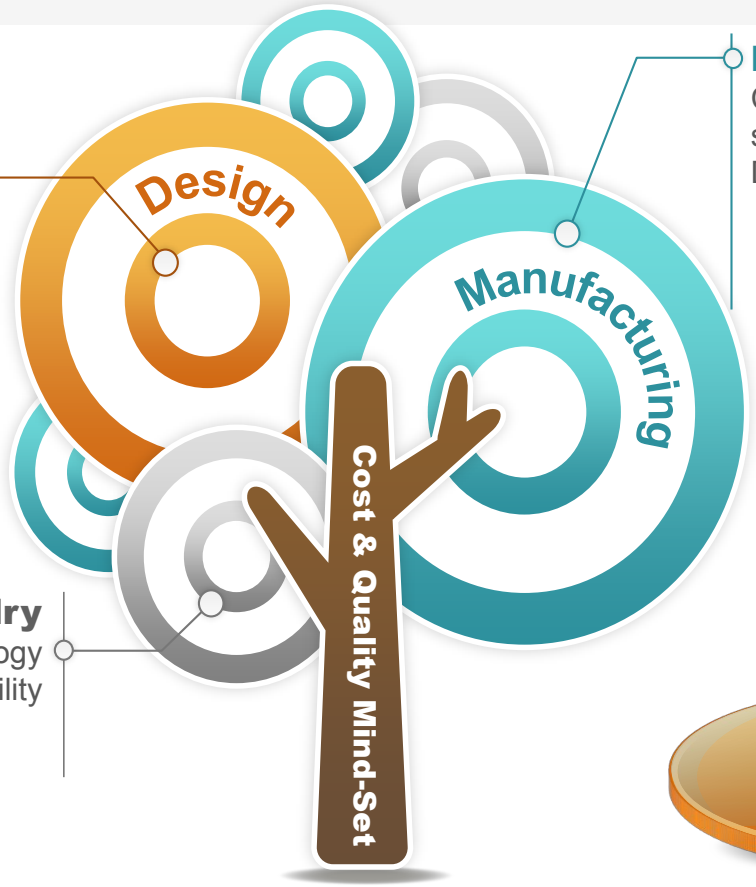
Prober and Handler Selection

Handler	P&P (Pick & Place)	Temperature	TriTemp		Extended Tri Temp		
		Multi-Site	x16 Site		x32 Site		
		Package Size	2x2mm ~ 80x80mm		~110x110mm	1.5x1.5mm ~ 110x110mm	
		ATC (advanced thermal control)	1000W	2000W	2200W	2500W	
	Gravity	Temperature	-55'C ~175'C				
		Multi-Site / Package	x4 Site				
	Turret / Rotary	Temperature	Room				
		Multi-Site / Package	x8 Site / 1.0x0.6 ~ 12x12)				
	SLT (System Level Test)	Package Size	5x5mm ~ 45x45mm		3x3mm ~ 90x90mm		
		Multi-Site	x16 Site		x128 Site		
Prober	Pogo Tower	Temperature	TriTemp				
		Die Thickness	>225um		>55um		
	Direct Dock	Temperature	TriTemp		Extended TriTemp		
		Die Thickness	>180um		> 55um & new enhanced probers		
		Year	Y2021	Y2022	Y2023	Y2024	Y2025

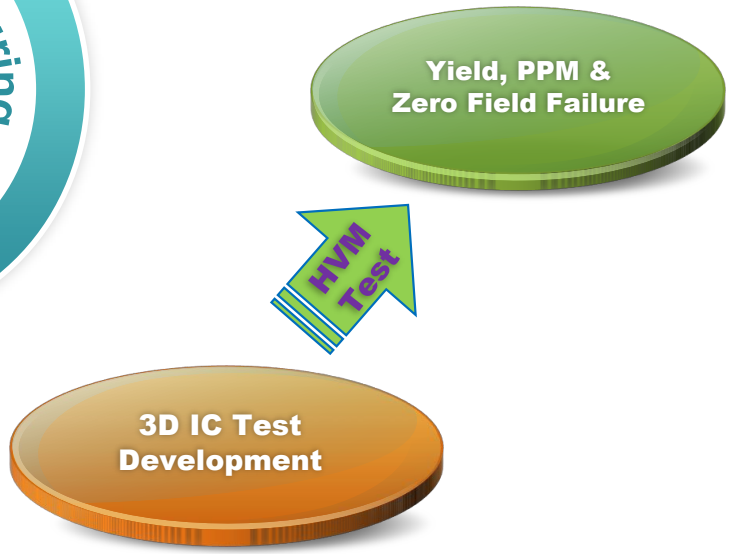
3D IC Test Strategy

EDA Platform Selection
IEEE 1149.1 Boundary Scan, JTAG
IEEE 1687-2014 IJTAG (Internal JTAG)
IEEE 1500-2005 ECT (Embedded Core Test)

Fab Foundry
Node Technology
TSV, uBump Capability



Manufacturing
Collaborate with OSAT for Turnkey solution: 3D IC Heterogeneous Package Design, Test Development, and HVM



Takeaway Conclusion

- ✓ 3D IC as the new format of microelectronics scale integration will continue to scale up as predicted in Moore's law.
- ✓ DFT at various standards is the DIRFT (Do It Right the First Time) strategy at the chip design stage.
- ✓ OSAT offers the 3D IC turnkey solution: diversified multidimensional heterogeneous Packaging and Test at the right ATE platform with a mutually defined Test Plan and SoW (Statement of Work).
- ✓ 3D IC Test Strategy is a cross-functional engineering program that involves multiple roles of Design, DFT, Packaging, Test Development, Product/Test, and Supply Chain Management.
- ✓ Semiconductor Industrial Community Collaboration for 3D IC Test Ecosystem is significantly required.

Thank You!

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