Not Just Chips

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The Challenges of Scaling Beyond Moore's Law and Into the World of 3DHI

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Product Director

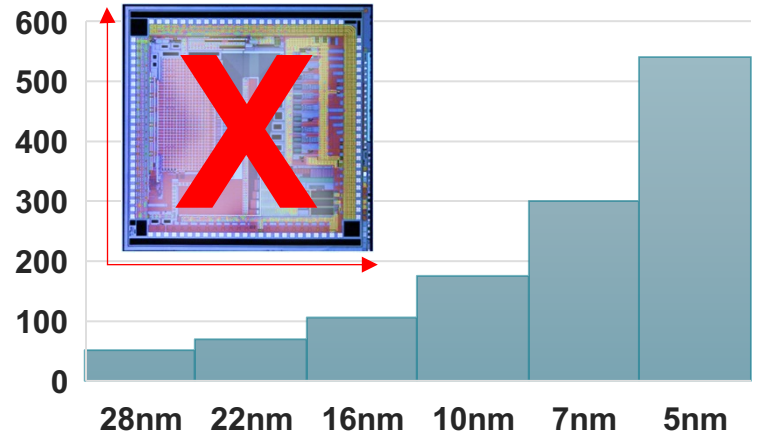
cadence®

Outline

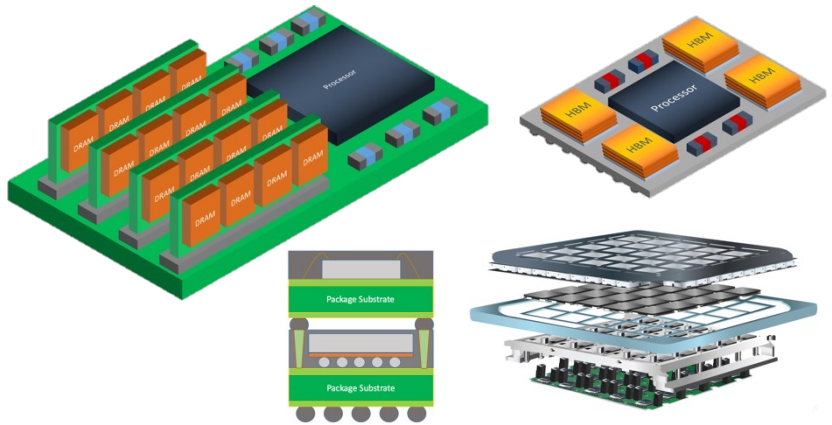
- Trends
- 3D Packaging vs Silicon Stacking
- Conclusion

Simply Following **Moore's Law** Alone is No Longer the Best Technical and Economical Path Forward

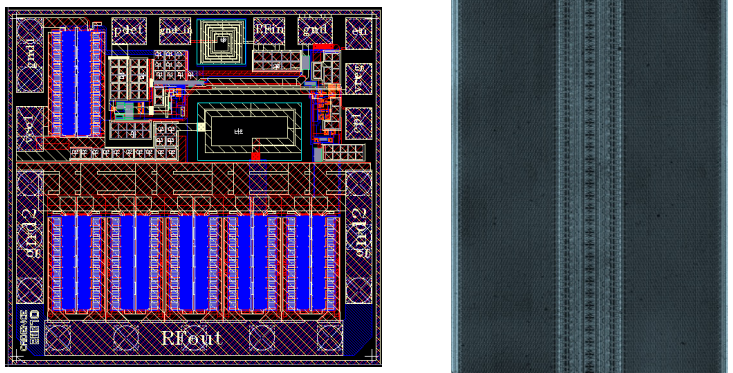
Cost & Yield & Size



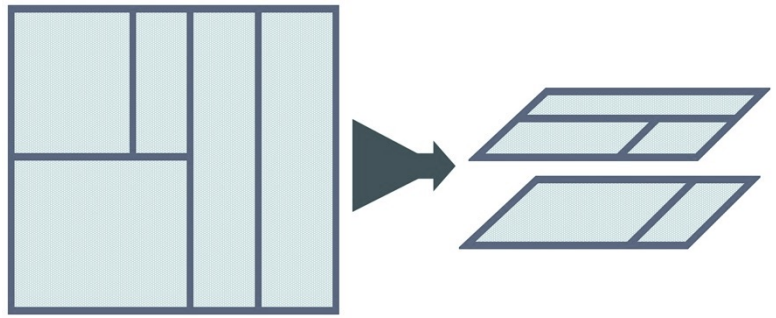
Lowering the Memory Wall



Analog/RF, I/O & Memory

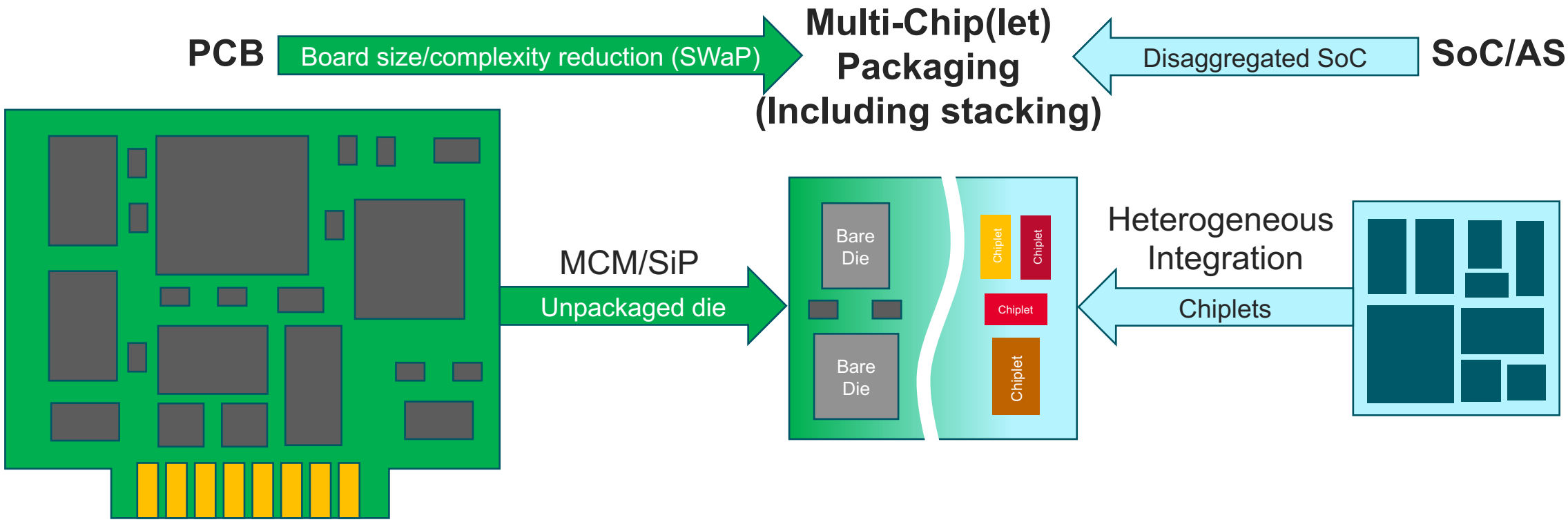


Form-Factor & Modularization



SiP/MCM vs. Heterogeneously Integrated Chiplet-Based Architectures

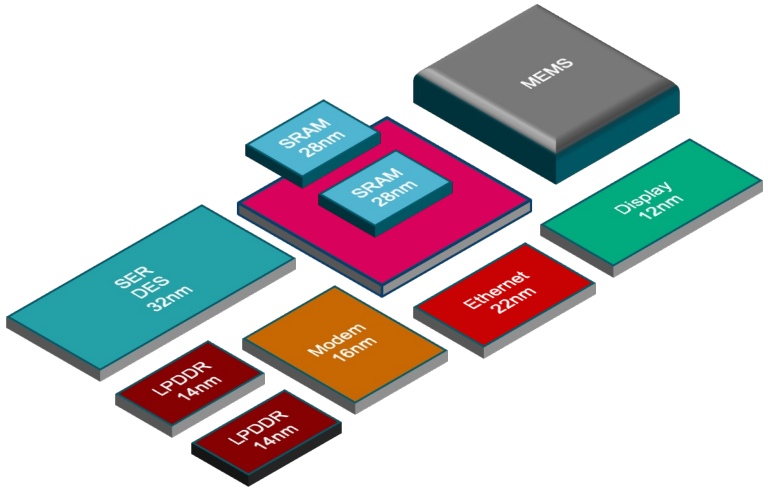
The transition from system on a chip (SoC) to system in a package (SiP)



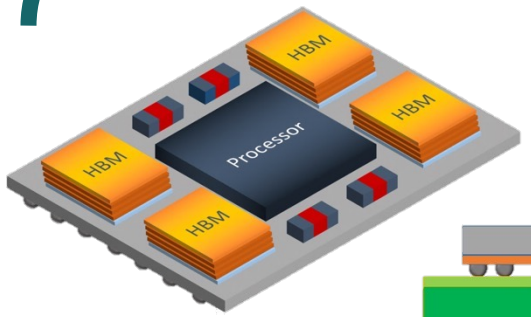
PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

Heterogenous Integration Leverages Multiple Packaging Technologies

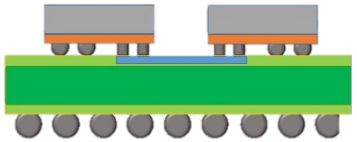


Heterogeneous Integration



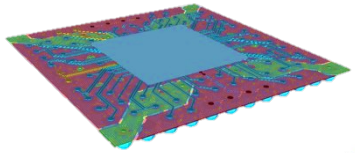
2.5D-IC (Silicon Interposer)

2010



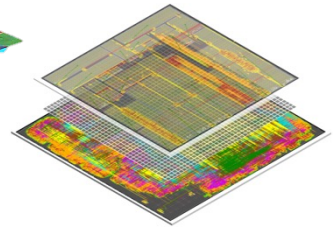
Interconnect Bridges

2012



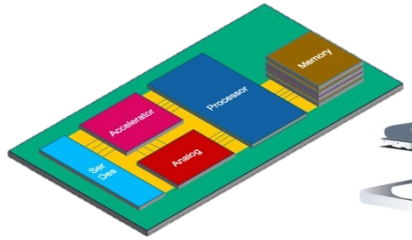
Ultra-High-Density RDL (FOWLP)

2015



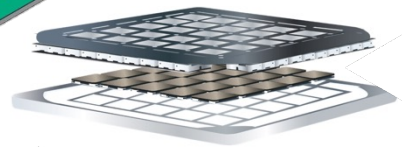
Silicon Stacking

2018

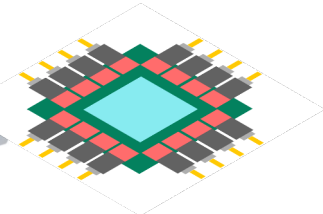


RDL Interposer

2020



3D System-on-a-Wafer



Co-Packaged Optics

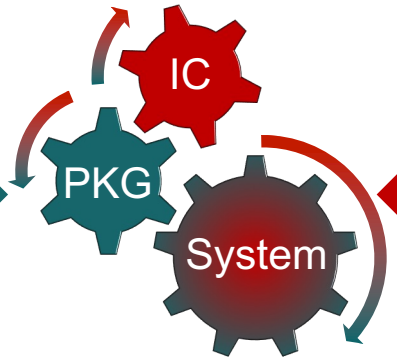
2022

The Needs of IC and Systems Designers are Converging

OSATs (SWaP)

Board design impact on packaging

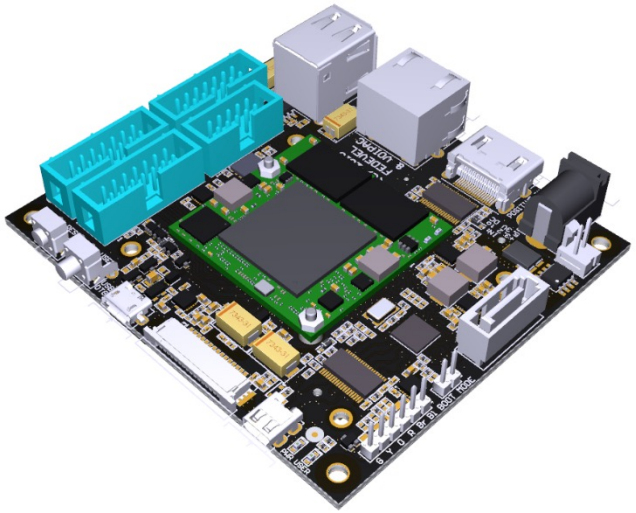
1980-2010



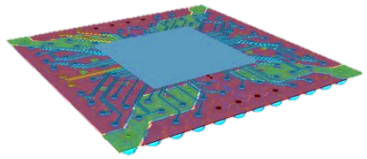
Foundries (PPA)

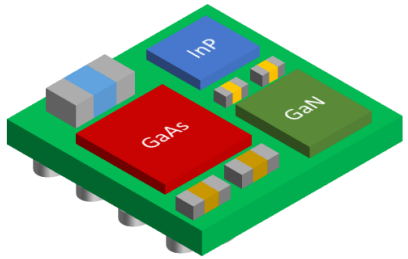
IC design impact on packaging

2011-Now

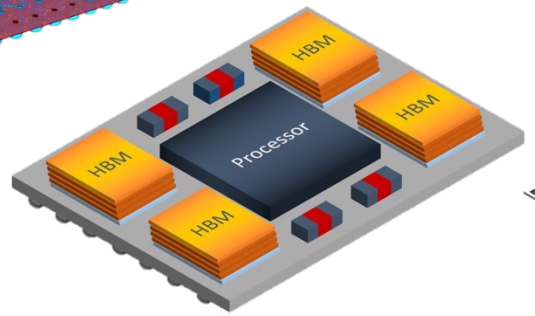


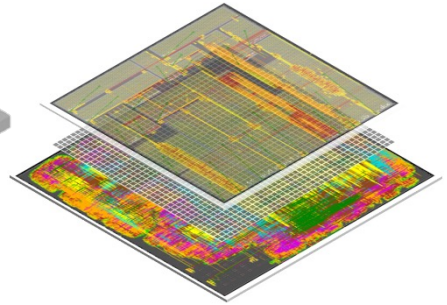
PCB Layout Flow
System-Level Analysis



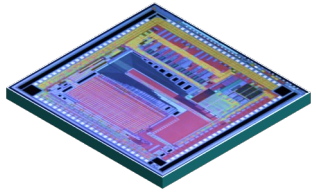


PCB-like Flow
System-Level Analysis



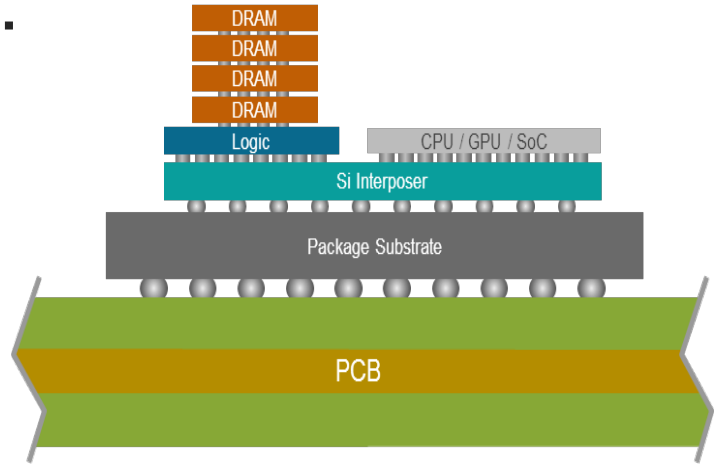


IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis



IC Flow
IC signoff Methodology

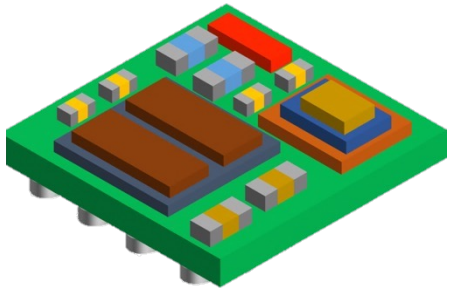
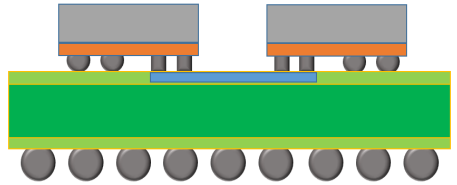
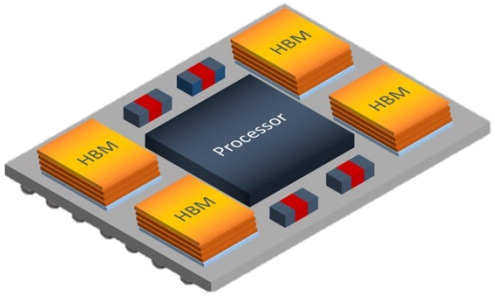
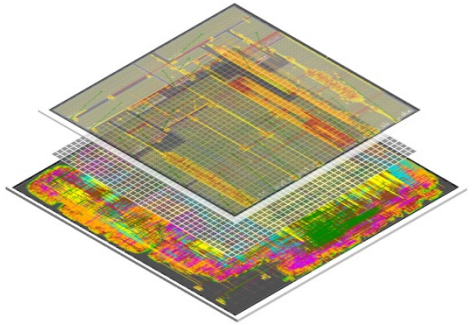
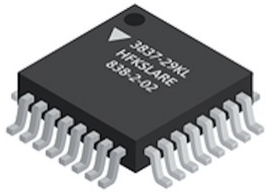
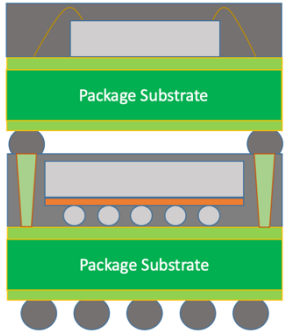
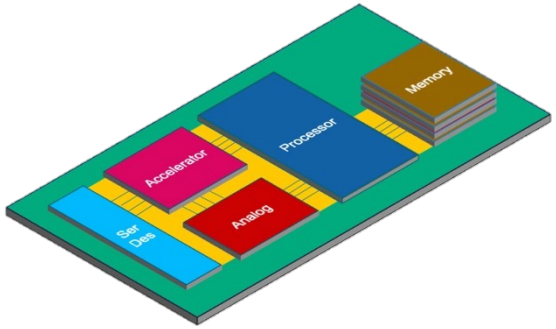
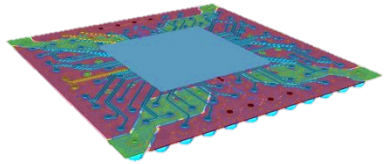
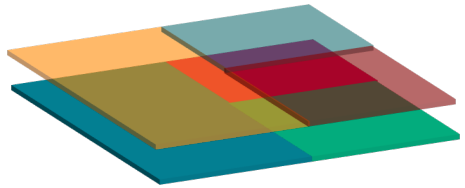
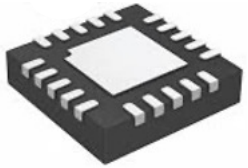
Things Have Changed For The Better…



- Yesterdays advanced IC packaging was often considered a *necessary evil*
  - Avoid negative impact on chip
    - Electrical, Thermal
  - Protect chip from the outside world
  - Redistribute IO to pitch more suitable for the PCB layout

- Todays advanced IC packaging is about *adding value* to end products
  - Multi-chip(let) solutions leading the way for “More than Moore” vision
  - Companies leveraging packaging technologies to create value and differentiation from their competitors
  - TSV, WLP and 3D stacking technologies providing a tremendous number of packaging options for all form-factors and budgets

Silicon Stacking
The Next IC Packaging Paradigm Change is Here…

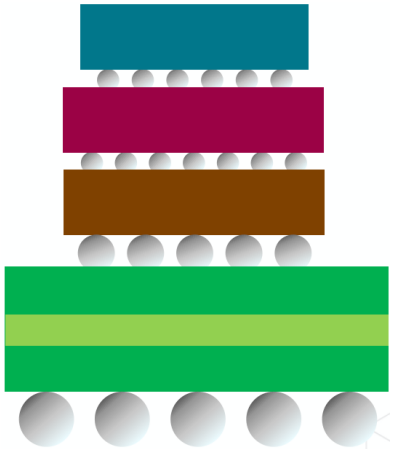
Mechanical	3D Packaging		Silicon Stacking	
Lead Frame	Laminate BGA Design Flow		Hybrid Design Flow	Die Design Flow
 DIP	 BGA/SiP/MCM	 Interconnect bridges	 Silicon (TSV) interposer	
 QFP	 Package on package (PoP)	 Organic (RDL) interposer	 FOWLP (Ultra-High-Density RDL)	 Bumpless wafer, chip, core, macro stacking
 QFN				

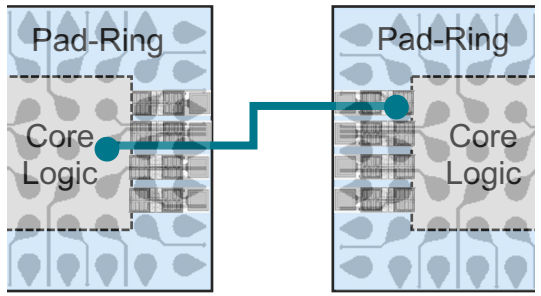
Silicon interposers and 3D chip-stacks mount to BGA/LGA packages

3D Packaging Versus Silicon Stacking (3DHI)

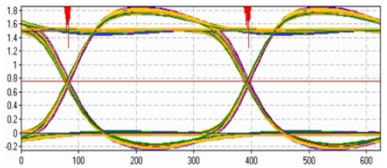
3D Packaging

- Solder-based connections (>25um)
- Each die designed independently
  - Black-box abstracts used for layout
- I/O buffer to I/O buffer signaling



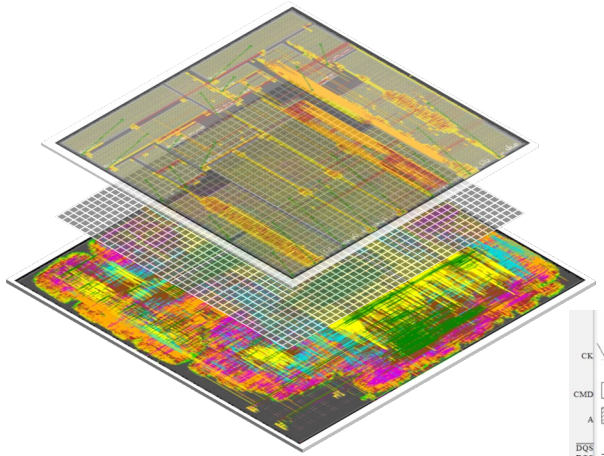


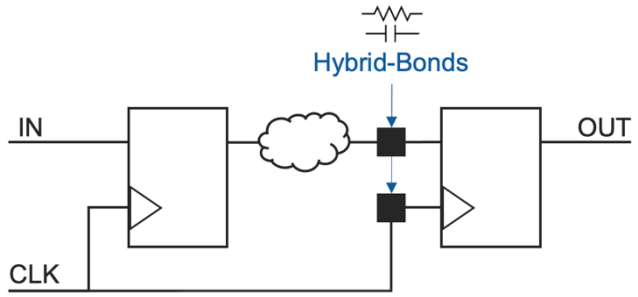
I/O buffer to I/O buffer
(AIB, OpenHBI, BoW, UCIe, etc)



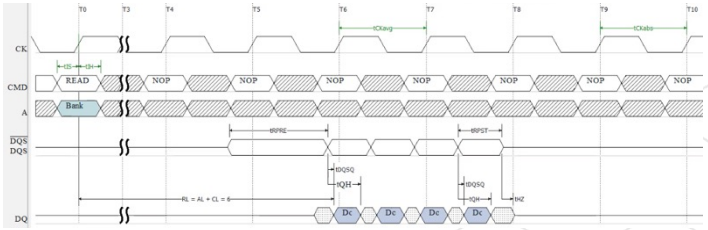
Silicon Stacking

- Solder-free connections (<10um)
- Single RTL partitioned at implementation
  - Full detail of IC required for layout
- DBI, hybrid-bond, cu-to-cu, direct connection

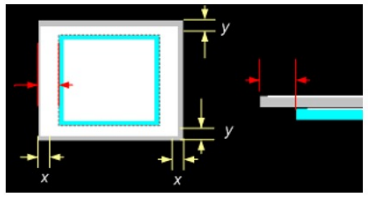




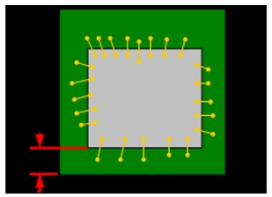
Interconnect through
hybrid bond

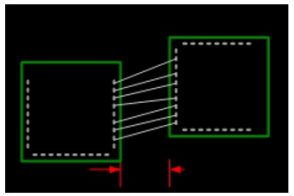


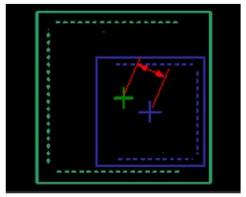
Multi-Chiplet 3D Diverse Ecosystem Challenges

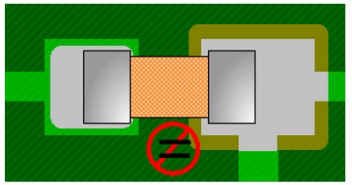


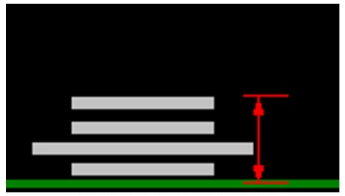
Die/Chiplet Overhang

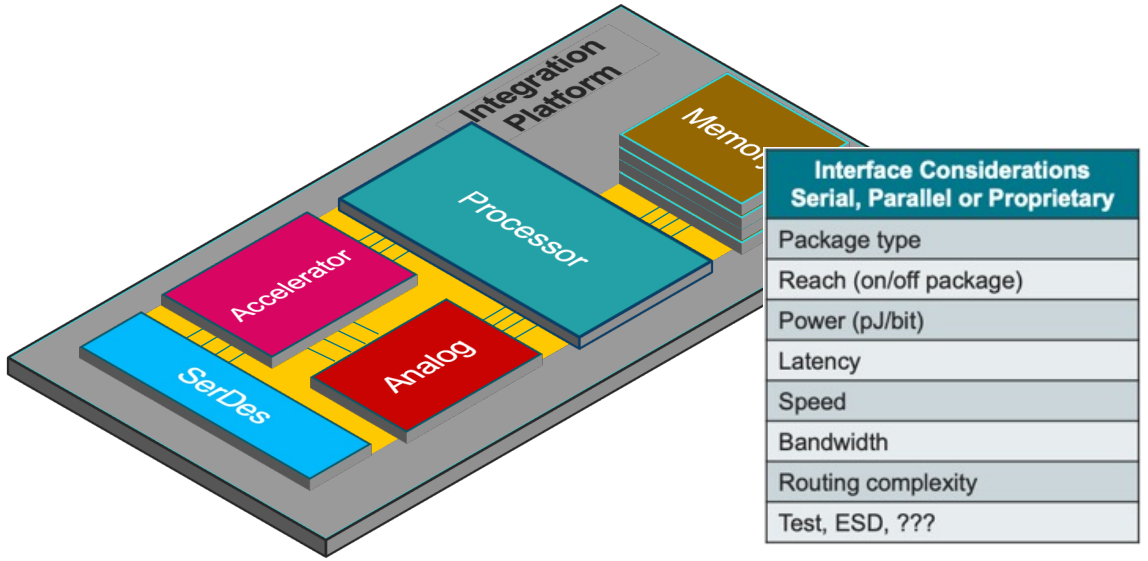

Die/Chiplet Spacing to Substrate Edge


Die/Chiplet to Die/Chiplet Spacing


Die/Chiplet Center to Center Offset


Tombstone Effect (% size diff)


Die/Chiplet Stack Height



Assembly Design Kits

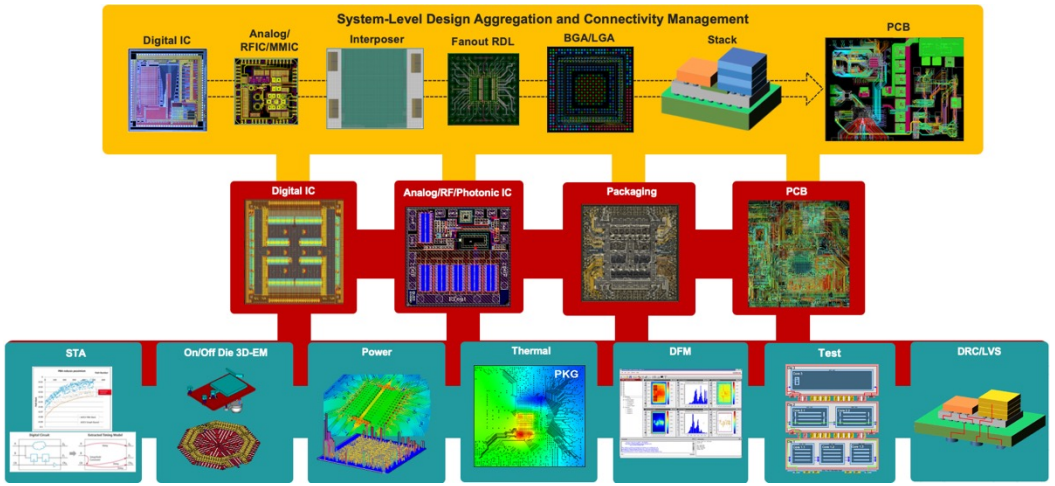
- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
- Foundries need to provide the packaging engineer all the data he/she needs to produce manufacturing output of a design that can be assembled and tested
- Contents; tech files, libraries, assembly rules, substrate DFM, rule decks, and design templates
- Security and Test solutions

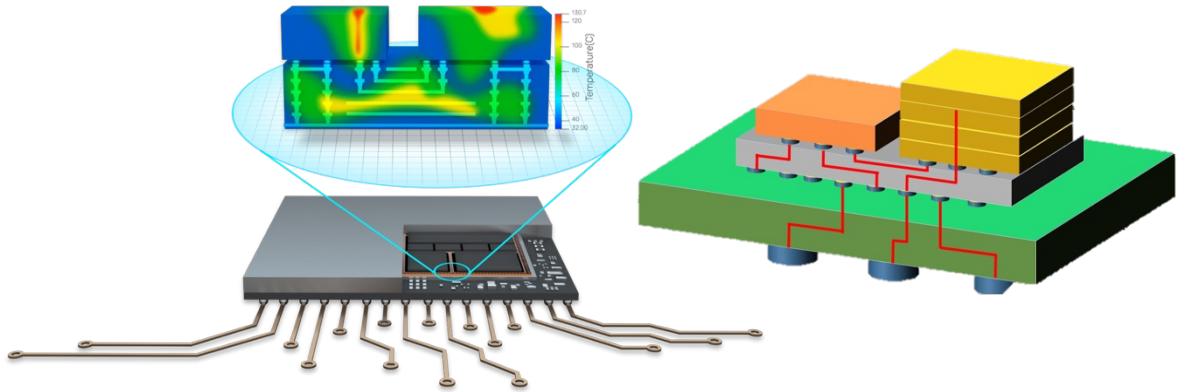
COTS Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
  - CHIPLET.US
- Progress with chiplet exchange formats
  - CDX, 3Dblox™
- Common communication interface
  - AIB, UCIe, BoW, …
  - Too many packaging options to standardize on a single interface

cadence

Multi-Chiplet 3D Flow Challenges





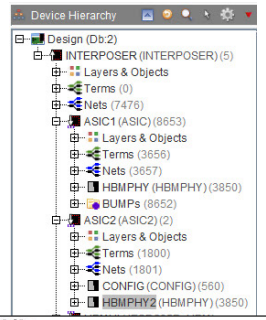
Design Flows

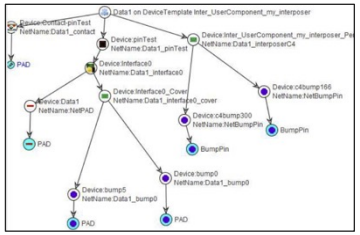
- Explosion in the number of design tools and required expertise mean complex design flows
- **Common cross-domain platform for design aggregation and optimization (co-design)**
- Capacity and performance impact on tools
- Support of existing and emerging 3D-IC standards
- Silicon stacking breaks traditional abstract die representation use model
- Package designers pivoting to foundry-based design and sign-off requirements

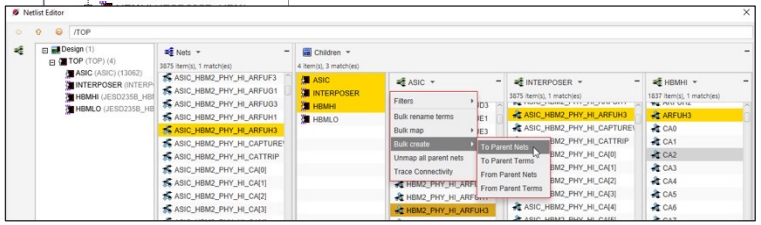
Analysis and Sign-Off

- Early-stage and signoff-level thermal/power analysis
- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Stacked-die EMIR
- Stress and CMP planarity checks
- New 3D-IC test standards
- High-capacity EM/SI/PI to support very large structures (billions of instances)
- Compliance kits for new chiplet-to-chiplet communication standards

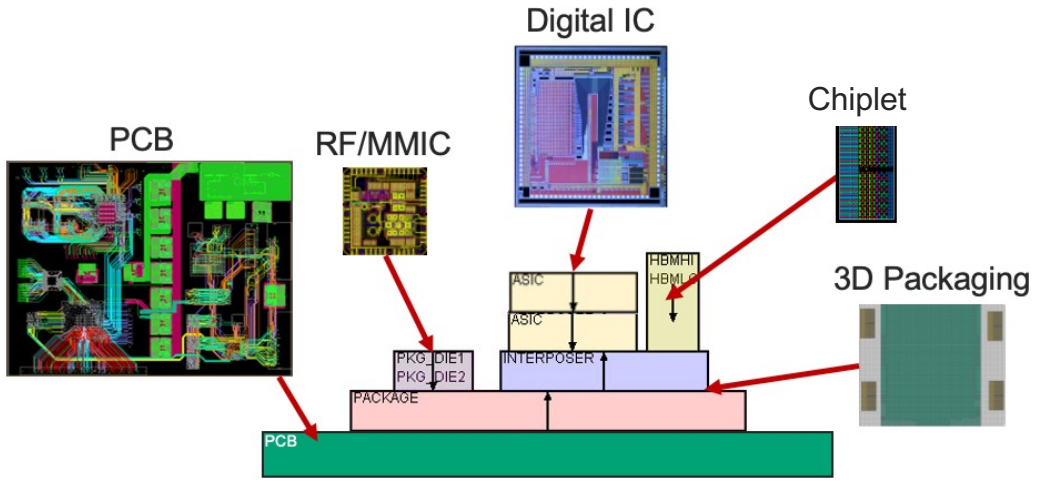
Top-Level Design Aggregation and Optimization



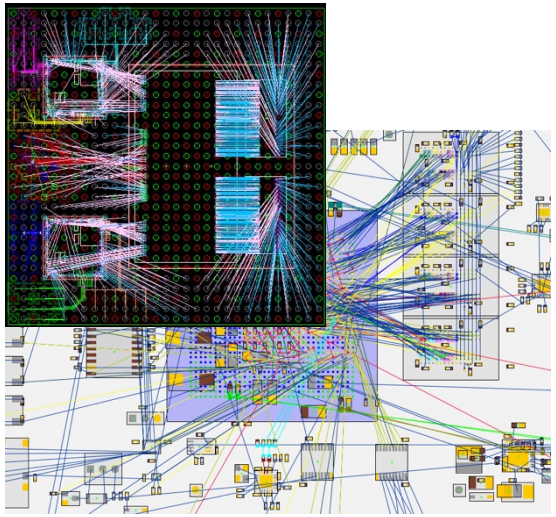




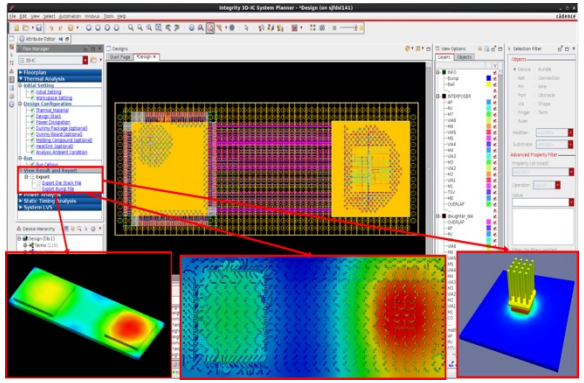
Multi-design management with chip(let)-chip(let)-package-board signal-mapping



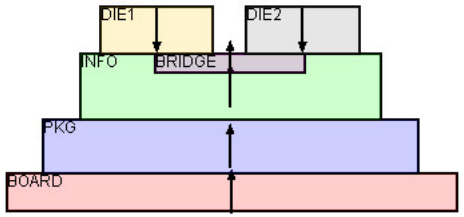
Hierarchical Planning and Optimization of System-Level Design and Connectivity



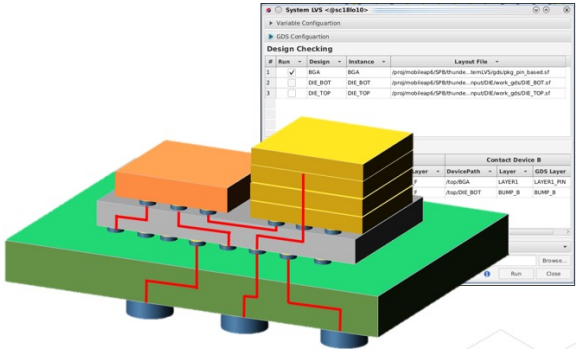
System-level co-optimization



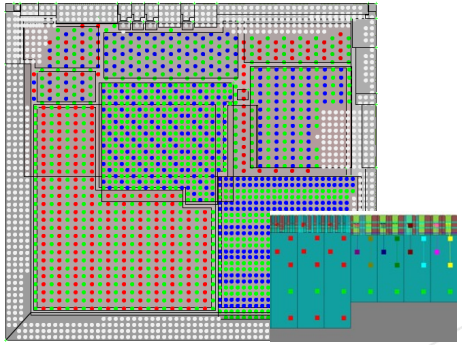
Early-Stage Thermal/Power Analysis



Stack management (Supports 3Dblox™)

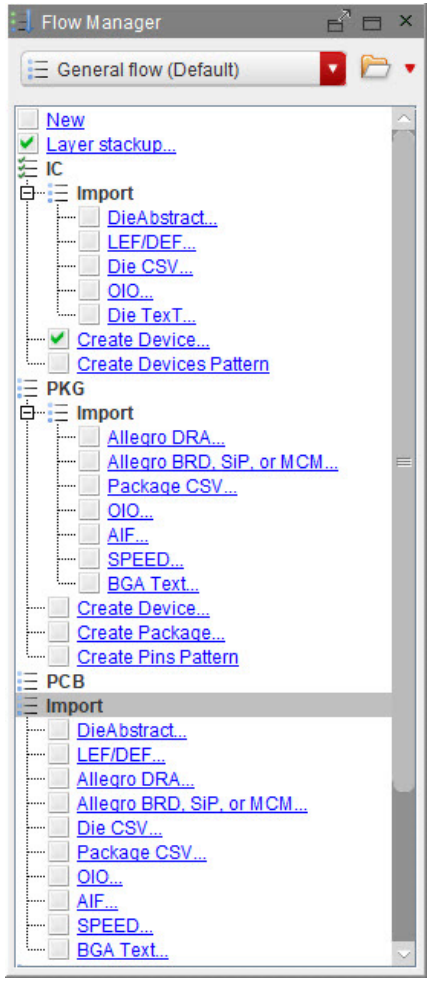


System-level connectivity/stack alignment verification (SystemLVS)

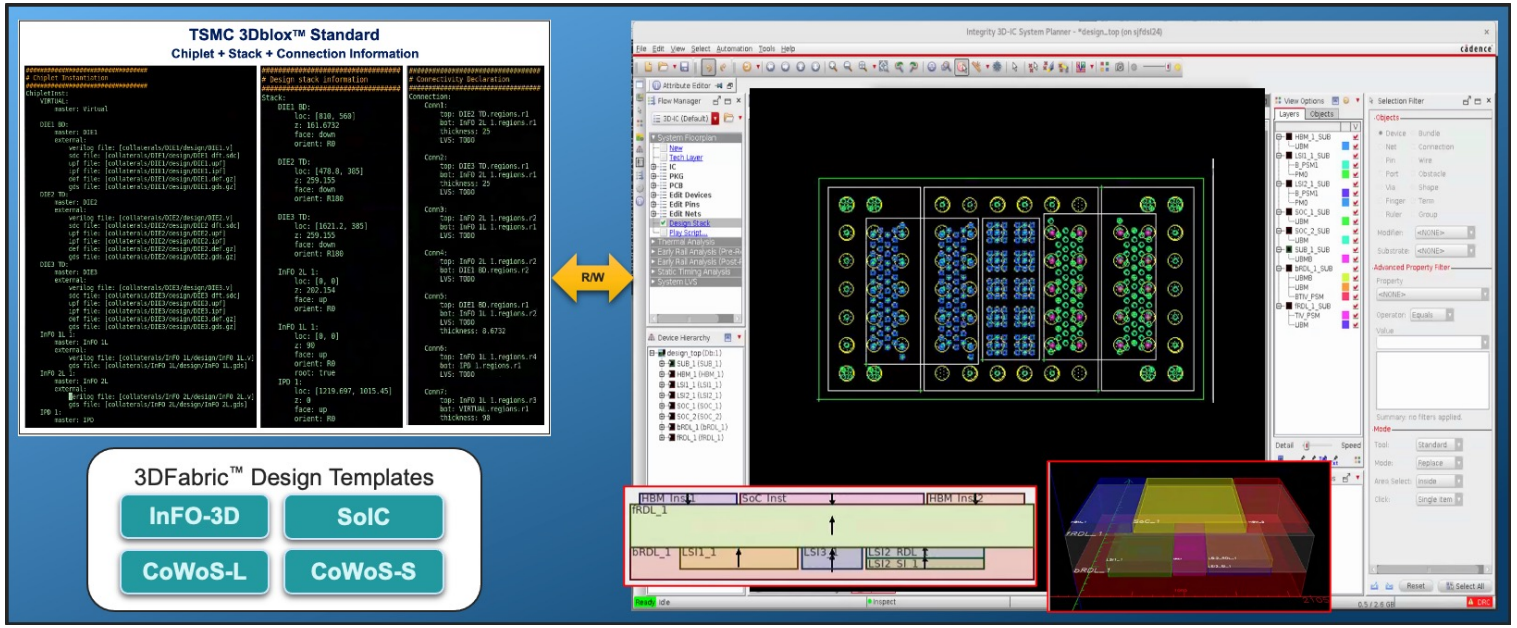


Advanced bump/TSV planning

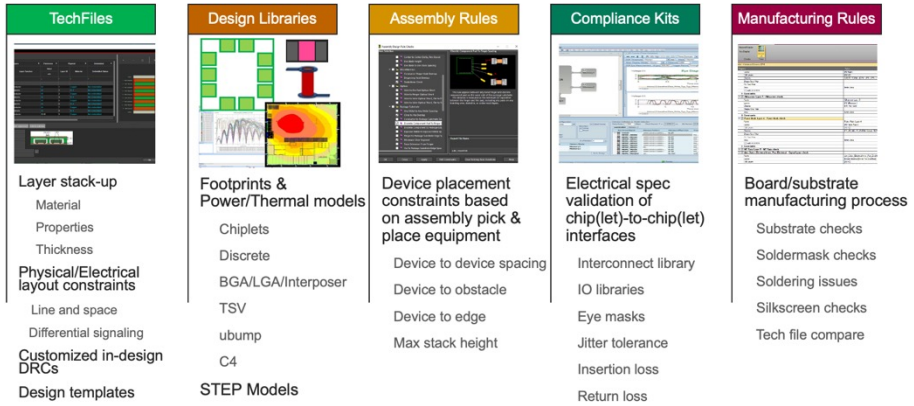
Standards and Co-Design Support



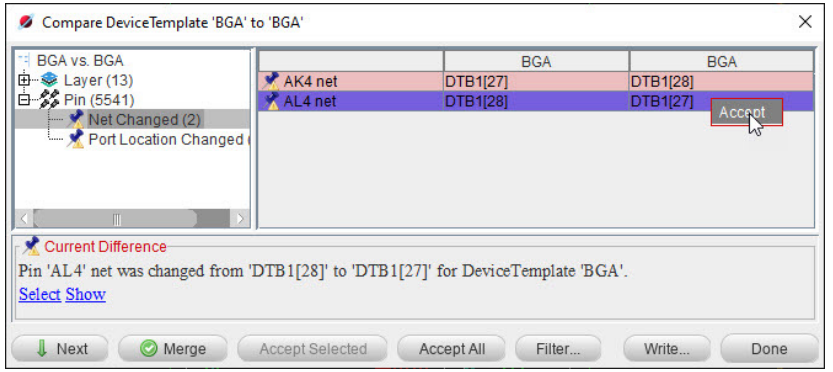
Industry Standard Formats



TSMC 3Dblox™



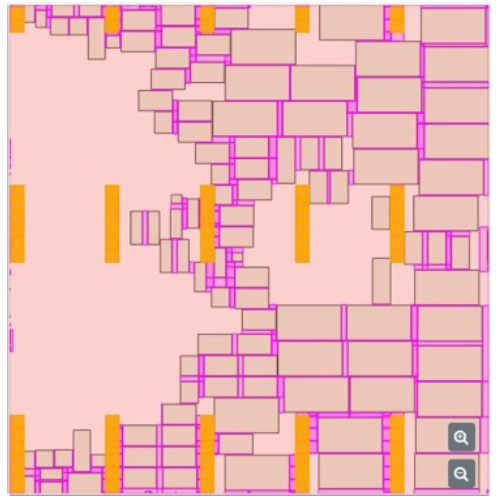
Assembly Design Kits (ADK)

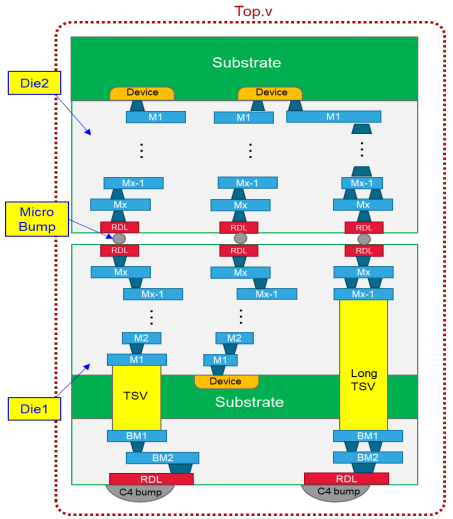


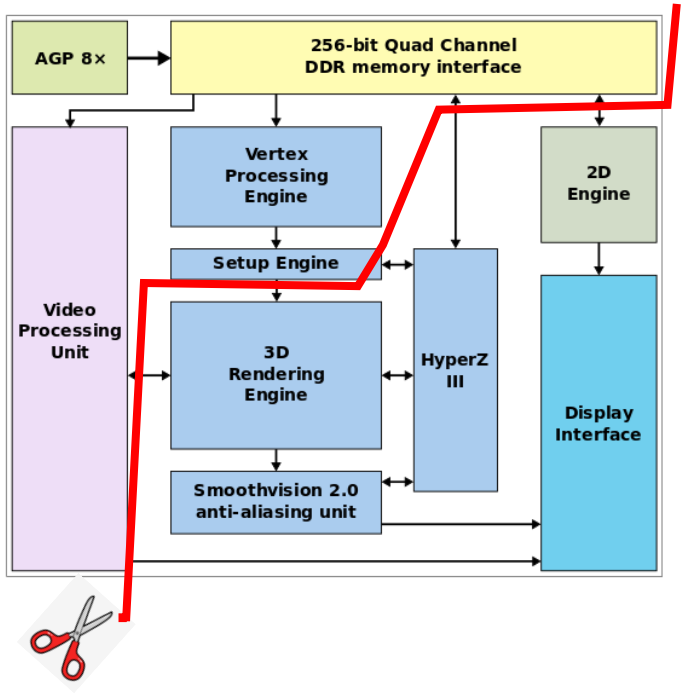
ECO Flow With Layout Tools

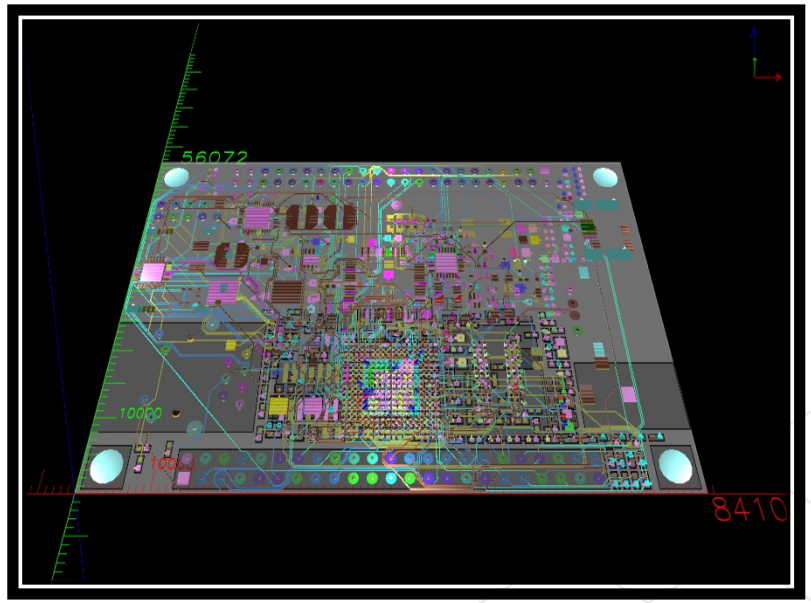
Monolithic Die Design To Silicon Stacking Implementation

- High-capacity (>100M instances) database
- Support for multi-chip(let) heterogeneous integration
  - Multiple tech LEFs/multiple PDKs in a single tool
- Native 3D partitioning
  - Cross-chip(let) mixed placer
- Stack configurator
  - 3Dblox™ support
- Automated TSV optimization
- 3D Visualization
- Co-design with package

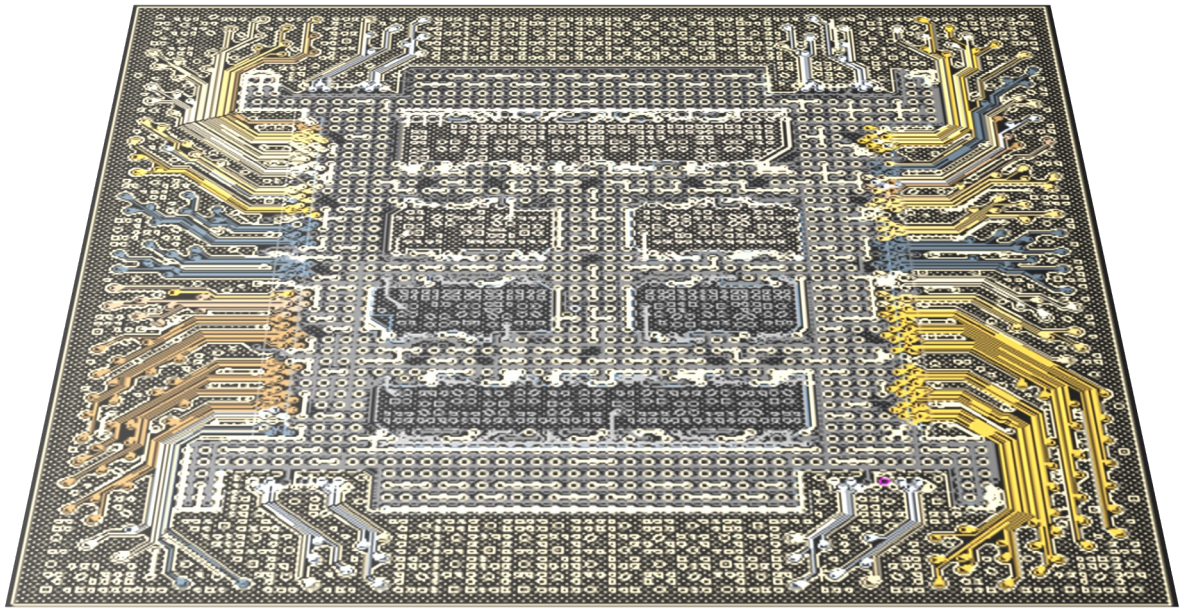








Pivoting to Ultra-High-Density Multi-Die Packaging

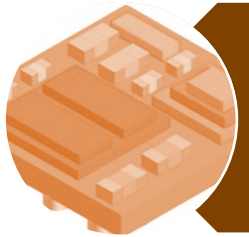


- Flexible connectivity model
- Die stack editor with advanced 3D visualization on DRC
- Bidirectional interface with mask-level physical verification
- Progressive metal (shape/pad/via) degassing
- Direct integration with 3D-EM, signal/power integrity and thermal modeling
- Advanced co-design capabilities with Digital IC and Analog/RF IC

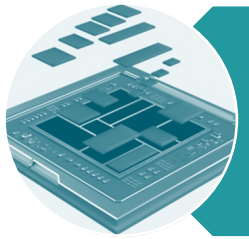
Conclusion

For the past five decades, the electronic industry has thrived while enjoying the benefits of Moore's Law. But things are changing…**The economics of semiconductor logic scaling are gone**

Gordon Moore knew this day would come. **He predicted** that *"It may prove to be **more economical to build large systems out of smaller functions**, which are separately packaged and interconnected."*



Providing the **best alternative to monolithic SoCs, advanced multi-chiplet 3D packages** have become a very attractive option for cost-sensitive complex designs



The generation of "**More Than Moore**" is here bringing new challenges and new opportunities

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THE NEXT GENERATION