Not Just Chips

April 4-6, 2023

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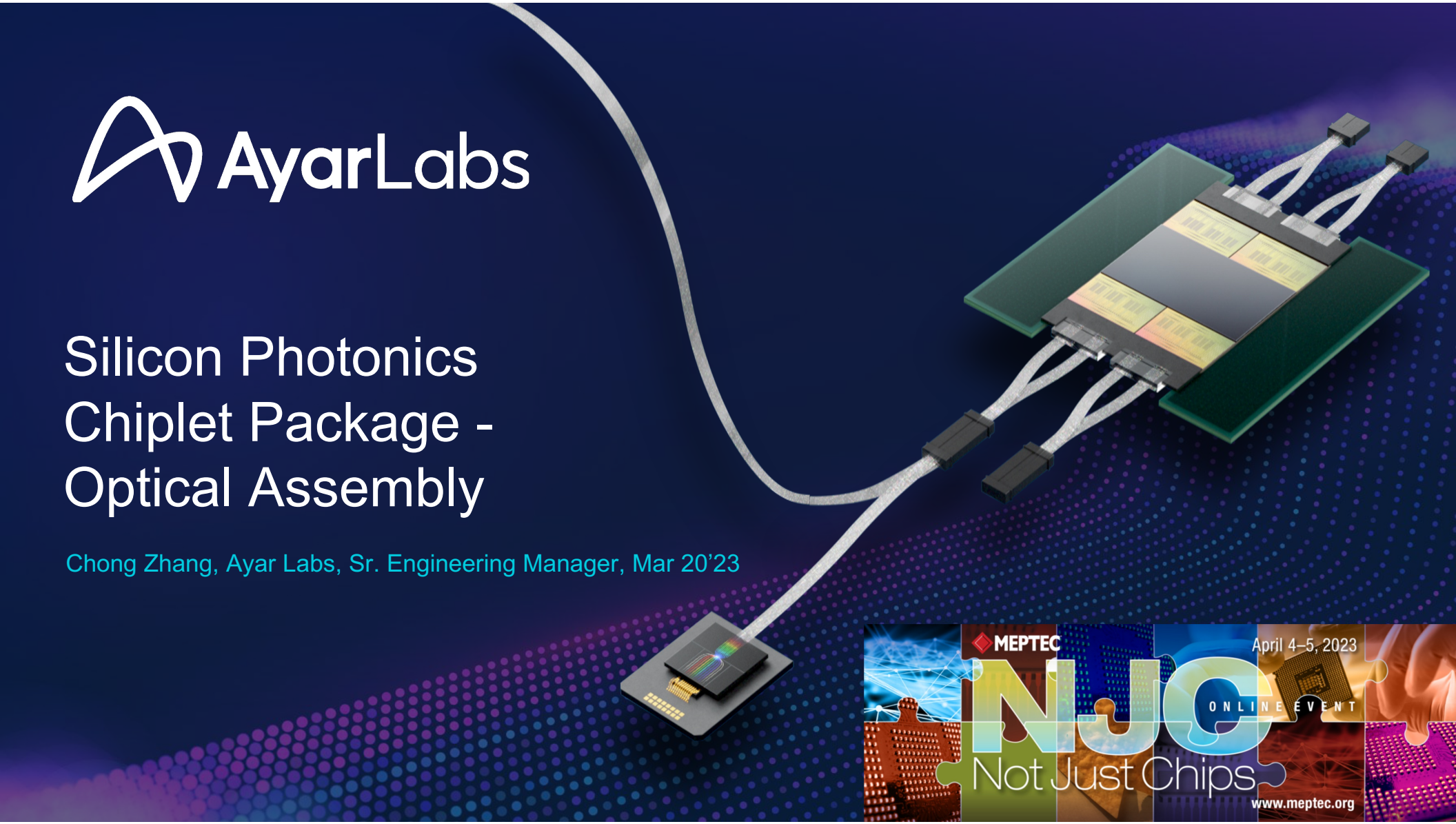
AyarLabs

Silicon Photonics Chiplet Package - Optical Assembly

Chong Zhang, Ayar Labs, Sr. Engineering Manager, Mar 20’23



Agenda (from MEPTEC)

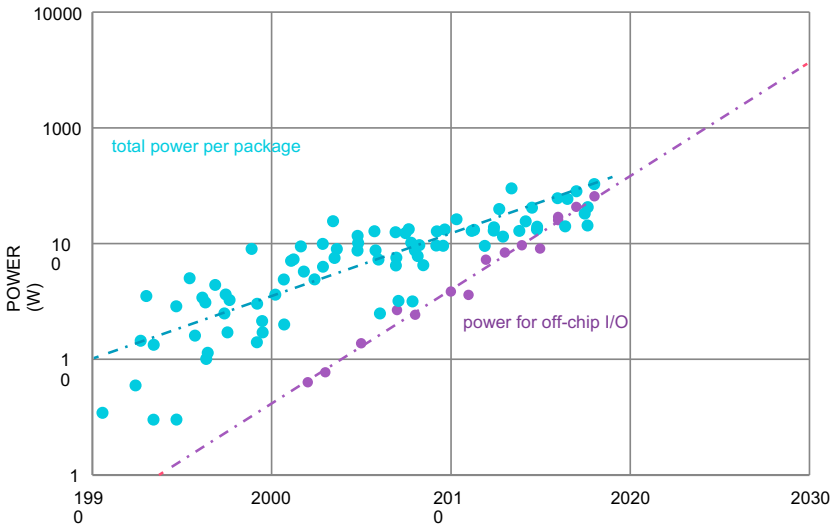
- **Ayar Labs' Silicon Photonics Optical IO Chiplet**
- **2nd Level Optical Interface Summary**
- **Optical Fibers in Silicon Photonics Packaging**
- **1st Level Optical Interface Summary**
- **Optical Adhesive Requirement**
- **Optical Assembly Tool Requirement**
- **Summary**

Ayar Labs' Mission: In-Package Optical I/O

Copper I/O Pin Density near maximum (underside of CPU)

Problem

- Package performance is pin limited
- Power for off-chip I/O increasing and unsustainable

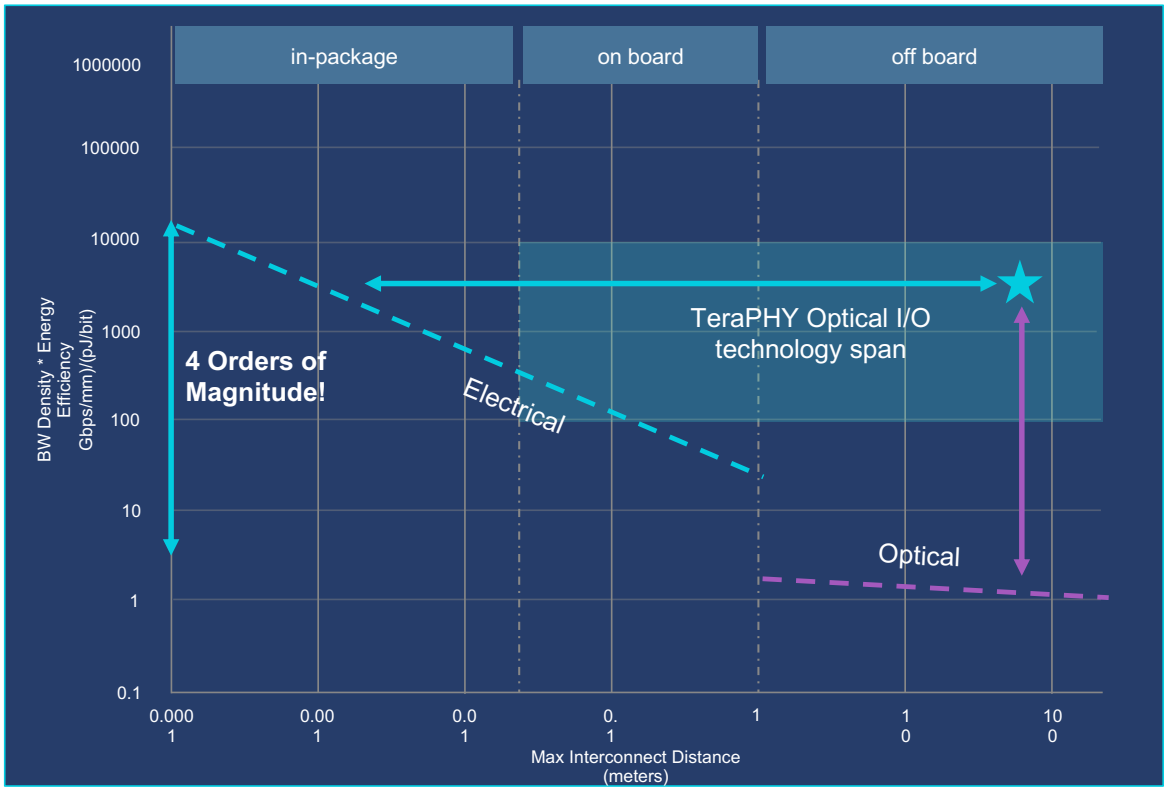


Benefits of Optical I/O

- More power available for compute
- Greater I/O bandwidth to feed more powerful CPU

Source: Xeon Cascade Lake, Anandtech April 2019; Source: G. Keeler, DARPA ERI 2019

The Case for In-Package Optical I/O

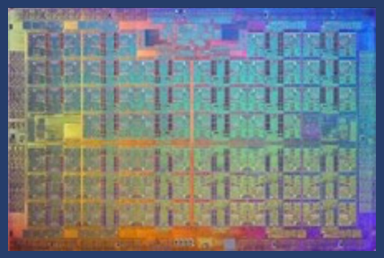
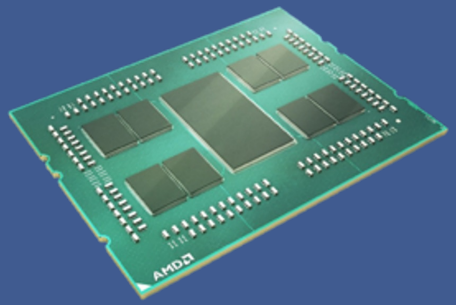
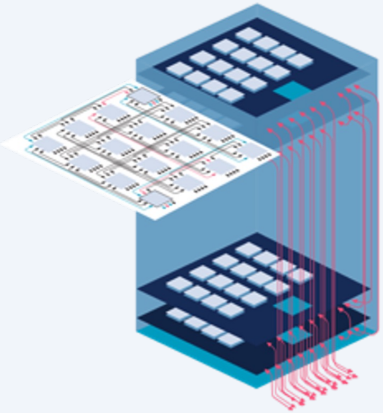


[Gordon Keeler, DARPA ERI Summit 2019]

Benefits of Optical I/O

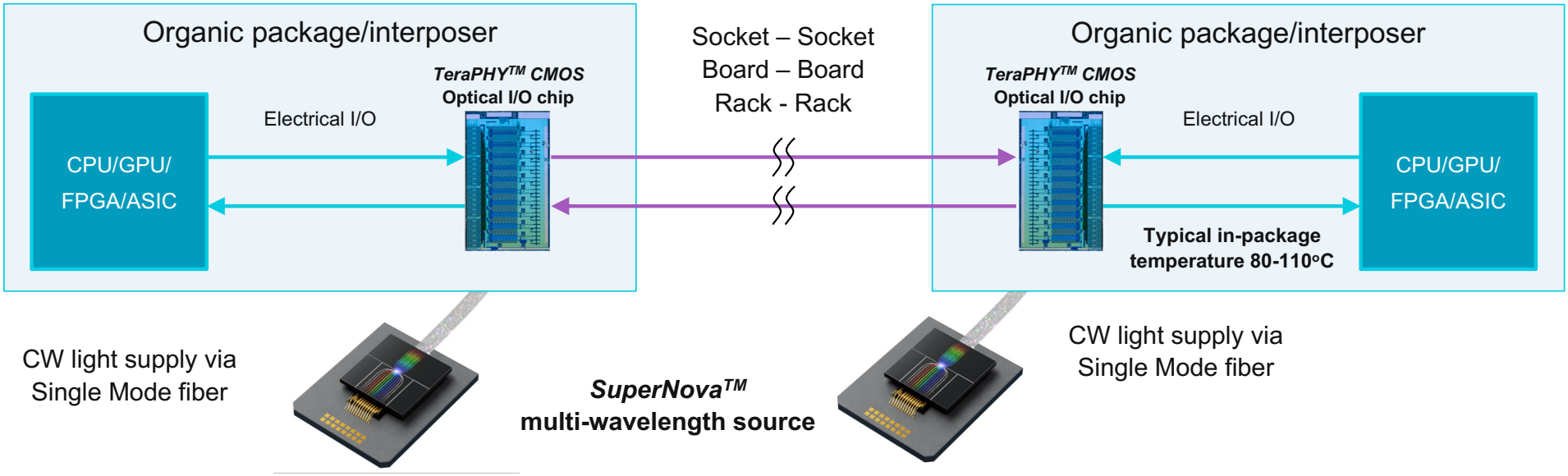
- **Existing in-package electrical chiplet I/O** meets bandwidth, density, and power needs, but cannot go further **than a few mm**.
- **Existing optical solutions** can support 100's of meters of reach, but cannot meet **performance needs**.
- Ayar Labs Optical I/O solution **combines the best of both worlds**.

Optical I/O will Redefine the Compute Socket

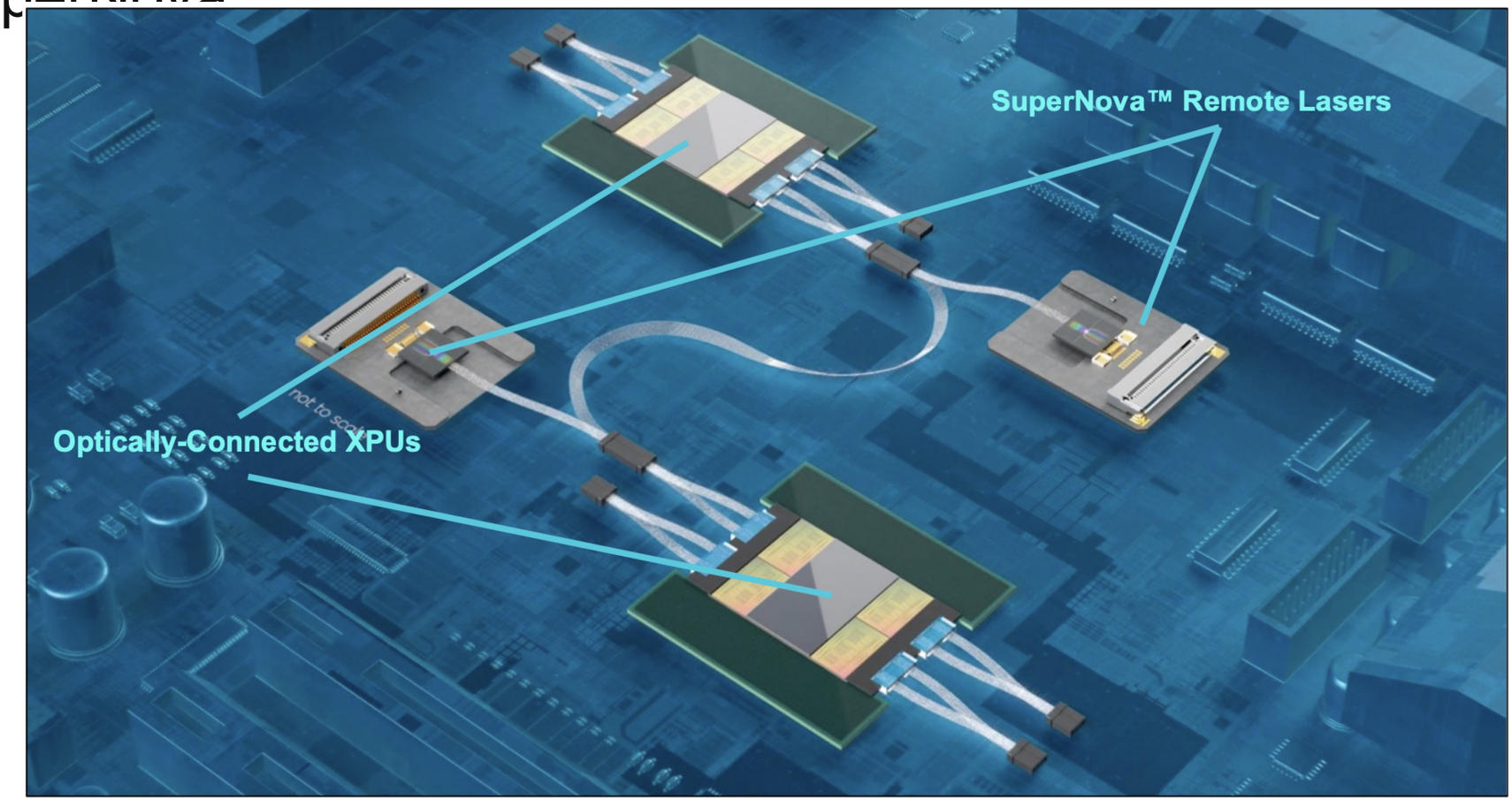
2018	2022	2026
		
Intel Xeon 8B Transistors	AMD EPYC 40B Transistors	The Rack Becomes the “Socket” 100T Transistors

A power efficient, high bandwidth, low latency interconnect WITH REACH will redefine computing architectures

Ayar Labs Core Technology

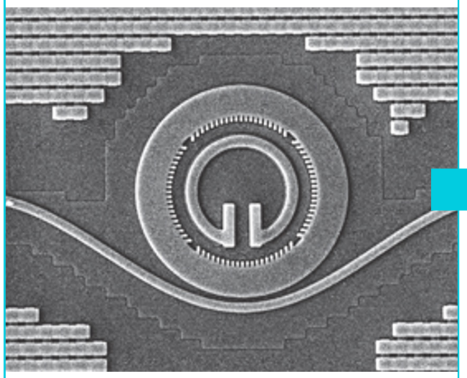


Ayar Labs - System solution with TeraPHY™ and SuperNova™



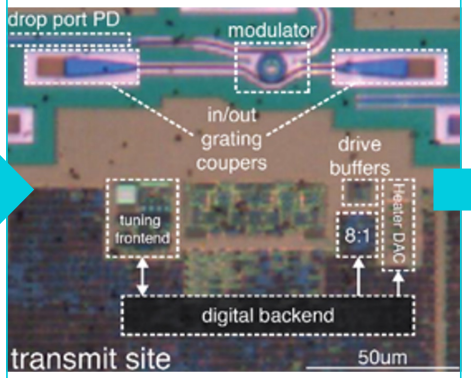
What Does this New Optical I/O Technology Look Like?

Micro-ring Resonators



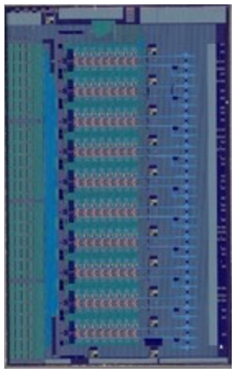
Up to 100x smaller than optical devices in traditional ethernet transceivers

Monolithic Integration



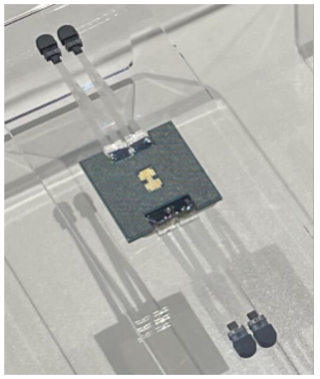
Dense integration of all electronics (TIAs, drivers, equalization, control) and photonics (waveguides, modulators, detectors) on a single CMOS chip

Optical I/O Chiplets



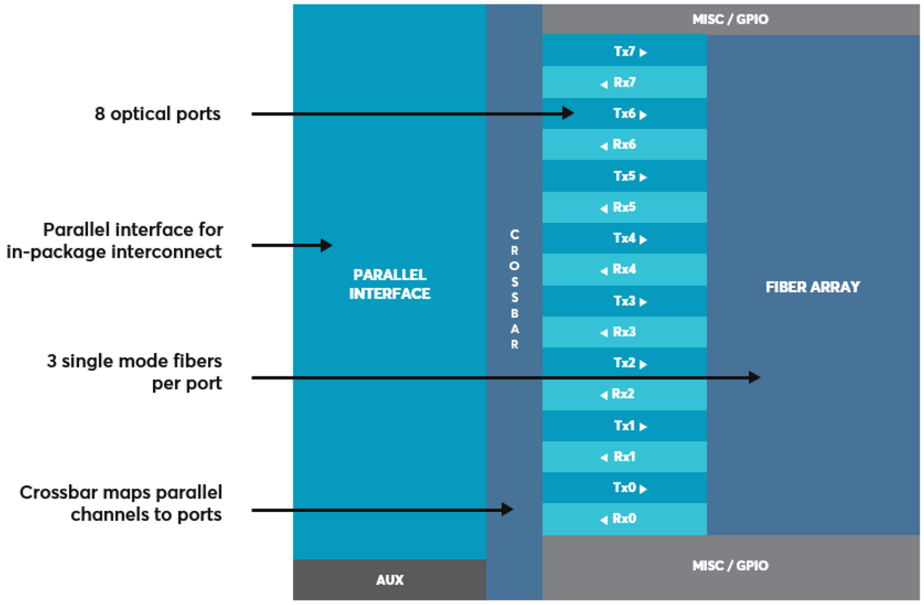
- TeraPHY™ chiplet for in-package optical I/O
- Multi-Tbps with <5pJ/bit
- Nanosecond latency (no FEC required)

SoC In-Package Integration



- Integration with state-of-the-art CPU/GPU/ASIC
- Direct from the package optical I/O

TeraPHY™ In-Package Optical I/O Chiplet

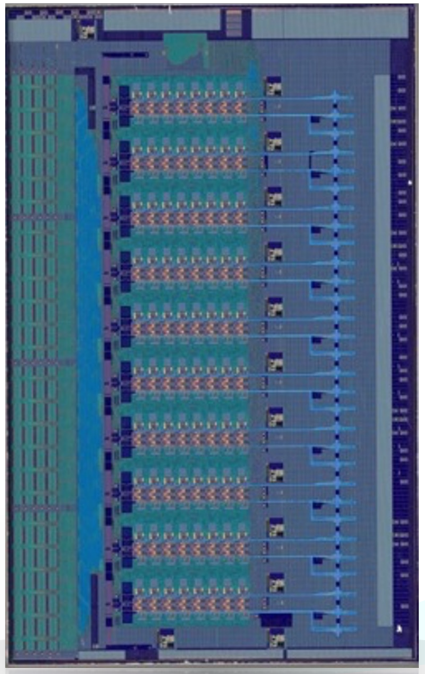


Features

- Supports AIB parallel electrical interface
- Future support for other parallel and serial interfaces
- 8 full-duplex optical ports
- 8 WDM slices per optical port
- Configurable up to 256 Gb/s per port (2 Tb/s per chiplet)
- NRZ modulation format on the optical port – no Forward Error Correction (FEC) required!
- Roadmap to 32+ Tb/s per TeraPHY™ chiplet
- Energy efficiency < 5 pJ/bit
- Latency < 2 x 5ns + TOF
- Distances up to 2km

TeraPHY™ Core Product Roadmap

Host SOC tailored Electrical Interfaces
("Parallel" with 2.5D packaging or "Serial" Organic Packaging)



Performance

Power

With every generation we double the bandwidth at the same time as lowering the energy per bit

2022
2 Tbps Chip
8 macros
8 λ / macro
32Gbps/λ NRZ

2024
4 Tbps Chip
8 - 16 macros
8 λ / macro
32 - 64 Gbps/λ

2026
8 Tbps Chip
8 - 16 macros
8 - 16 λ / macro
32 - 112 Gbps/λ

2028
16 Tbps Chip
8 -16 macros
16 - 32 λ / macro
56 - 112Gbps/λ

2028+
32 Tbps Chip
8 - 16 macros
32 λ / macro
56 - 112Gbps/λ

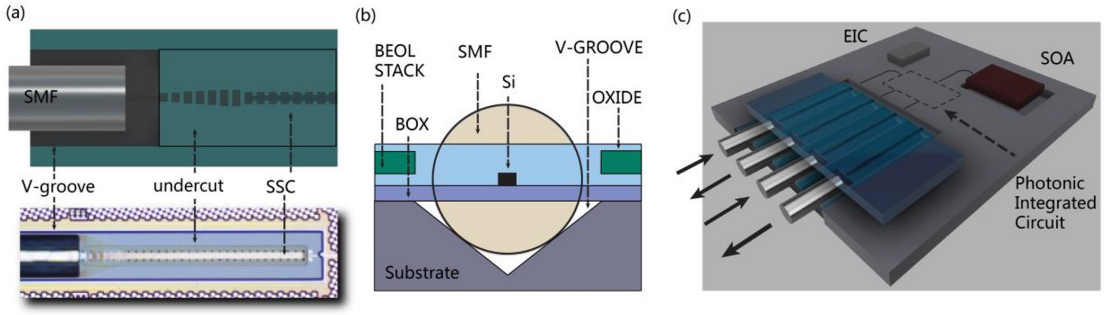
Note: Chip configurations are notional and subject to change

Roadmap reflects core product features. Optimized, custom variants not reflective

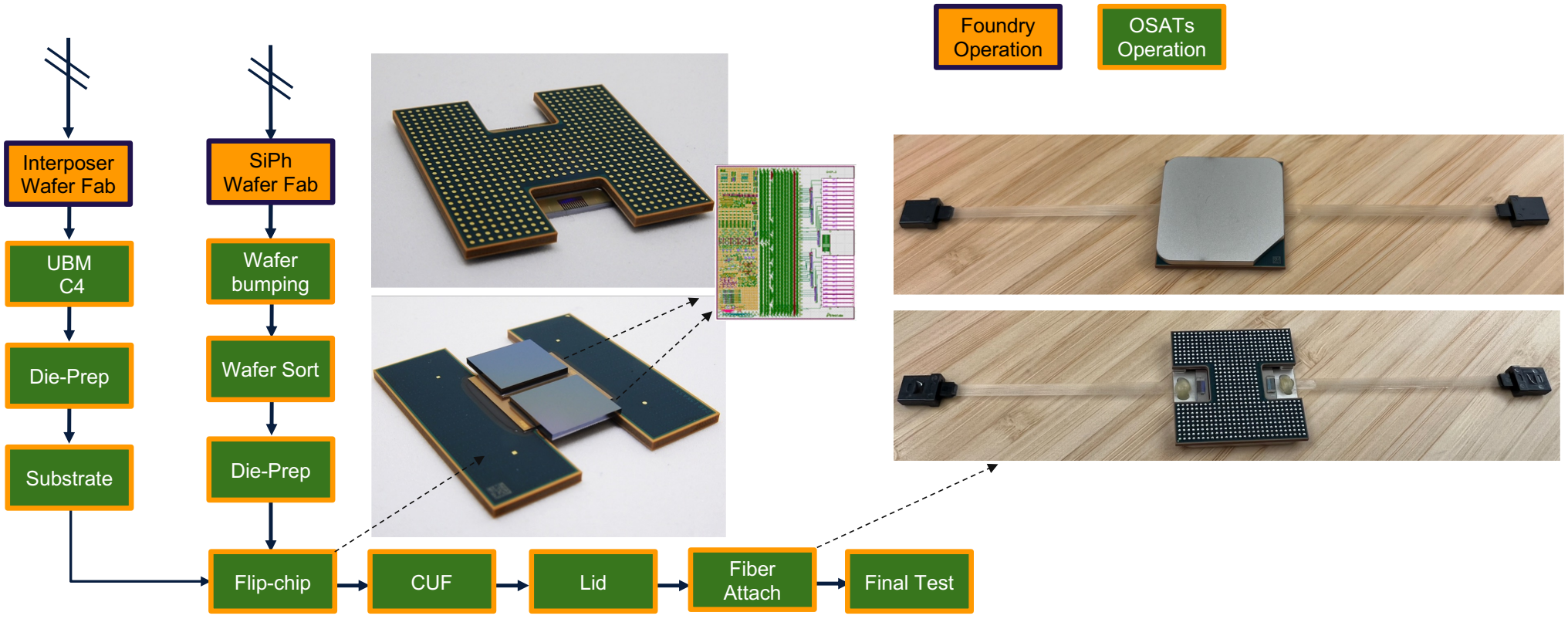
Test Vehicle for Silicon Photonics MCP

- Enable an assembly process flow for silicon interposer-based Multi-Chip Packages (MCP) utilizing Cu-pillar, flip-chip, and IOSMF fiber attach.
- Accomplish above objective by demonstrating:
  - GlobalFoundries' 45CLO (aka GF Fotonix) flip-chip with IOSMF , silicon interposer, and Cu-pillar technologies
  - Industry acceptable assembly yield and reliability metrics
  - Demonstrate viable supply chain, including:
    - Chip supplier, Interposer supplier, organic substrate supplier, fiber array unit (FAU), optical assembly, consumables (e.g., Capillary Underfill (CUF), epoxies, etc.)

Ref: B. Peng, et al., "A CMOS Compatible Monolithic Fiber Attach Solution with Reliable Performance and Self-alignment," in Optical Fiber Communication Conference (OFC) 2020, OSA Technical Digest (Optical Society of America, 2020).

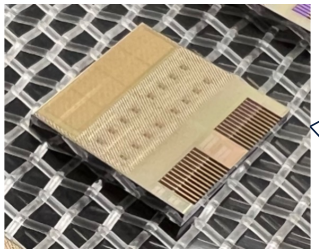


Chip-on-Chip-on-Substrate Process Flow



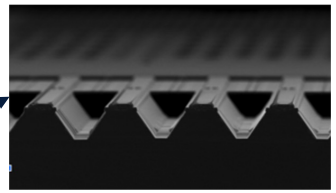
Optical Assembly Background

- Purpose of photonics packaging: provide optical connection between photonics chip and industry standard optical interface.
  - Existing optical communication infrastructure is based on fiber optics.

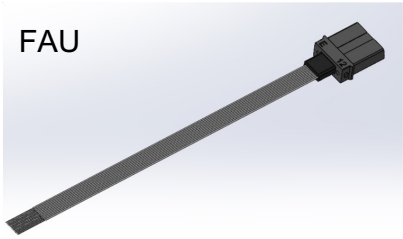


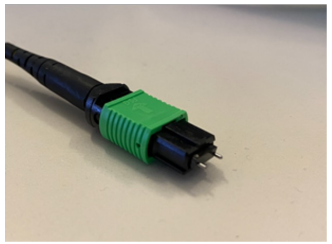
Photonics packaging

edge coupler with v-groove as optical interface on die



FAU

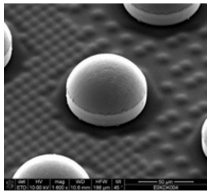




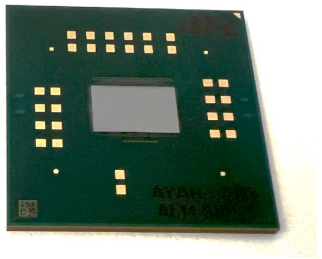
Stress buffer between pluggable optical interface and chip, optical interconnect

Electronics packaging

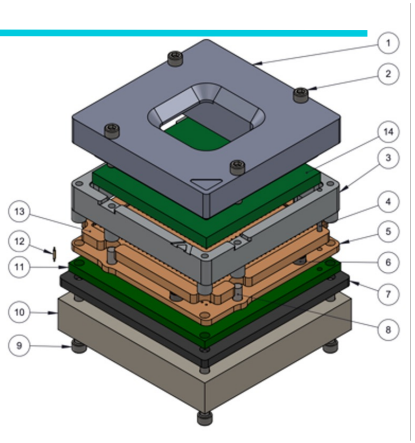
Cu pillar or C4 bumps as electrical interface on die



Substrate



Mechanical support for the chip and electrical interconnect



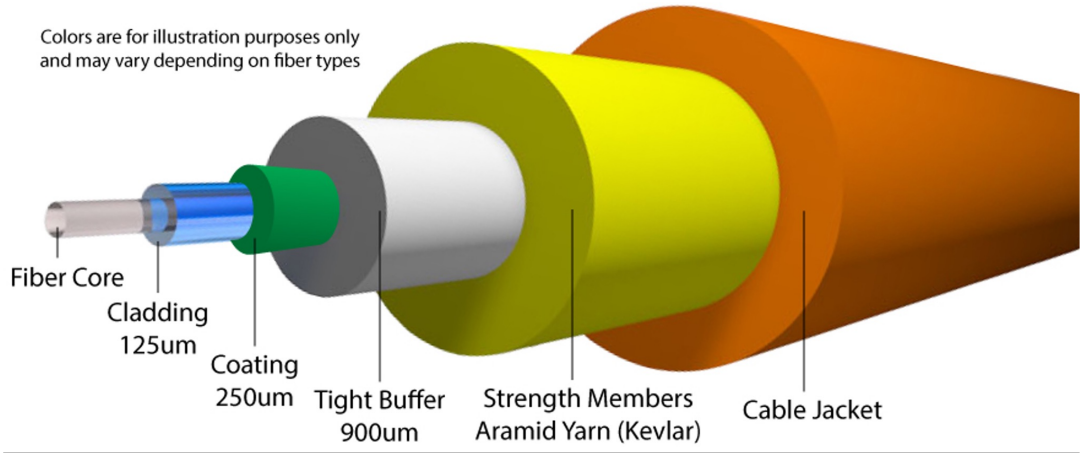
2nd Level Optical Interfaces

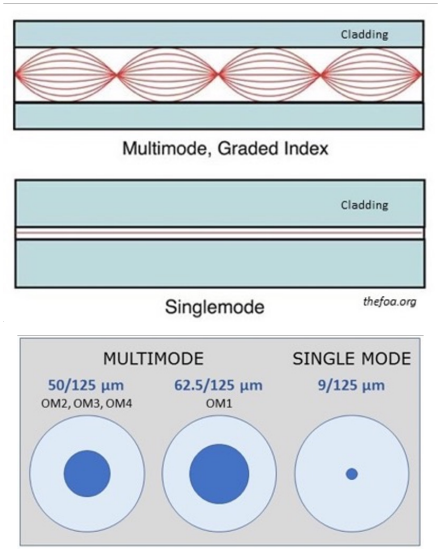
Name	Long form	Coupling type	Ferrule dia	Typical Application	Image
FC	Ferrule connector	Screw	2.5mm	Datacom, telecom, measurement equipment	
LC	Lucent connector	Snap	1.25mm	High-density connections, transceivers	
MPO or MTP	Multiple-Fiber Push-On/Pull-off	Snap	2.5x6.4mm	SM or MM multi-fiber ribbon. device interconnections.	
MT ferrule	Mechanical Transfer ferrule	Snap	2.5x6.4mm	Same as above	
SC	Subscriber connector	Snap	2.5mm	Datacom and telecom (most widely deployed)	

New standard of 2nd level optical interfaces for Optical IO Chiplet:

- Multi-channel (>=12 ch), and compact (can fit within package)
- Pluggable, low loss (<0.35dB) and low variation for repeat mating (10s of mating cycle)
- Low reflectance (<-50dB)
- Solder reflow compatible (260C)
- Resistance to damage and scratch, easy to be cleaned

Optical Fiber for Optical IO Chiplet



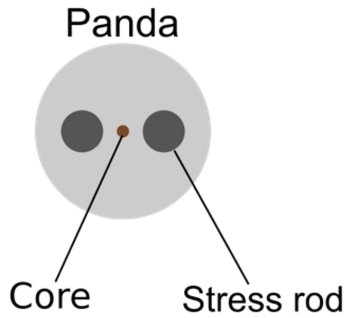


Requirement of optical fiber for Optical IO Chiplet

- SM fiber (typical). PM fiber is required for certain device
- Operating Wavelength: O-band (typical)
- Small cladding diameter (<=80um might be needed), tight tolerance (<1um)
- Low cost, PM fiber ribbon might be needed
- Coating is solder reflow compatible

Polarization Maintaining Fiber (PMF)

- PM fiber (PMF) has a strong built-in birefringence
- The polarization of light launched into the fiber is aligned with one of the birefringent axes



Key optical characteristics

Modal birefringence

$$B_m = \frac{\Delta\beta}{k_0}$$

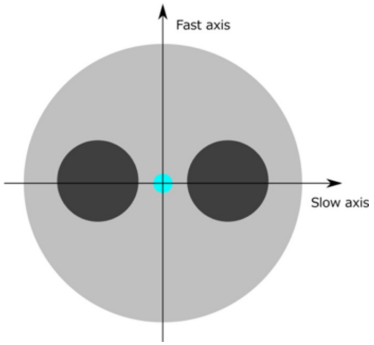
Δβ: propagation constants

$k0=2\pi/\lambda_0$

Large modal birefringence reduces polarization crosstalk, PMFs typically Bm > 10^{-4}

Beat length

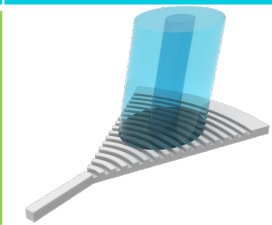
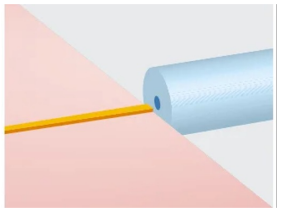
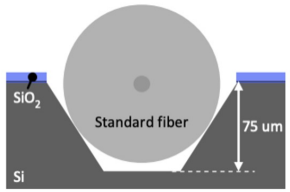
$$L_B(m) = \left(\frac{2\pi}{\Delta\beta}\right) = \left(\frac{\lambda_0}{B_m}\right)$$



Polarization Extinction Ratio (PER) =

$$10\log_{10}\left(\frac{P_y}{P_x}\right)$$

1st Level Optical Interfaces

Type	R&D effort	IL	PDL	Fiber Attach Run rate	Die Prep complexity	Structure stability	Real estate on chip	Scalability	Figure
Grating coupling	Low	High	High	Low	Low	Mid	Large	High	
Edge coupling	Low	Low	Low	Low	High	Low	Small	Low	
V-groove	High	Low	Low	High	Low	High	Large	Low	

NOTE: IL = Insertion Loss, PDL = Polarization Dependent Loss,

Optical Adhesive Key Parameters

- High transparency for the wavelength interested.
- Refractive index: match with oxide, or special requirement based on waveguide design
- UV vs thermal cure: UV cure is required to snap cure the component before thermal cure
- Viscosity: specific range is required for dispense and flow control
- Curing shrinkage: less is preferred
- Coefficient of Thermal Expansion (CTE): low is preferred
- Modulus: depends on application
- Moisture absorption: less is preferred
- Adhesive need to survive solder reflow, and reliability test such as damp heat and thermal cycles.

Optical Assembly Tool

Optical source	Optical power meter	Adhesive dispenser
Vision camera	Alignment engine	UV cure head
Base	Control station	Sensors

Automation software

Requirement:

- High accuracy, high precision
- High throughput
- High integration between alignment engine and sensors
- Easy to operate and debug
- Low cost, low maintenance, reliable

Summary

- Ayar Labs' TeraPHY chiplet can provide a high bandwidth, high energy efficiency, low latency in-Package Optical I/O for future high performance computing requirement
- Ecosystem for optical assembly of silicon photonics chiplet needs to be developed
- A better standard of 2nd level optical interfaces for Silicon Photonics Chiplet is needed
- Optical fiber requirement for silicon photonics chiplet was reviewed. Low cost single mode fiber (SMF) and polarization maintaining fiber (PMF) with tight tolerance control will be needed
- High throughput, scalable 1st level optical interfaces assembly process is required for silicon photonics chiplet to go HVM. V-groove-based edge coupling is currently the industry preference

Thank You!

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