Not Just Chips

April 4-6, 2023

MEPTEC
THE NEXT GENERATION

www.meptec.org

Signal Integrity Analysis at the Dawn of the Interposer Era

Kelly Damalou, Lead Product Manager

Dr. Matt Commens, Senior Manager Product Management

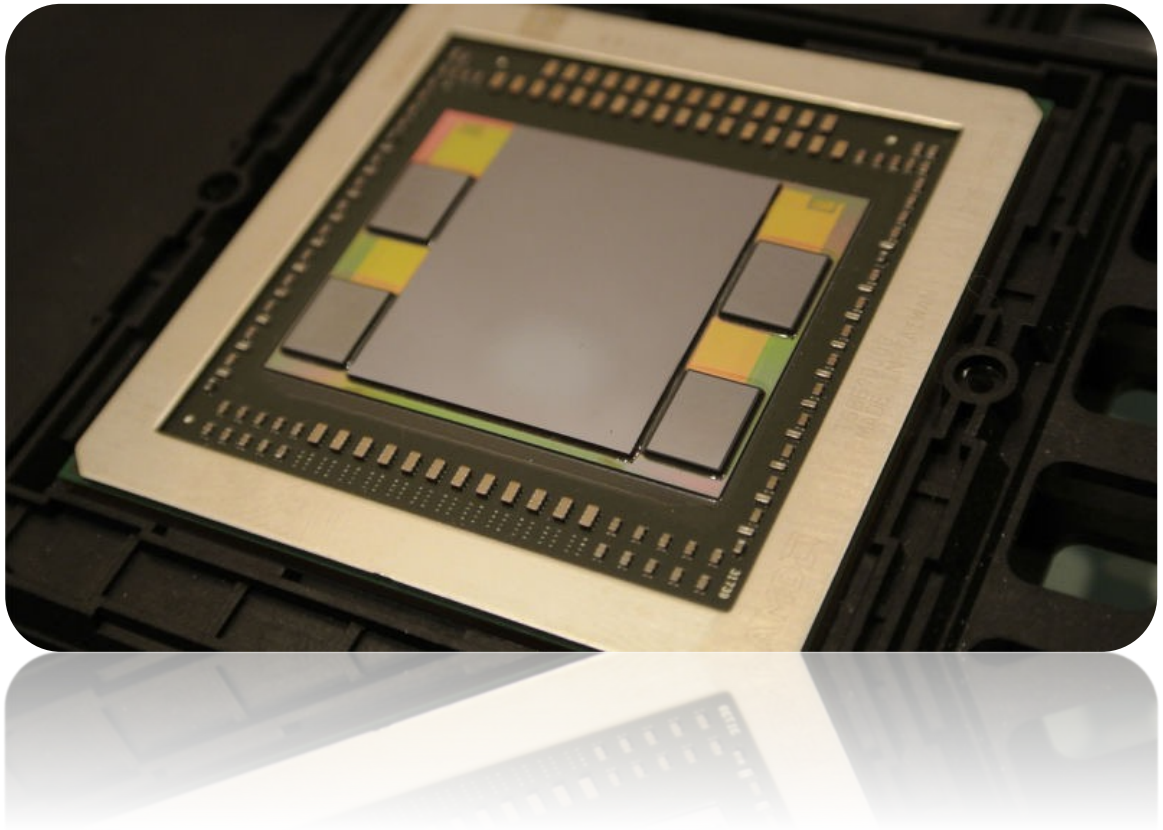
Ansys

Agenda

- 3D-ICs, chiplets and interposers
- Solving the interposer signal integrity challenge: A chip-centric approach
- Solving the interposer signal integrity challenge: A system-centric approach
- Conclusions

IC Market Megatrends…

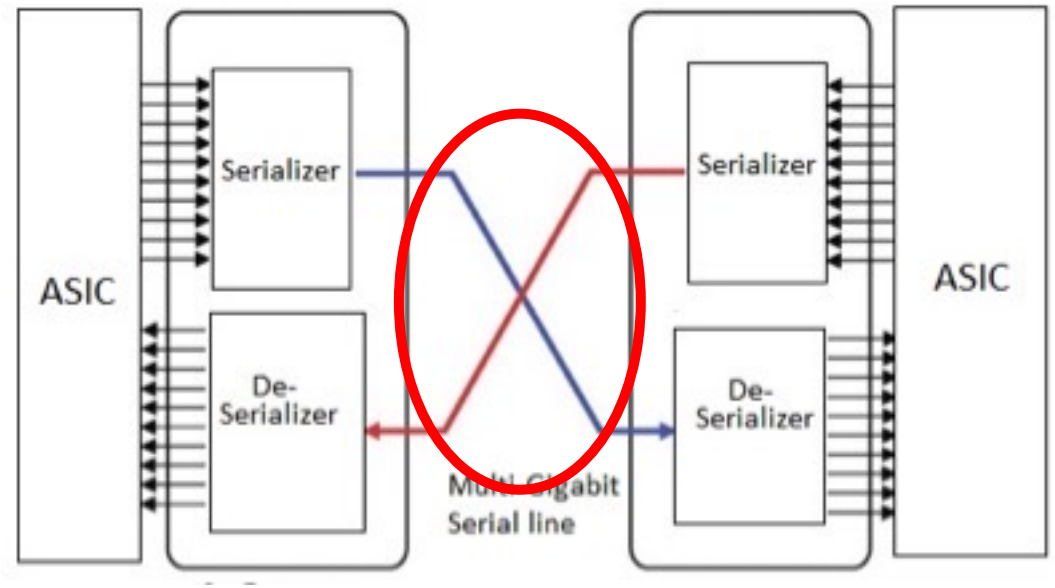
- **Multi-die 3D-ICs on silicon interposers**



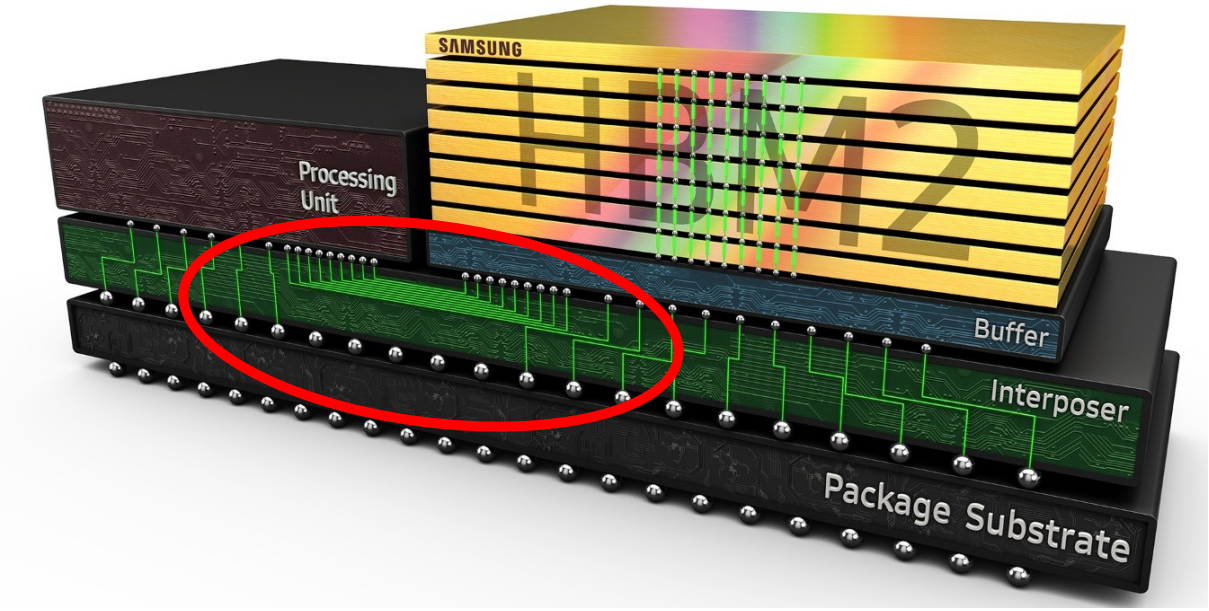
- Bespoke Silicon
- Automotive
- Cloud Computing
- High-Performance Computing (HPC)
- Artificial Intelligence (AI)
  - Machine Learning (ML)
- Internet-of-Things (IoT)
- 5G/6G

All 3D-ICs have in common…

- Extensive use of **SerDes** blocks for chip-to-chip or intra-die multi-Gbps communication (up to 224Gbps!)

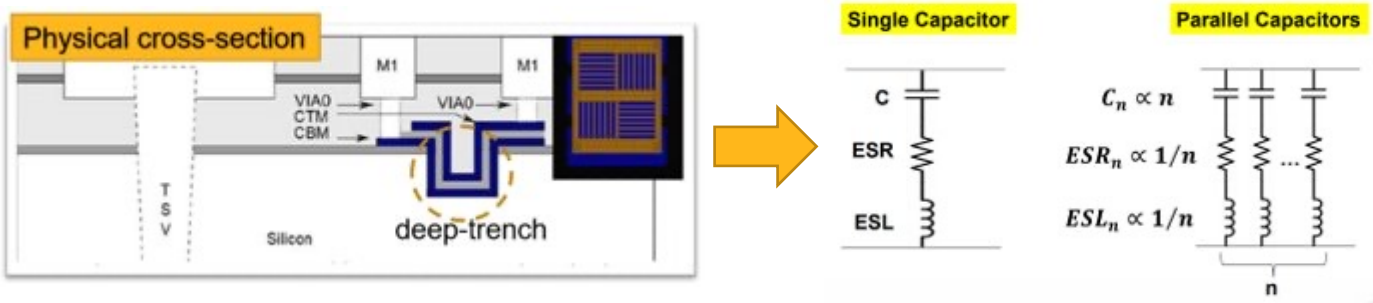


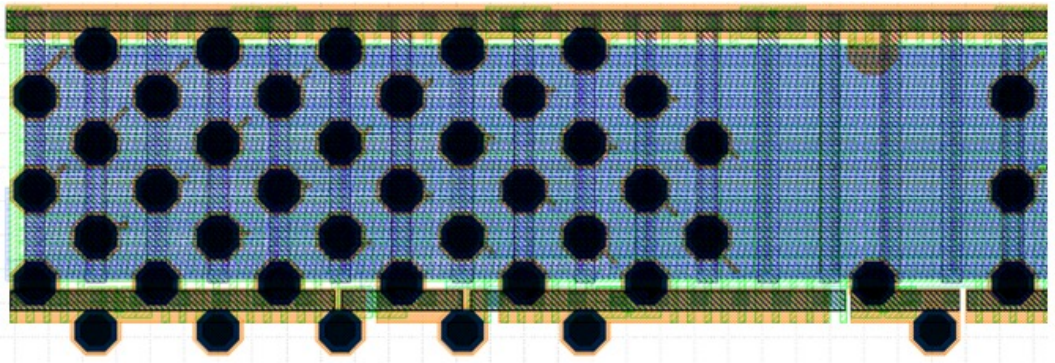
- **HBM2/3** DRAM architectures for very high-speed core-to-memory I/O



Heterogeneous Design with Silicon Interposers

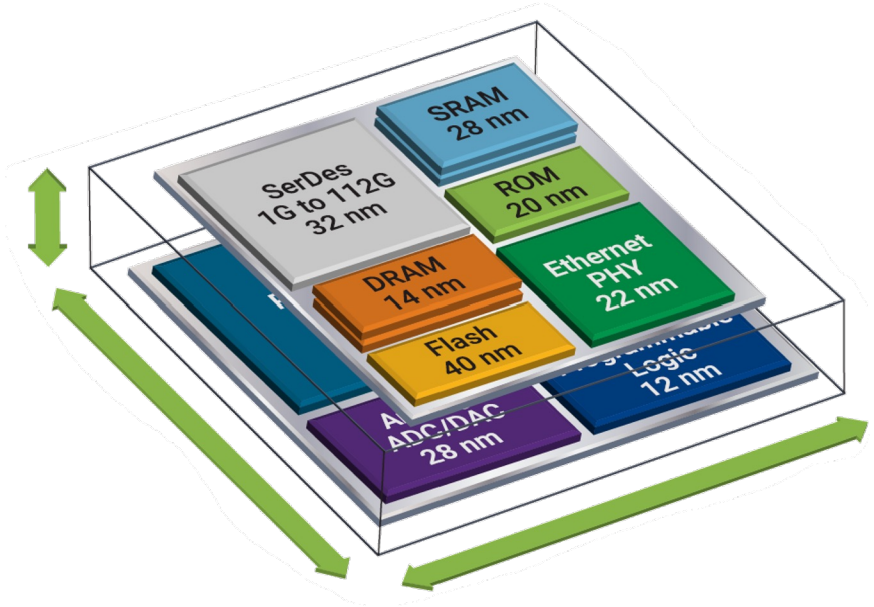
- Heterogeneous design allows for process selection and optimization
  - Each part of system can have an optimized process
- Incorporate ultra high-density capacitors for power integrity
  - Interposer Capacitors (iCAPs)
- Chiplets assembled to form entire system
- Interposers provide for system assembly





3D-IC Engineering Challenges

Engineering Goal



- **Effectively managing 2.5D/3D heterogeneous Integration**
- **Maximizing Power-Performance-Area density**

Engineering Requirements

- **Explore** design trade-offs in early stage with physics insights for optimal architecture selection
- **Implement** optimal design with sophisticated guides (routers, design-rules checkers, …)
  - Progressive design refinement capabilities
- **Analyze** performance against relevant operating conditions throughout the design process
- **Assess** chip-package to system-level electrothermal and structural integrities for reliable, safe and secure solutions
- **Ensure** optimal materials selection for reliability, cost and sustainability targets

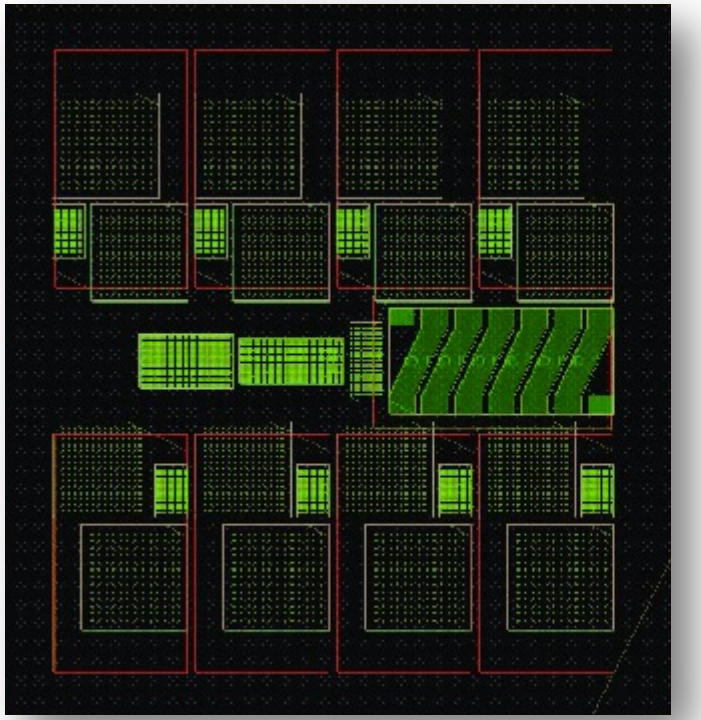
Signal Integrity Analysis for High-Speed Channels

Deep-Dive on the Ansys chip-centric SI analysis workflow with RaptorX

Ansys

SI Challenges for High-Speed Silicon Interposer 2.5D/3D-ICs

- Strict specifications for higher data rates and higher frequencies
- Complex layout, numerous micro-vias plus coupling to silicon substrate
- Components designed and verified separately
- Higher risk of design failure
- Longer design cycles
- Performance compromises
- Extremely costly design re-spins



High-speed channels requires EM-aware SI simulation incl. power and ground network as the whole system performance depends on it!

RaptorH: The Die-centric Approach to 2.5D/3D-IC SI Analysis

Single product with choice of electromagnetic solvers

HFSS: Gold-standard full wave

RaptorX: Accurate, high capacity, high speed

Intuitive interface reduces pilot errors

Cadence Virtuoso and Synopsys Custom Compiler integrations

Read ITF & iRCX files, including encrypted, to automate process setup

Automatically include Layout Dependent Effects (LDE)

Built-in smart defeaturing for faster simulations

Via and void simplifications

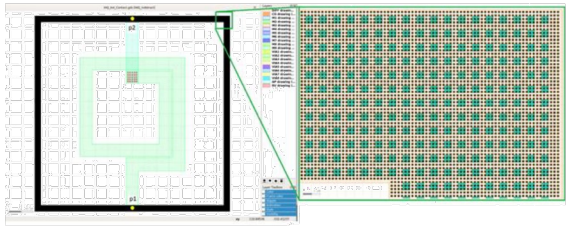
Hierarchy exclusion and simplification

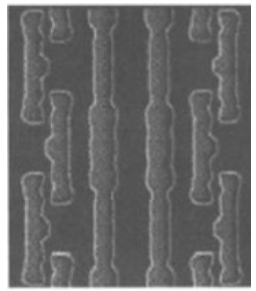
High Performance Modules (HPM)

Access additional cores

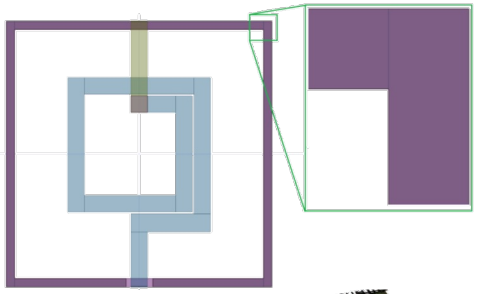
New! Create *"HFSS-ready"* 3D Layout Components

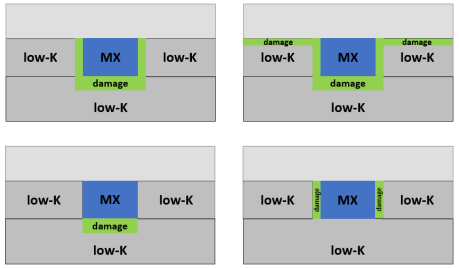
For collaboration and downstream system analysis

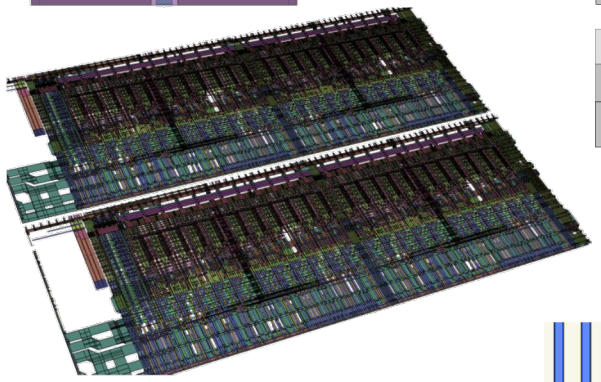


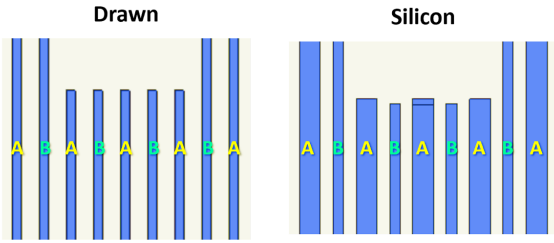


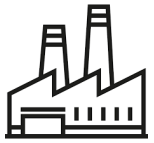
Images: Nanofabrication: Principles, Capabilities and Limits, Zheng Cui, Springer 2010.









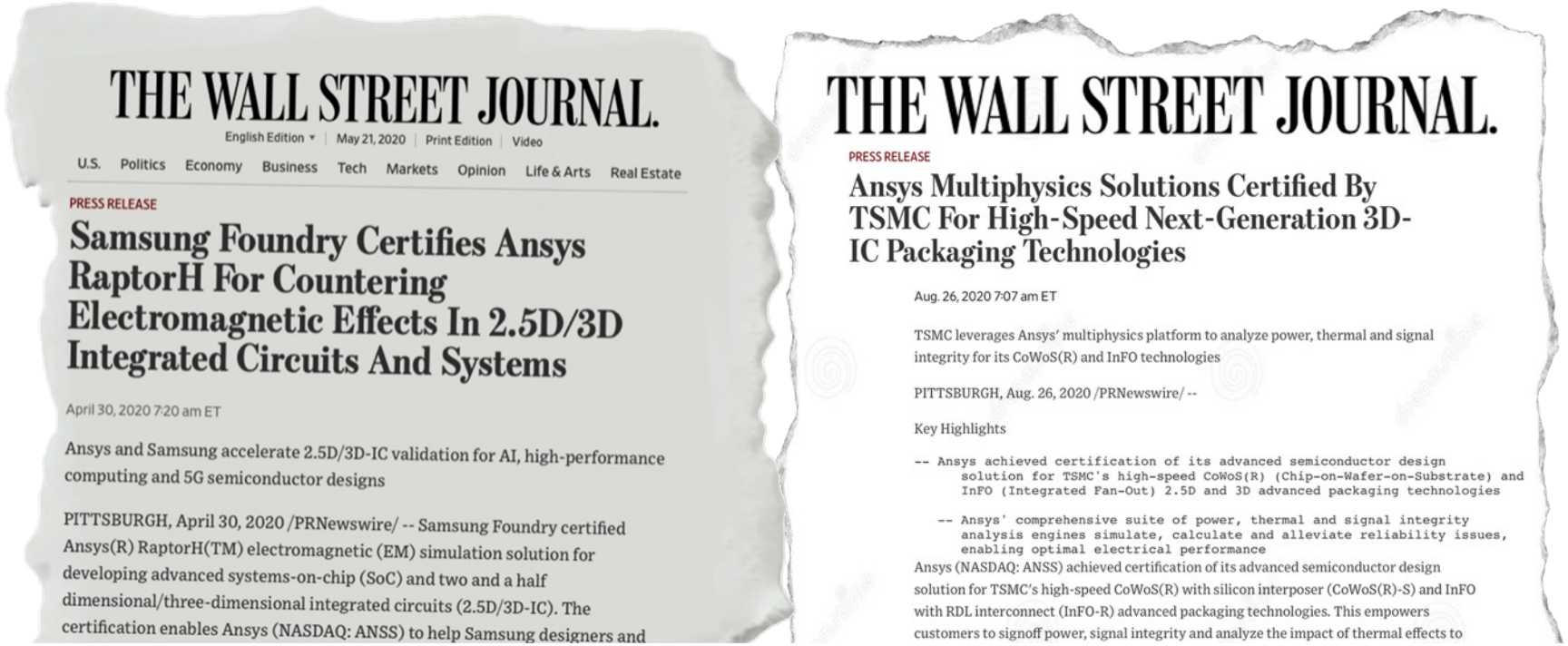


Foundry Certification

- Samsung / certified RaptorH for Interposer modeling
- TSMC / certified RaptorH for CoWoS based design (more to come)

RaptorH certification by foundries seals golden reference status

RaptorH was certified by Samsung and TSMC for 2.5D- and 3D-IC technologies



THE WALL STREET JOURNAL.

English Edition | May 21, 2020 | Print Edition | Video

U.S. Politics Economy Business Tech Markets Opinion Life & Arts Real Estate

PRESS RELEASE

Samsung Foundry Certifies Ansys RaptorH For Countering Electromagnetic Effects In 2.5D/3D Integrated Circuits And Systems

April 30, 2020 7:20 am ET

Ansys and Samsung accelerate 2.5D/3D-IC validation for AI, high-performance computing and 5G semiconductor designs

PITTSBURGH, April 30, 2020 /PRNewswire/ -- Samsung Foundry certified Ansys(R) RaptorH(TM) electromagnetic (EM) simulation solution for developing advanced systems-on-chip (SoC) and two and a half dimensional/three-dimensional integrated circuits (2.5D/3D-IC). The certification enables Ansys (NASDAQ: ANSS) to help Samsung designers and

THE WALL STREET JOURNAL.

PRESS RELEASE

Ansys Multiphysics Solutions Certified By TSMC For High-Speed Next-Generation 3D-IC Packaging Technologies

Aug. 26, 2020 7:07 am ET

TSMC leverages Ansys' multiphysics platform to analyze power, thermal and signal integrity for its CoWoS(R) and InFO technologies

PITTSBURGH, Aug. 26, 2020 /PRNewswire/ --

Key Highlights

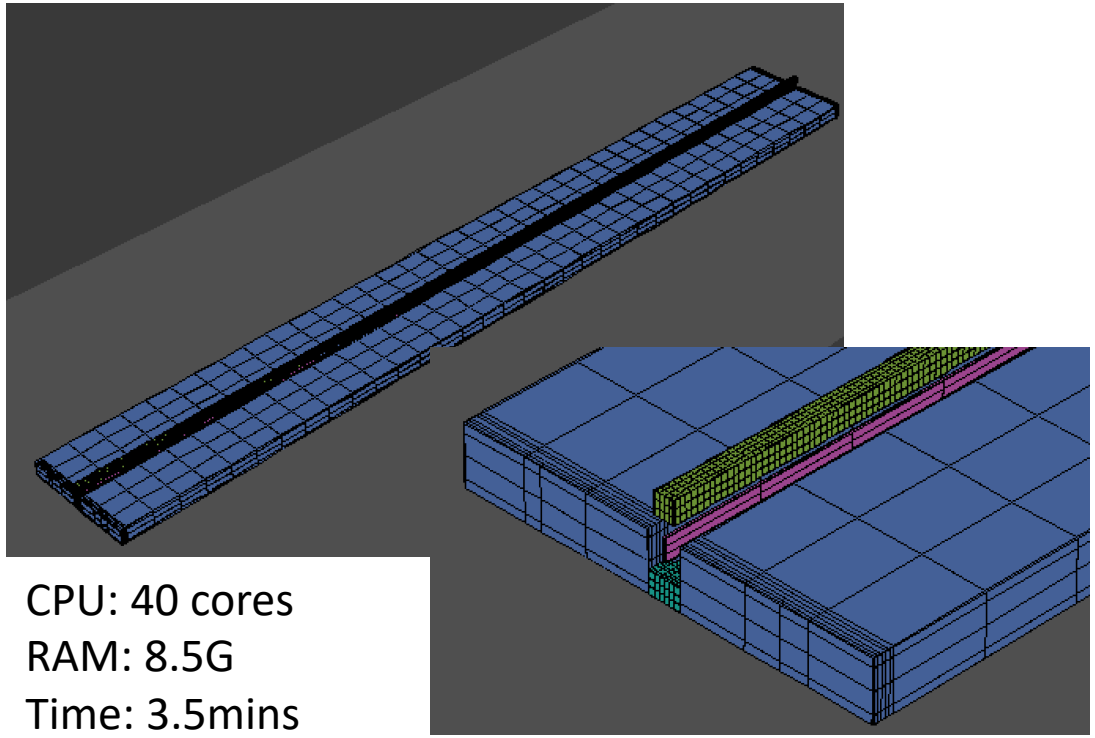
-- Ansys achieved certification of its advanced semiconductor design solution for TSMC's high-speed CoWoS(R) (Chip-on-Wafer-on-Substrate) and InFO (Integrated Fan-Out) 2.5D and 3D advanced packaging technologies

-- Ansys' comprehensive suite of power, thermal and signal integrity analysis engines simulate, calculate and alleviate reliability issues, enabling optimal electrical performance

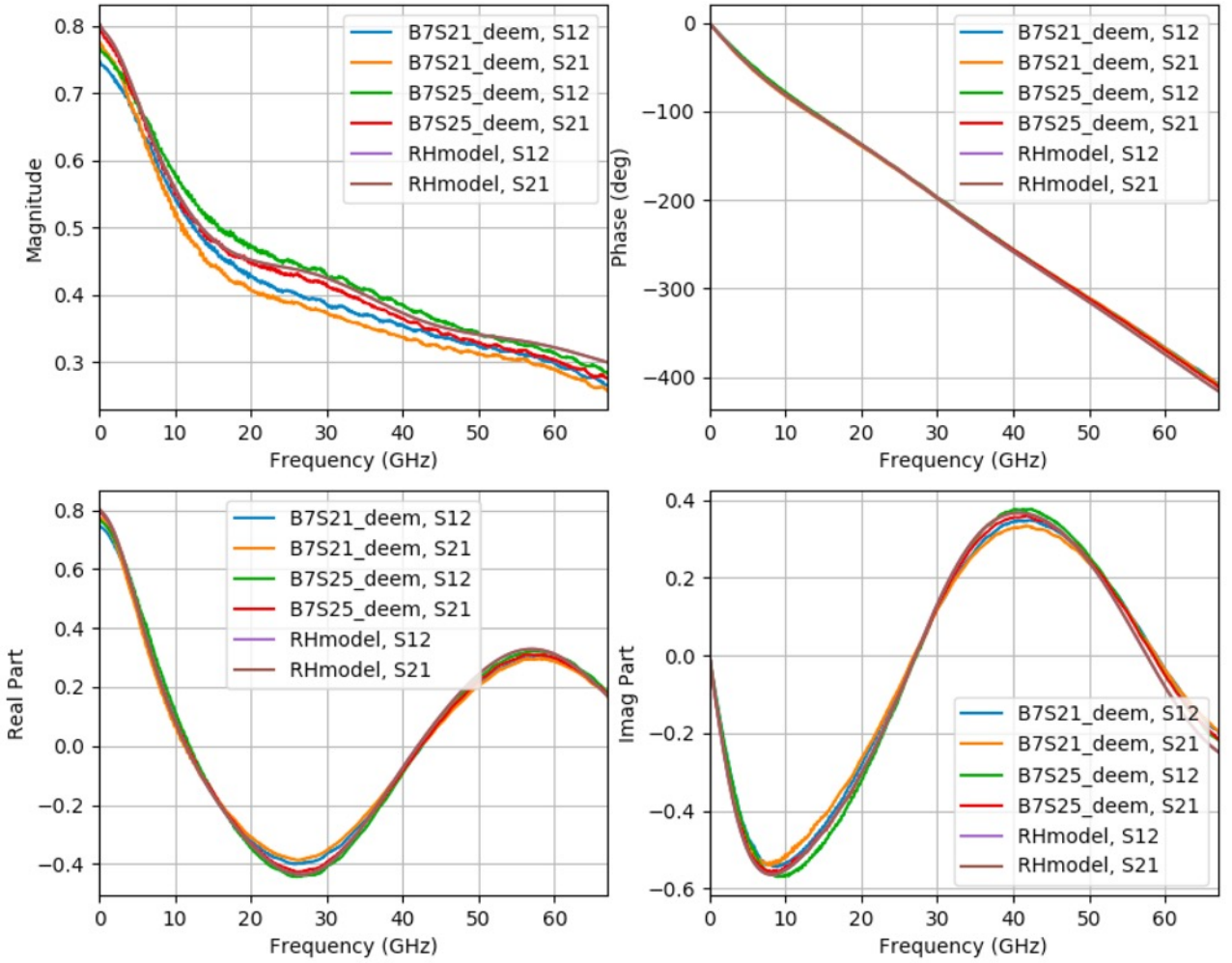
Ansys (NASDAQ: ANSS) achieved certification of its advanced semiconductor design solution for TSMC's high-speed CoWoS(R) with silicon interposer (CoWoS(R)-S) and InFO with RDL interconnect (InFO-R) advanced packaging technologies. This empowers customers to signoff power, signal integrity and analyze the impact of thermal effects to

TSMC certified Ansys RaptorH (RaptorX solver) for DC-70GHz

- Multiple silicon experiments run
- Models exhibited perfect correlation from DC-70GHz



CPU: 40 cores
RAM: 8.5G
Time: 3.5mins

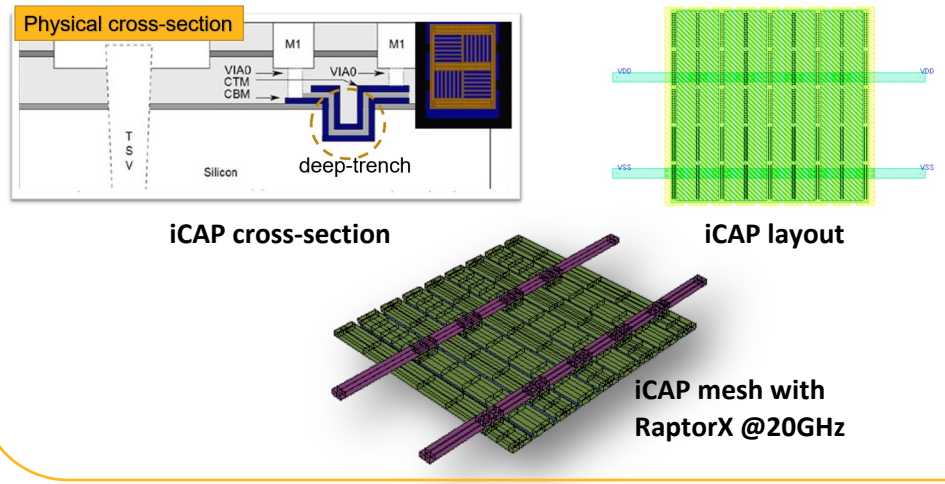


Analytical modeling of iCAPs (**I**nterposer **CAP**acitors)

- iCAPs are ultra high-density capacitors widely used in power management at interposer configurations
- 1000s of iCAPs in an interposer
- **RaptorX can solve 1000s of iCAPs with highest fidelity and speed**
- RaptorX leverages the capability to model conformal dielectric arrangements

Important building block in the interposer analysis workflow

Layout and RaptorX mesh of iCAP @20GHz

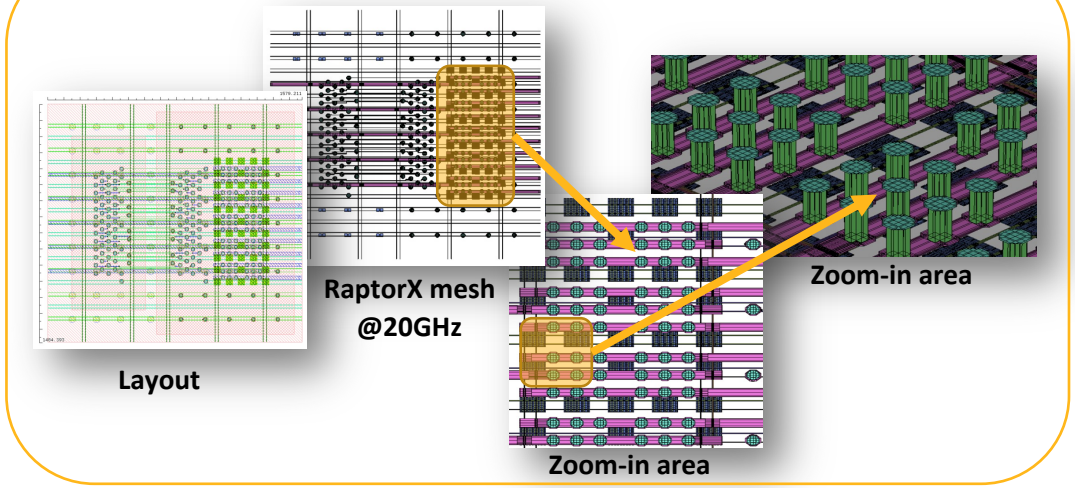


iCAP cross-section

iCAP layout

iCAP mesh with RaptorX @20GHz

Large layout with iCAPs meshed @20GHz with RaptorX



Layout

RaptorX mesh @20GHz

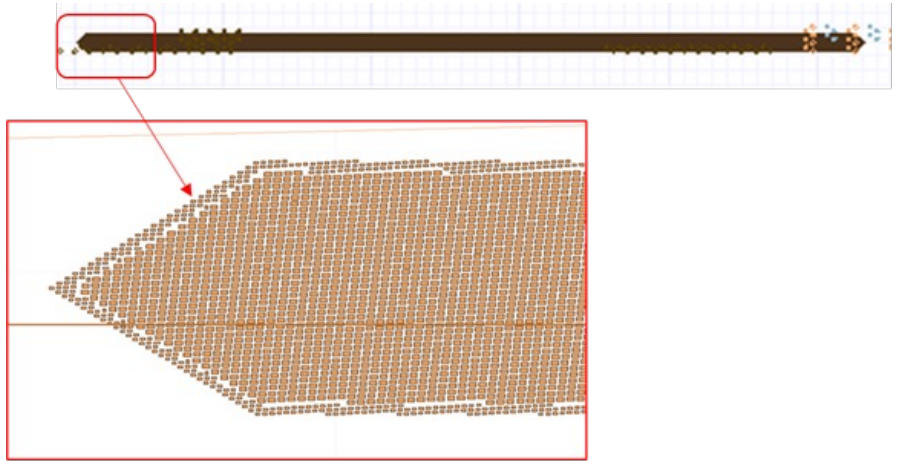
Zoom-in area

Zoom-in area

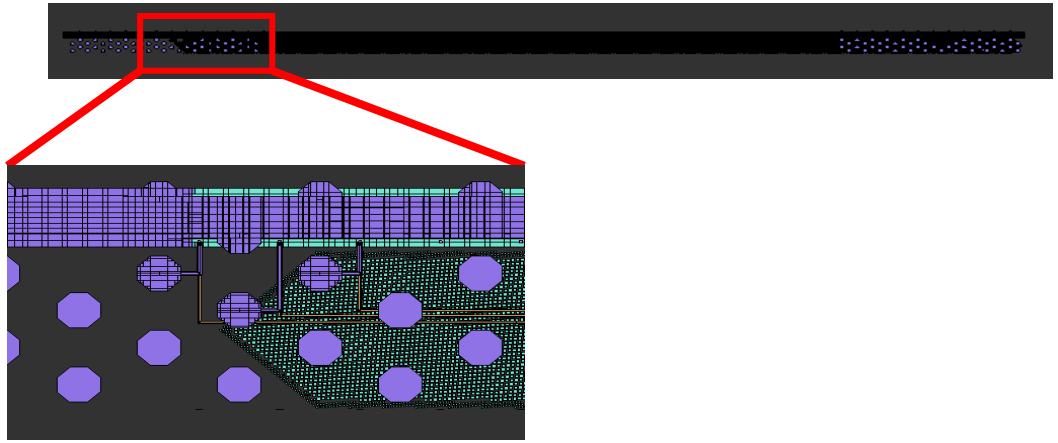
Case study: HBM channel with dense dummy tiles

HBM Design with dummy metals

- Interposer design with lots of floating metals on M1 layer
- 3 signal nets and GND nets
- Three metal layers
- Length is about 6mm



	RaptorX
Dummy Layer extraction	Yes
Number of signals	3 signals + GND
Extraction Time	25m:21s
CPU cores	40
RAM	56.4G

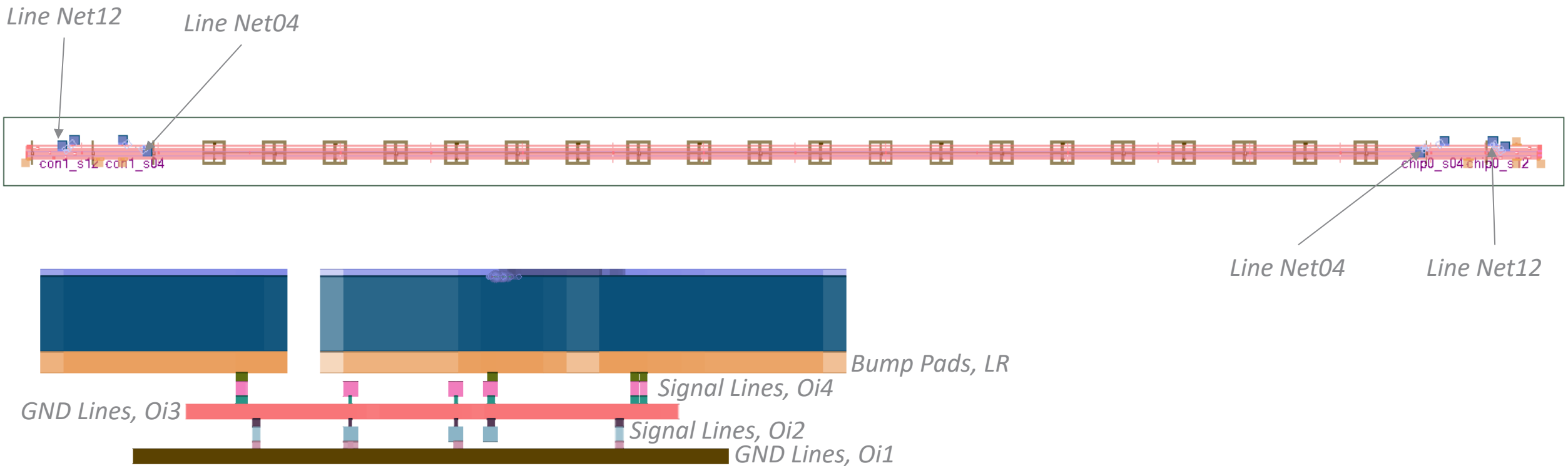


Case study:

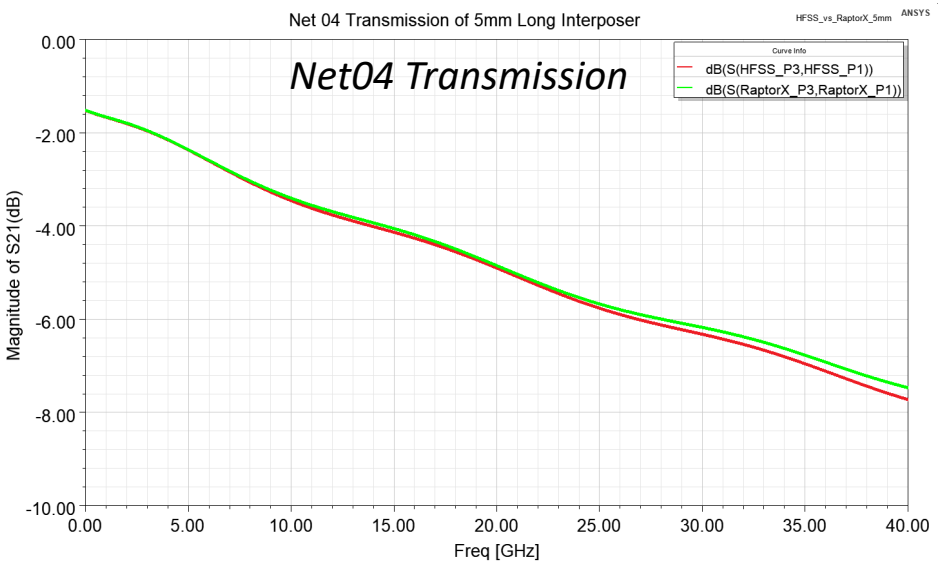
5mm Si Interposer with 2 signal lines and GND

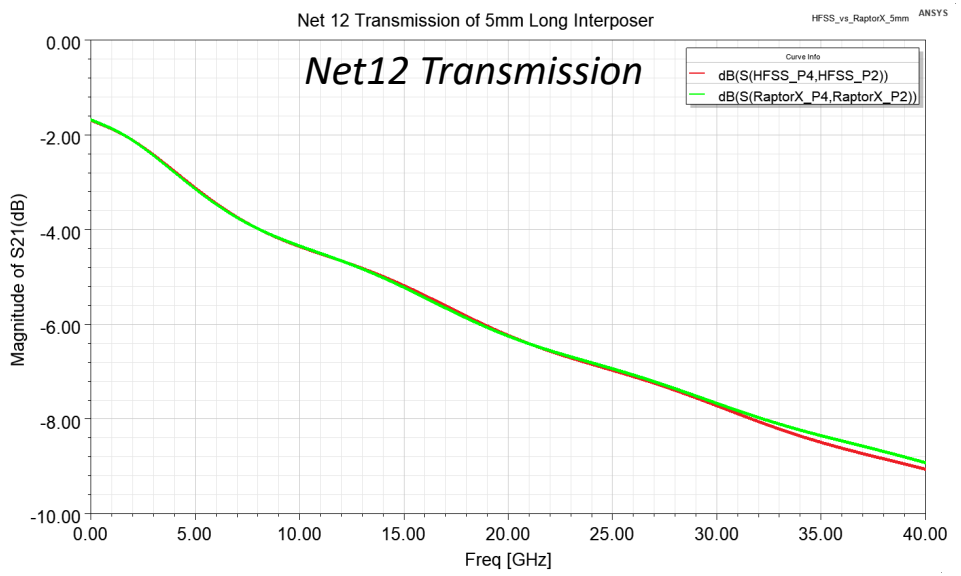
Layout: ~5.2 mm x 0.04 mm with 2 signal lines and GND

- Net04 is ~4.2mm long on Oi4 layer
- Net12 is ~5mm long on Oi2 layer
- GND net mainly on layer Oi3, also partly on Oi4 and Oi1



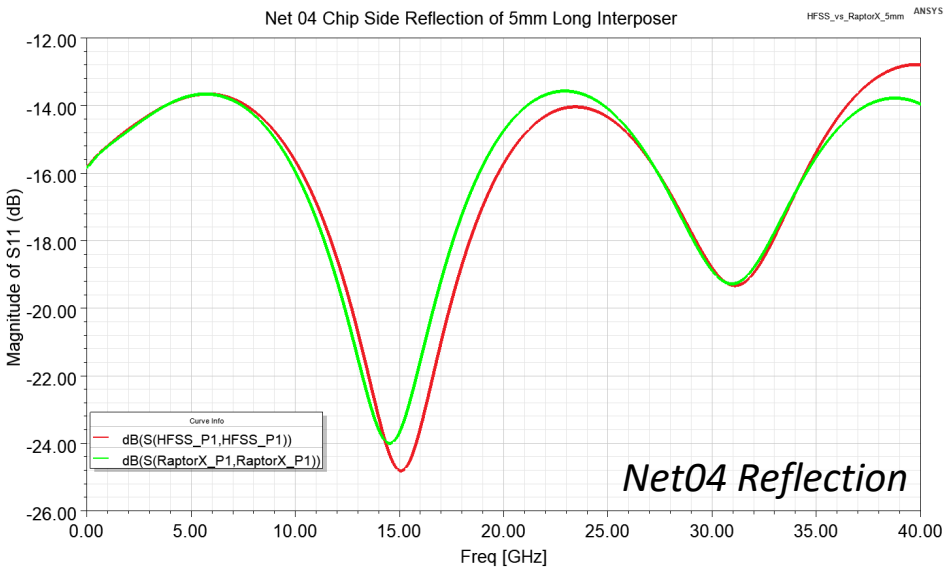
RaptorX vs HFSS: Transmission & Reflection of Net04 and Net12

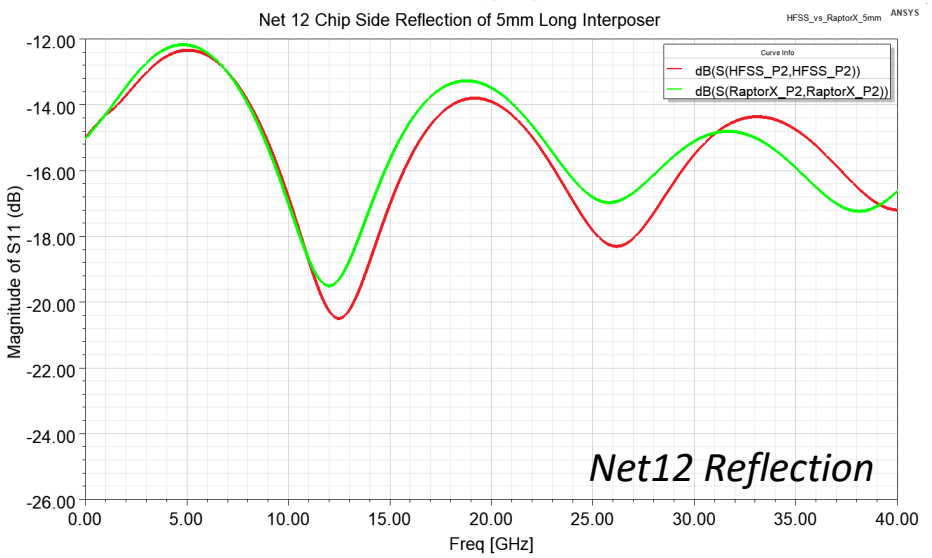




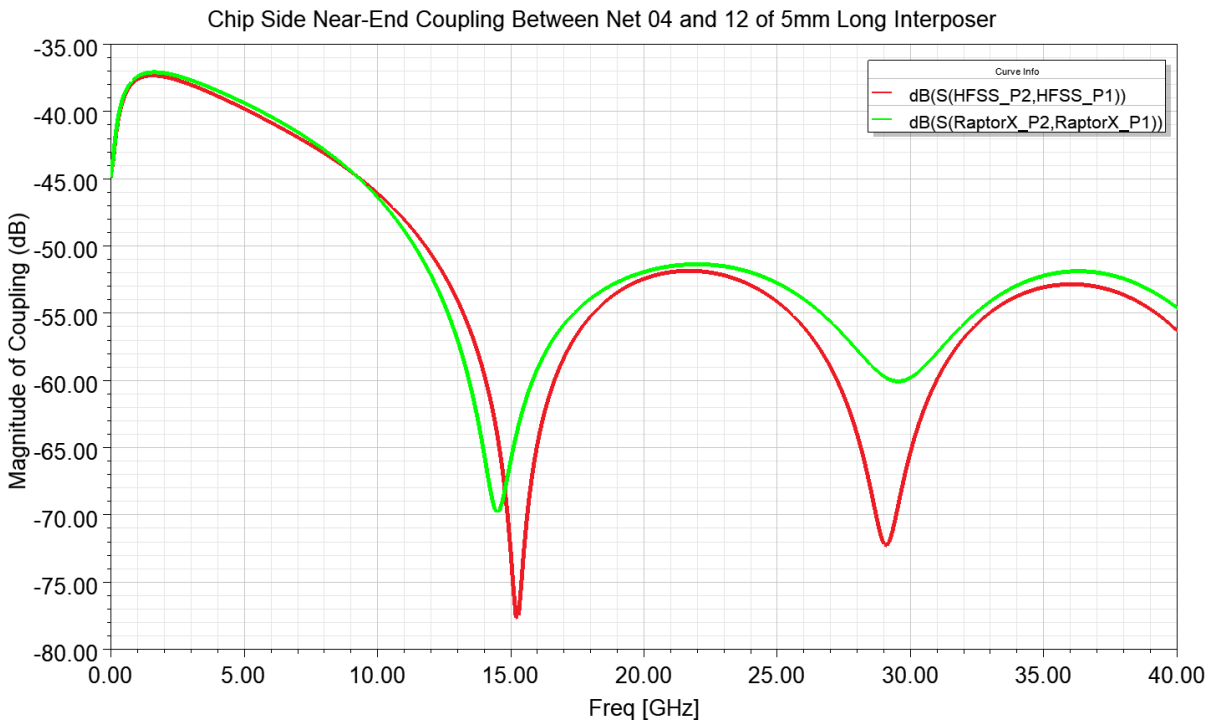
HFSS

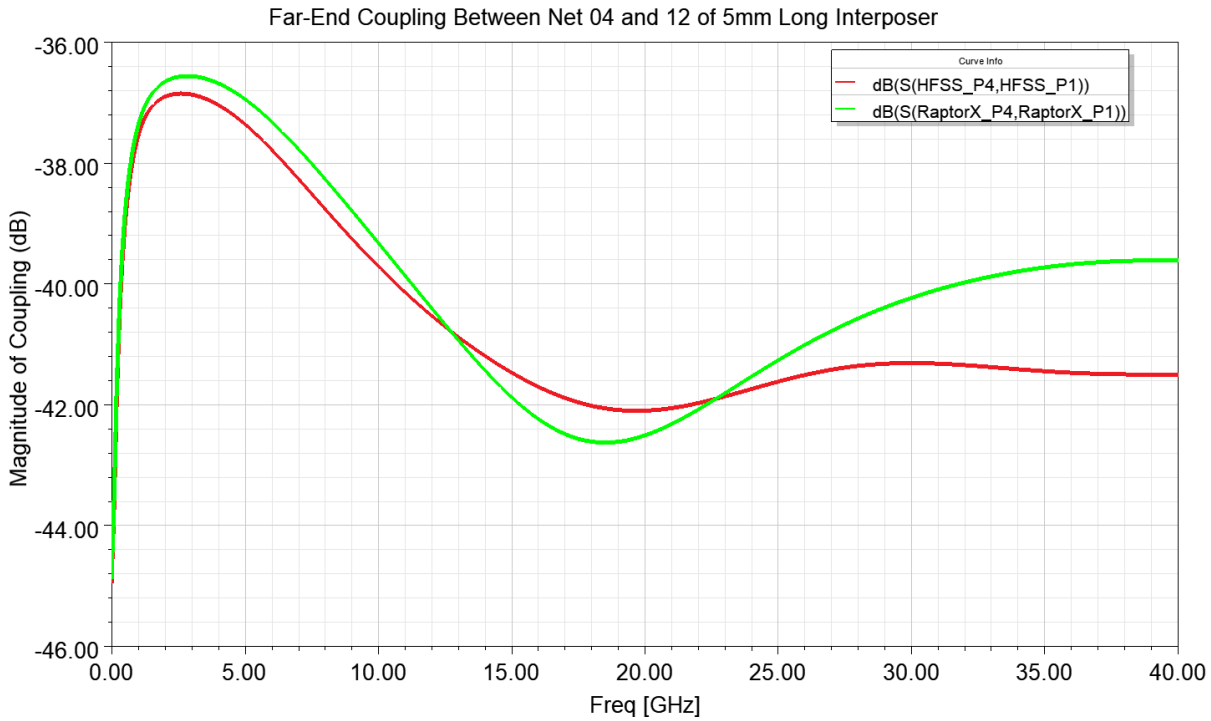
RaptorX





RaptorX vs HFSS: Coupling of Net04 and Net12

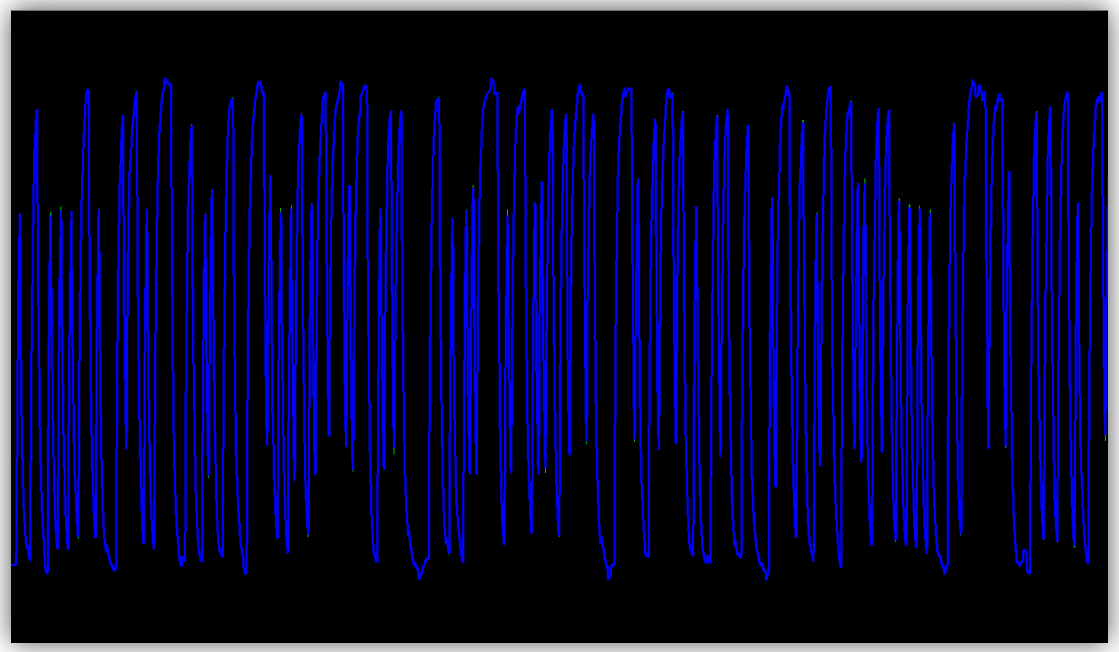




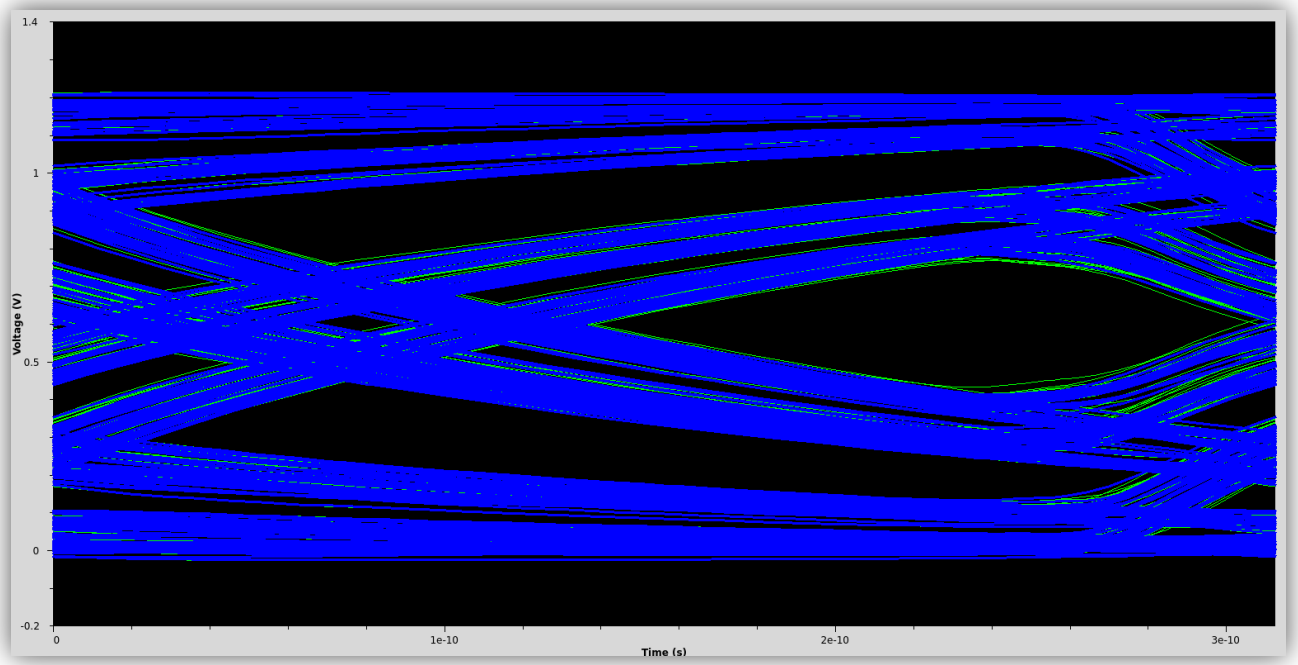
HFSS

RaptorX

Circuit simulation results at termination



Waveform



Eye diagram

HFSS — RaptorX

Excellent correlation of output waveform and eye diagram

Solving the SI problem in System Design

Deep-dive on Ansys system-centric SI analysis workflow with HFSS

Ansys

Key Capability: Gold Standard Accuracy, Reliability

HFSS is accepted as the industry gold standard for accuracy

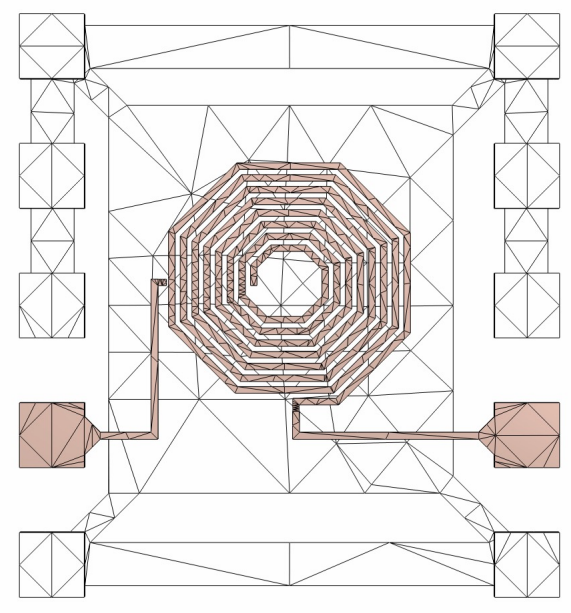
- This begins with automatic **adaptive** meshing

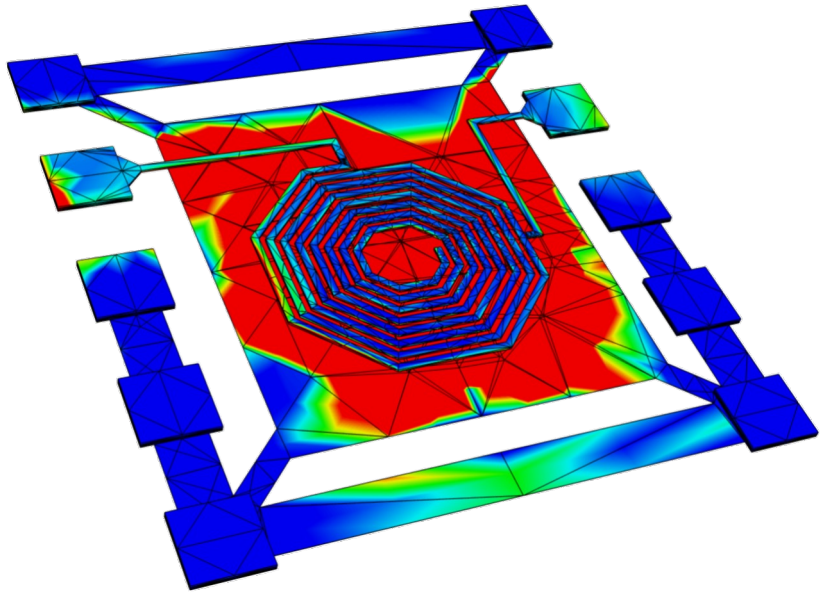
Mesher and solver work hand in hand to…

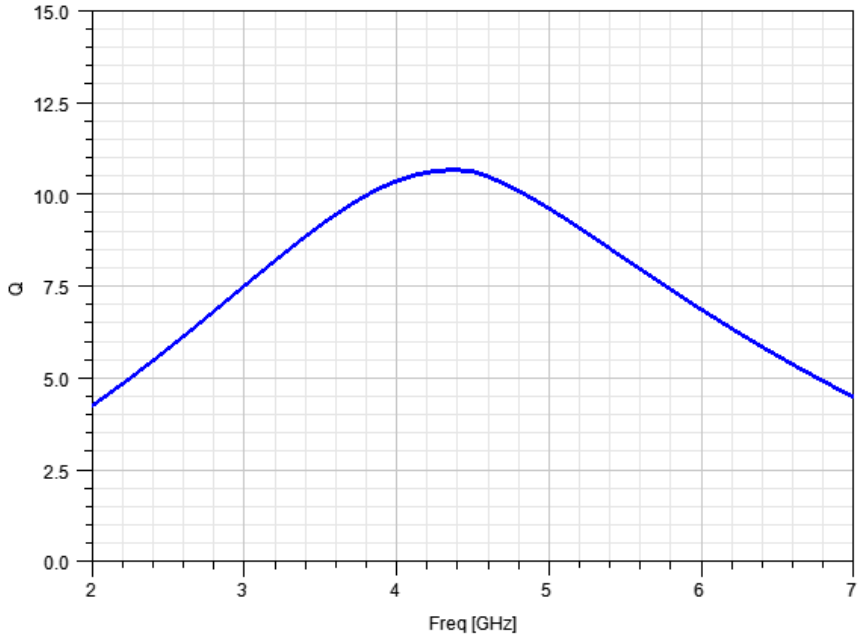
- Determine mesh distribution: **Efficiency**
- Represent the electromagnetics: **Accuracy**

The physics defines the mesh,
the mesh does not define the physics

- Provides accurate and **reliable** solutions
- Generate final designs through simulation
- Eliminate prototypes, time and cost

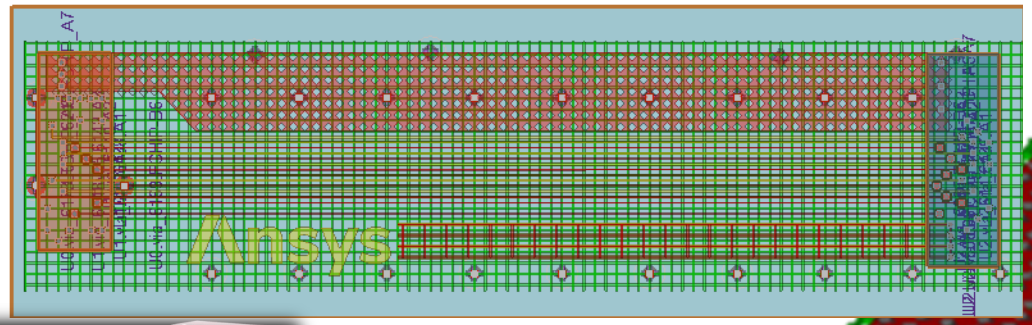


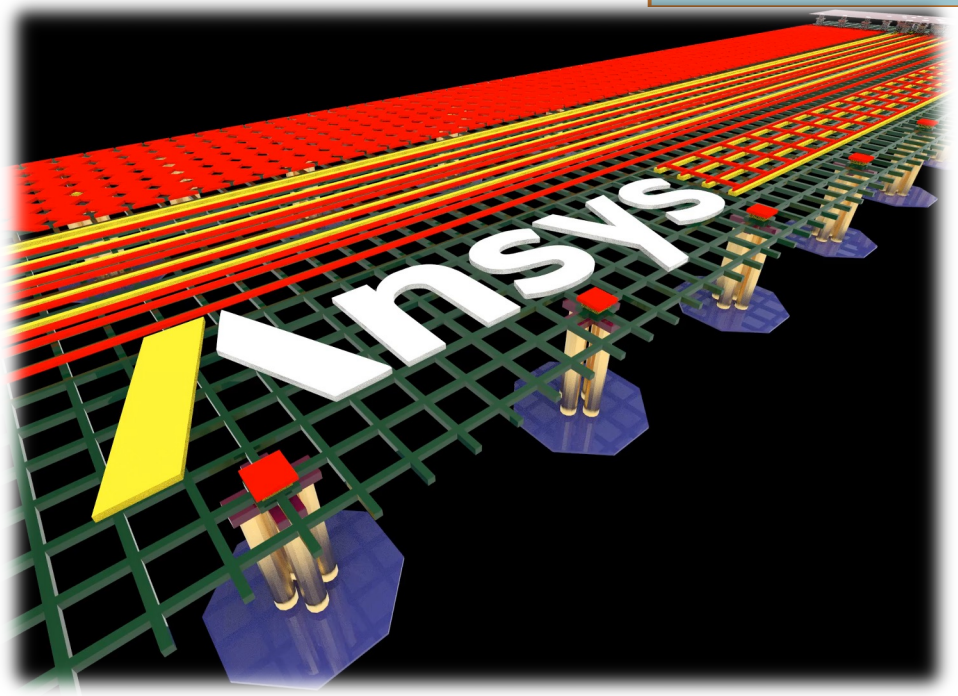




Interposer Design

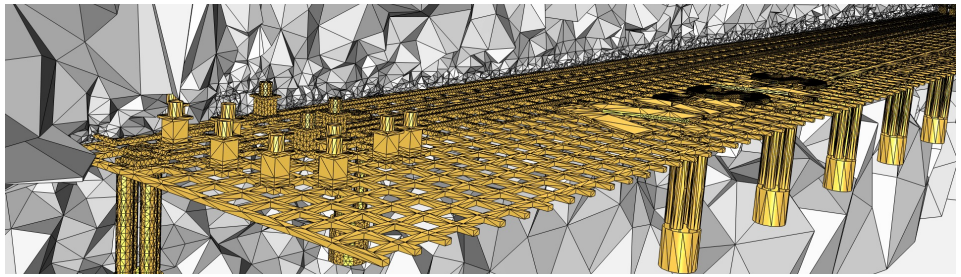
- Includes TSVs with 300nm SiO_2 outer layer
- Parametric design
- Power and signal nets

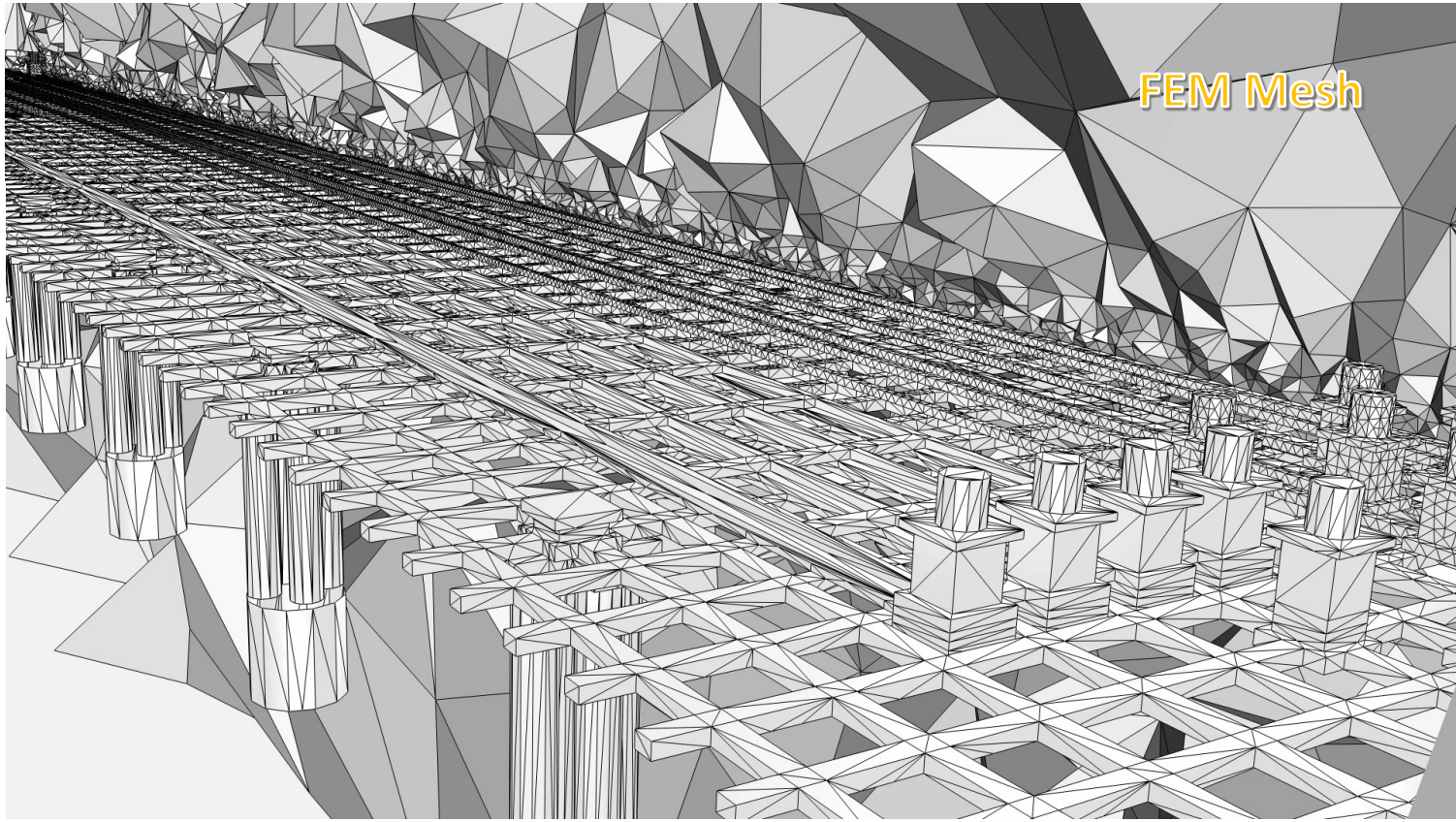


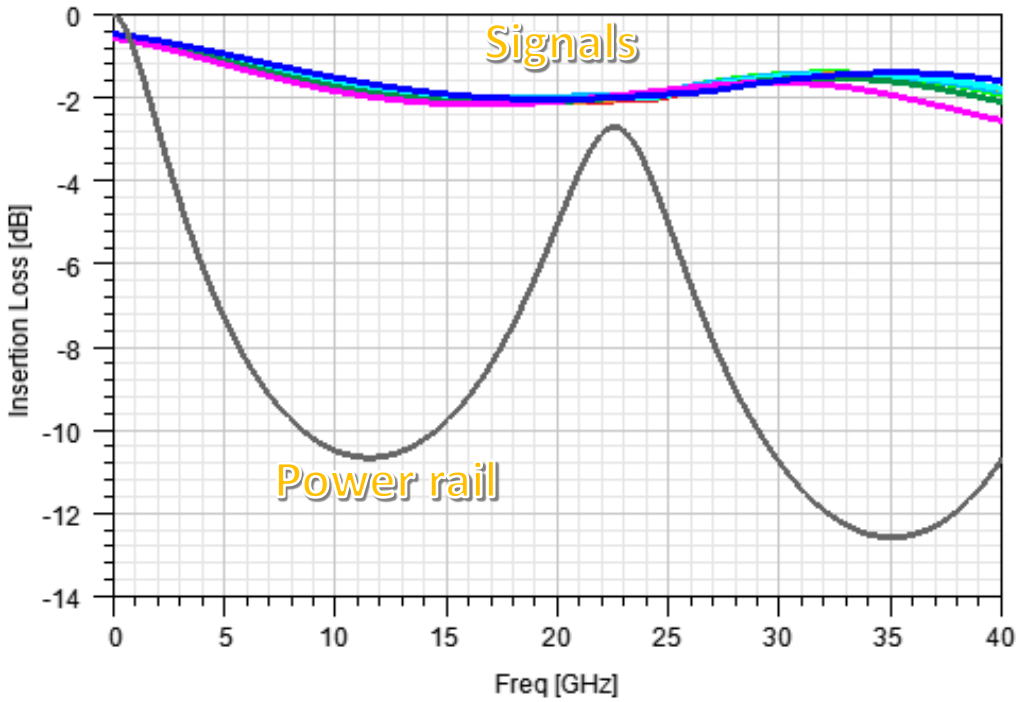


HFSS simulation

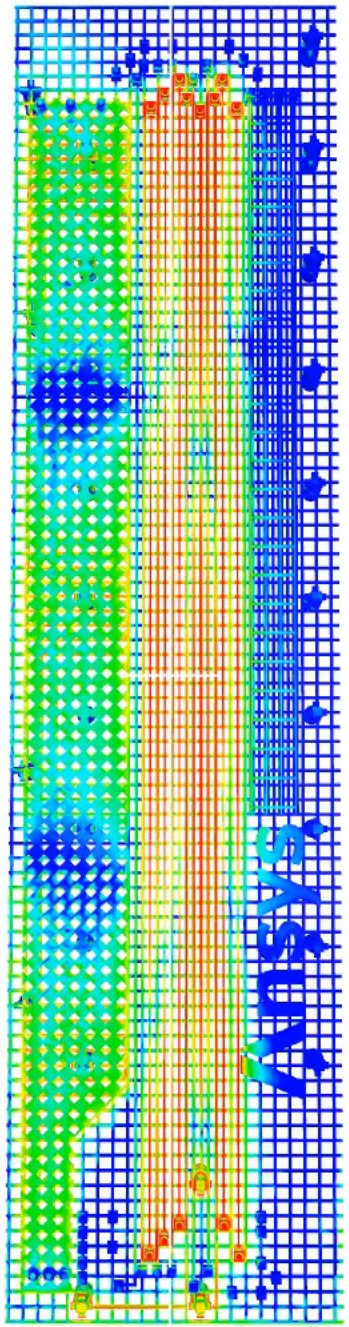
- Adaptive frequency 10 GHz
- Sweep from 0 to 40GHz
- Simulation time: 16m 31s
  - 10 nodes with 32 cores each







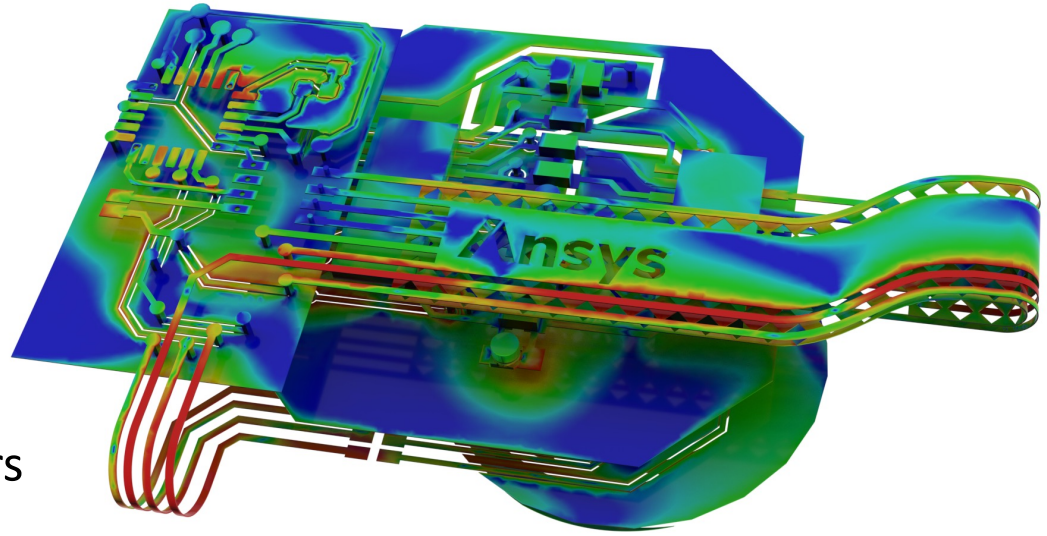
Electric Field at 100GHz



Interposer Optimization

HFSS 3D Layout

- Dedicated HFSS design type for IC, Packages and PCBs
- Full 3D finite element simulation of layered structures
  - Same 3D meshing and FEA simulation as HFSS 3D
- HFSS 3D Layout Ease-of-Use
  - Multi-technology hierarchy
  - Layer stackup, nets, via padstacks,
  - Components and Component libraries
  - Automated port creation
- HFSS 3D Layout has multiple solvers
  - HFSS 3D Layout includes SIwave and planar EM MoM solvers
  - Integrated with Nexxim time domain circuit simulation

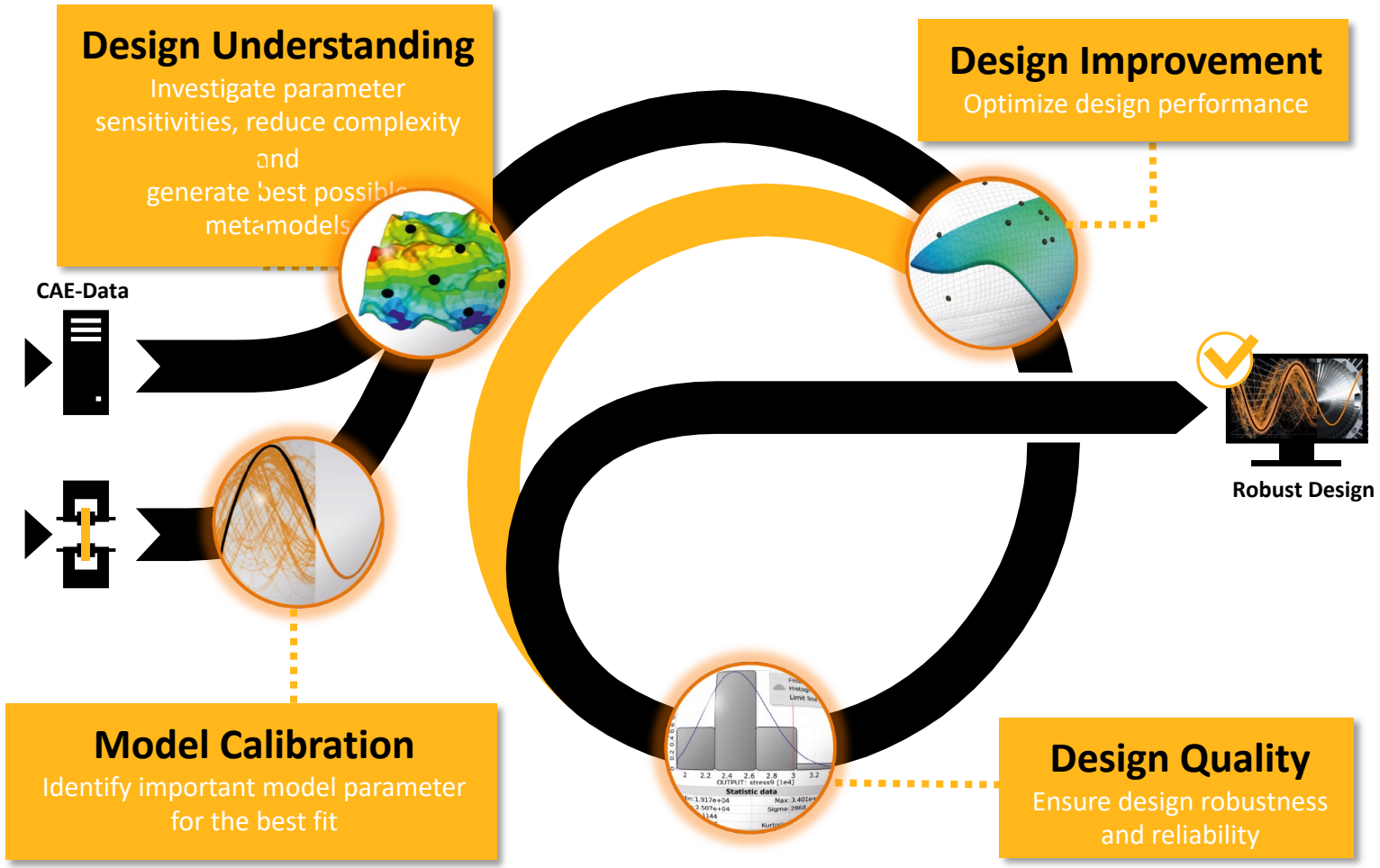


Ansys optiSLang: *Power of Variation Analysis*

- **Understand your design sensitivity**
  - Which parameters influence what?
  - Which constraints and goal conflicts do I need to address?

- Metamodeling **machine learning**
  - Metamodel of Optimal Prognosis" (MOP) : A supervised ML technique which detects the important input variables and determines suitable regression functions

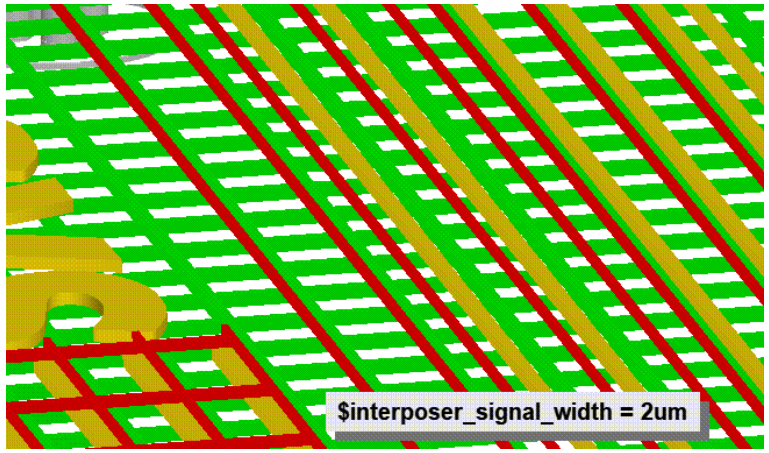
- **Robustness/Reliability** module to address:
  - Robust Design Optimization (RDO),
  - Uncertainty Quantification (UQ),
  - Design for Six Sigma (DfSS)

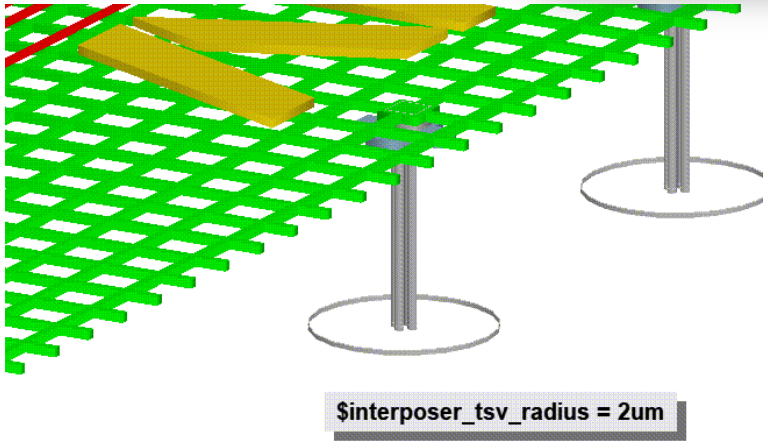


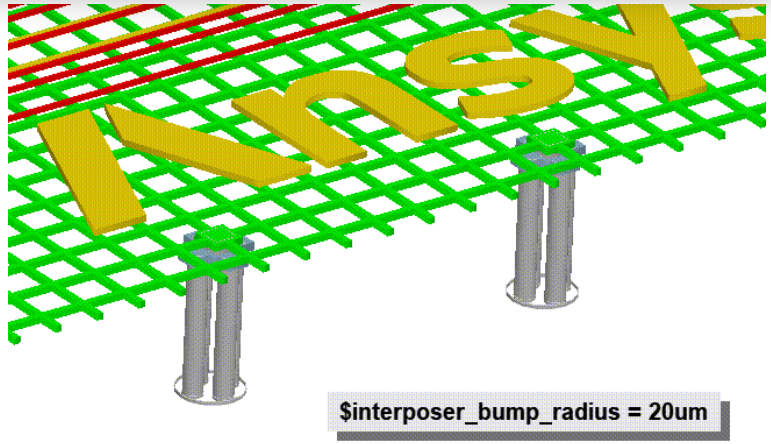
HFSS 3D Layout Parametric Design

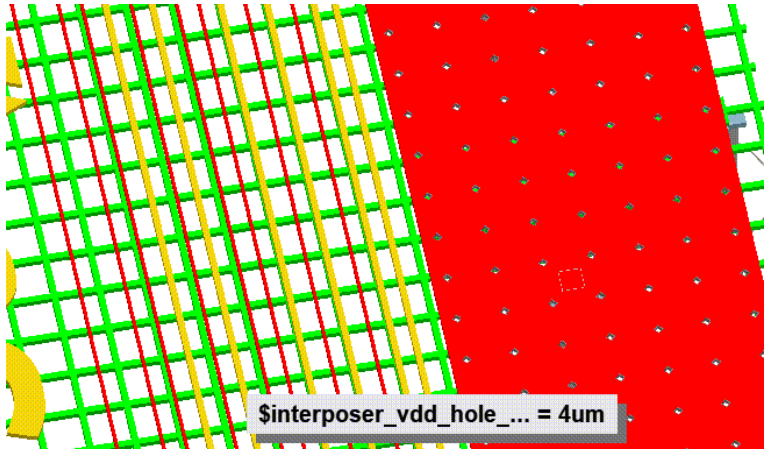
- Six variables were created
  - Easily create parametric variables on any layout

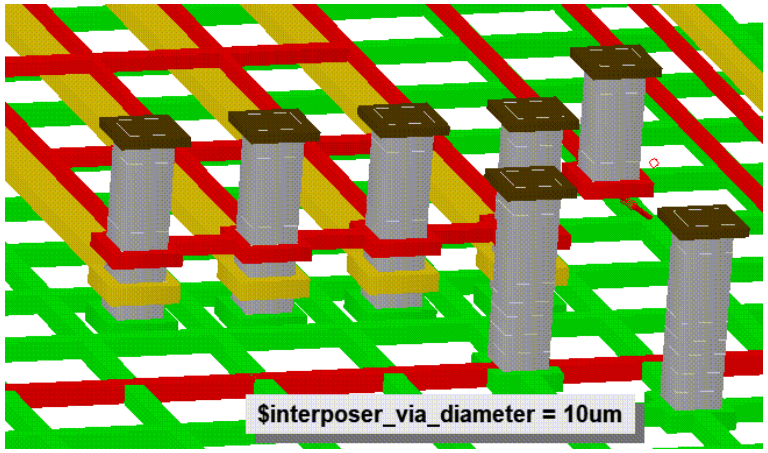
	Activation	Name	Parameter type	ence	Constant	Value type	Resolution	Range		Range plot
1	☑	_interposer_bump_radius	Optimization	40	☐	REAL	Continuous	20	60	
2	☑	_interposer_signal_width	Optimization	2	☐	REAL	Continuous	2	8	
3	☑	_interposer_tsv_radius	Optimization	6	☐	REAL	Continuous	2	8	
4	☑	_interposer_via_diameter	Optimization	14	☐	REAL	Continuous	10	18	
5	☑	_interposer_vss_width	Optimization	4	☐	REAL	Continuous	4	20	

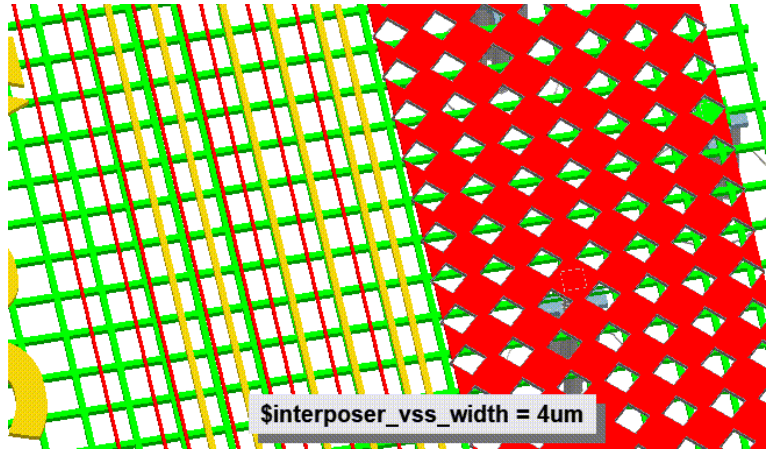




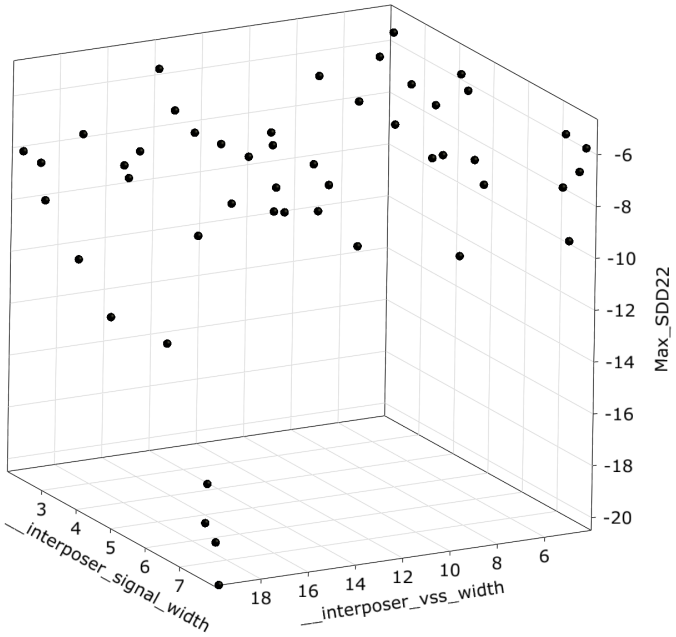


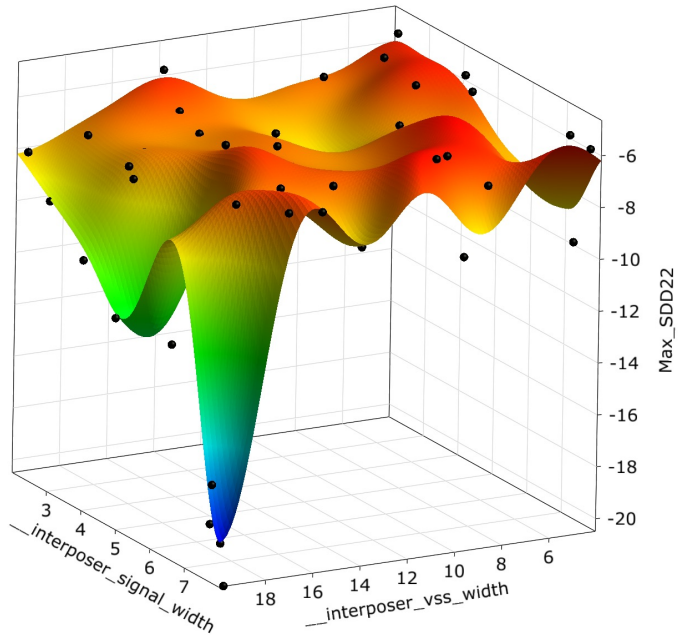


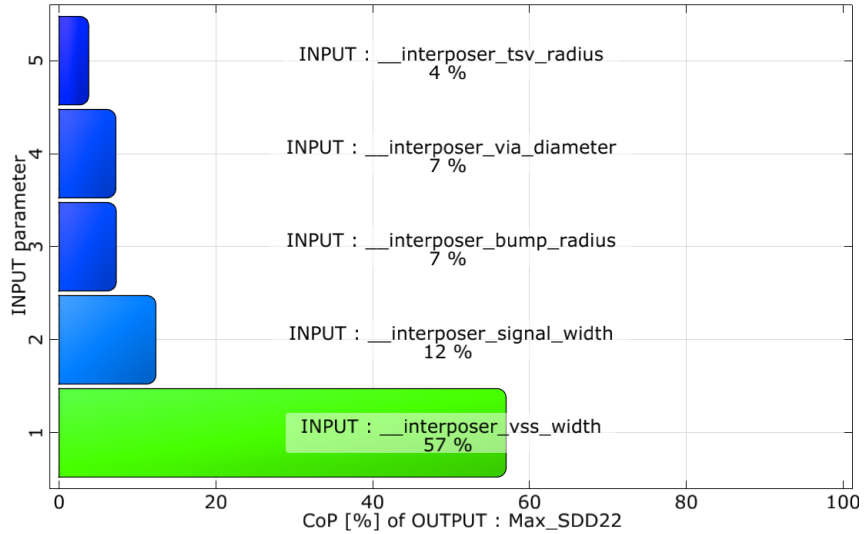




Sensitivity Analysis in optiSLang







- **optiSLang** creates design of experiments, DoE
- HFSS 3D Layout evaluate design points

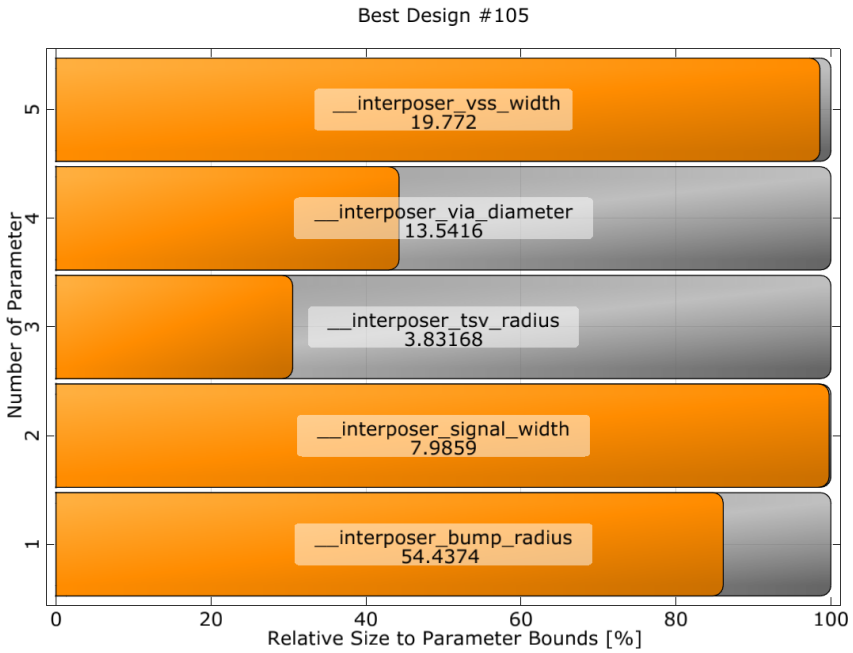
- **optiSLang** fits a metamodel of optimal prognosis (MOP) to results.
- Using ML MOP, quickly study design space without requiring HFSS to evaluate additional design points

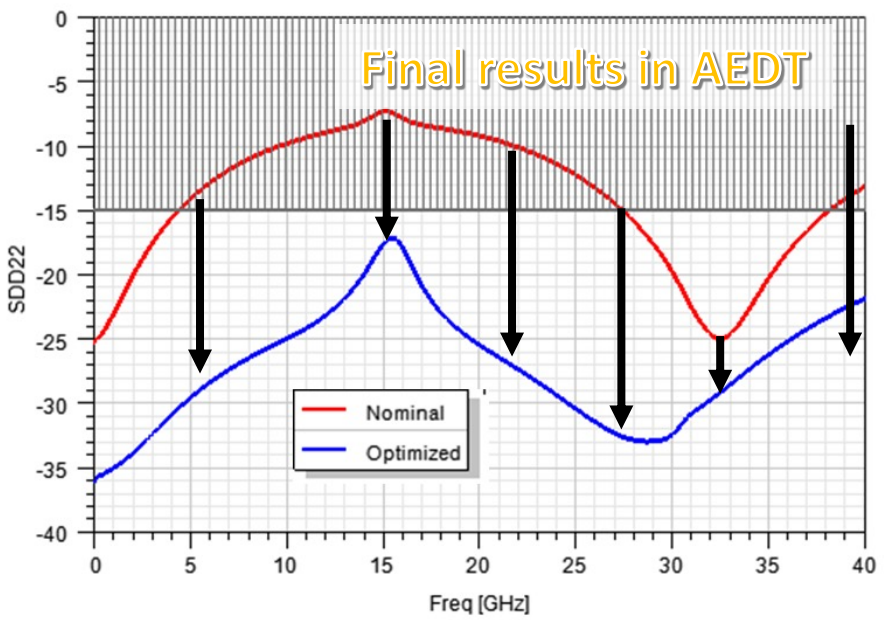
- **optiSLang** determines the sensitivity of the device to the input parameters:
  - Small changes in what input parameters will cause the largest change in the response?
  - Which input parameters have minimal impact on response and can be ignored

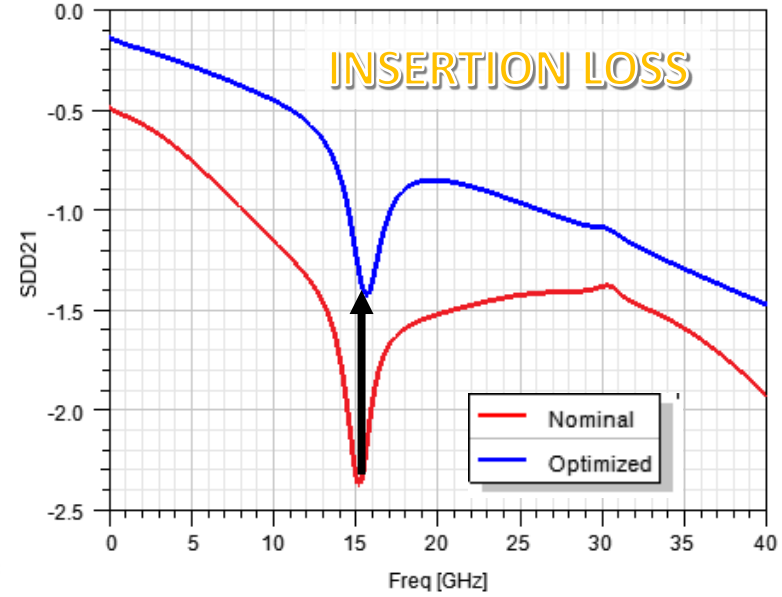
Sensitivity Analysis Results in optiSLang

- Final design shows a 10dB improvement over initial, achieving the target of <-15dB

- Additional optimization can be performed to optimize the results even further



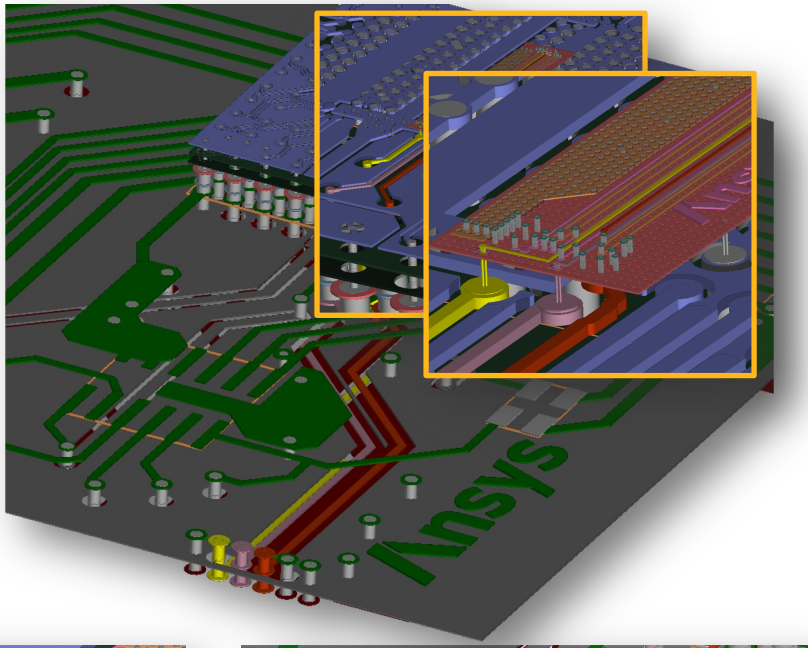


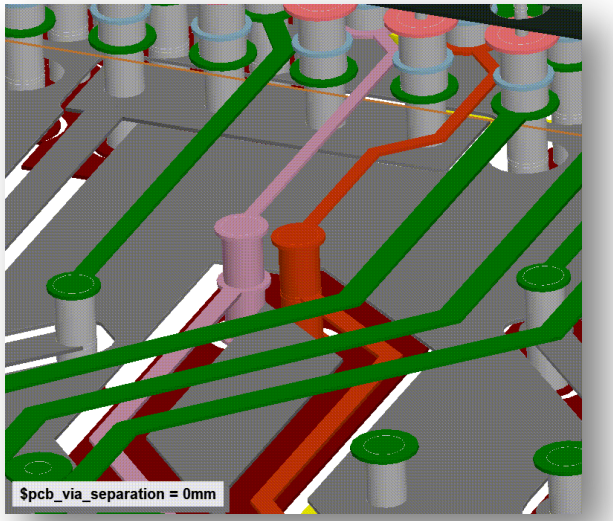


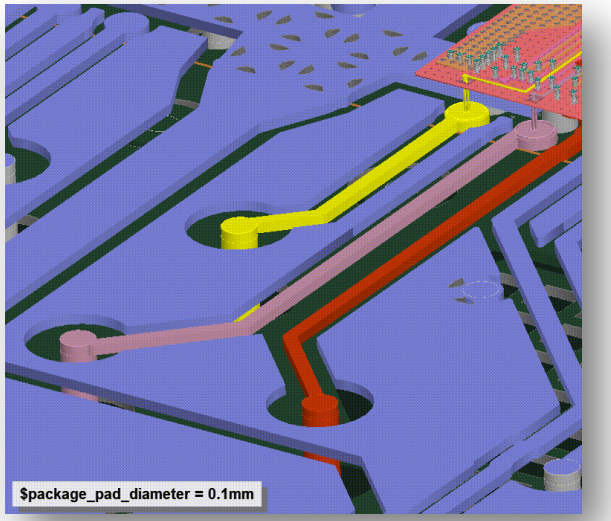
Optimizing Interposer on Package on PCB

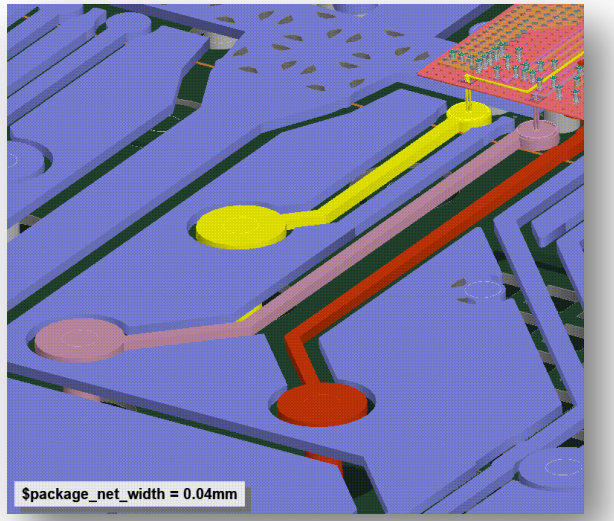
Interposer on Package on PCB Optimization

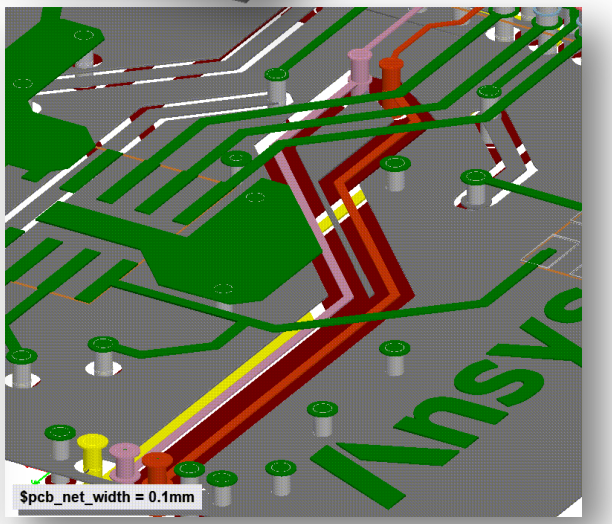
- Use the interposer sensitivity information from the optiSLang to optimize the entire system
- Parametric variables on package and PCB
  - Routing
  - Pad size
  - Package trace width
  - PCB trace width





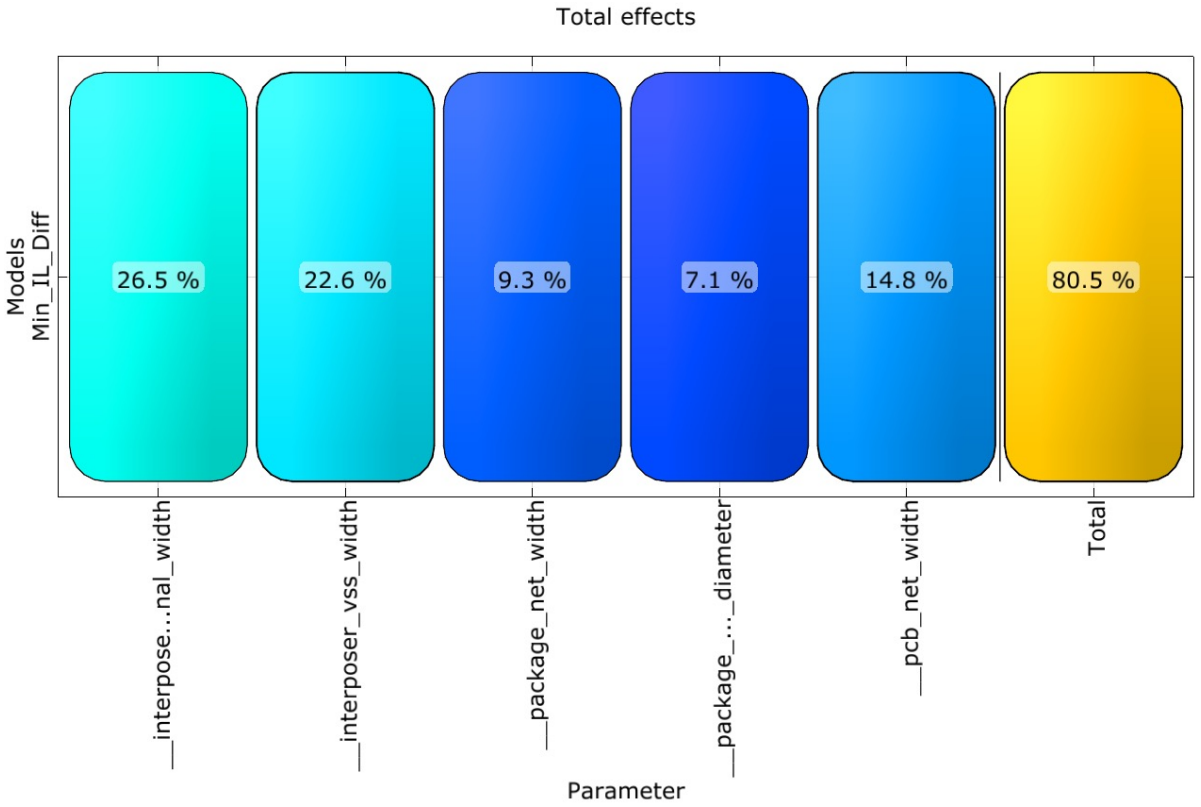


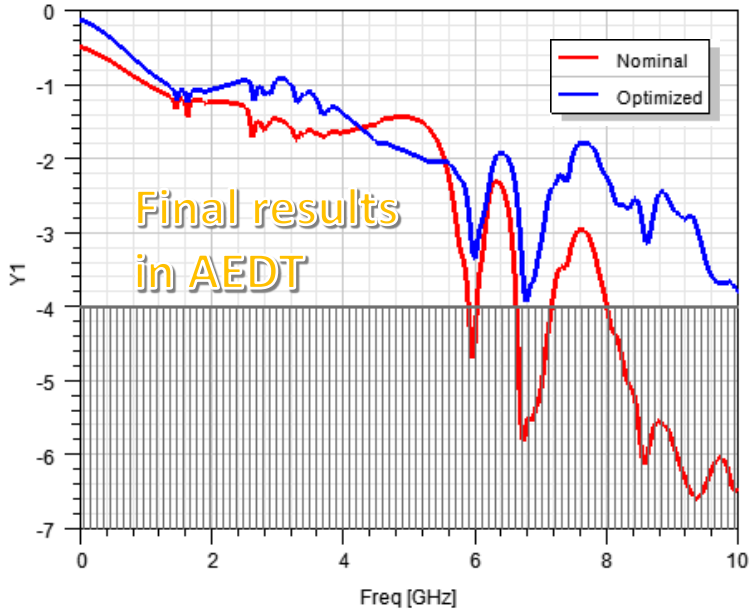


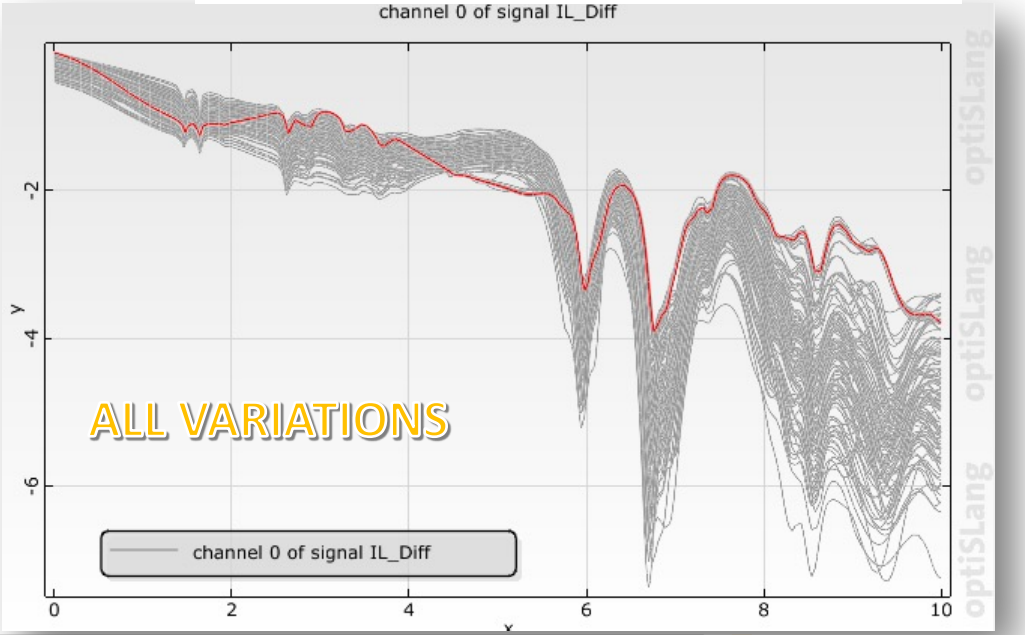


Interposer on Package on PCB Optimization

- Coefficient of Prognosis shows that interposer *VSS* and *signal widths* and *PCB net width* strongly affects IL

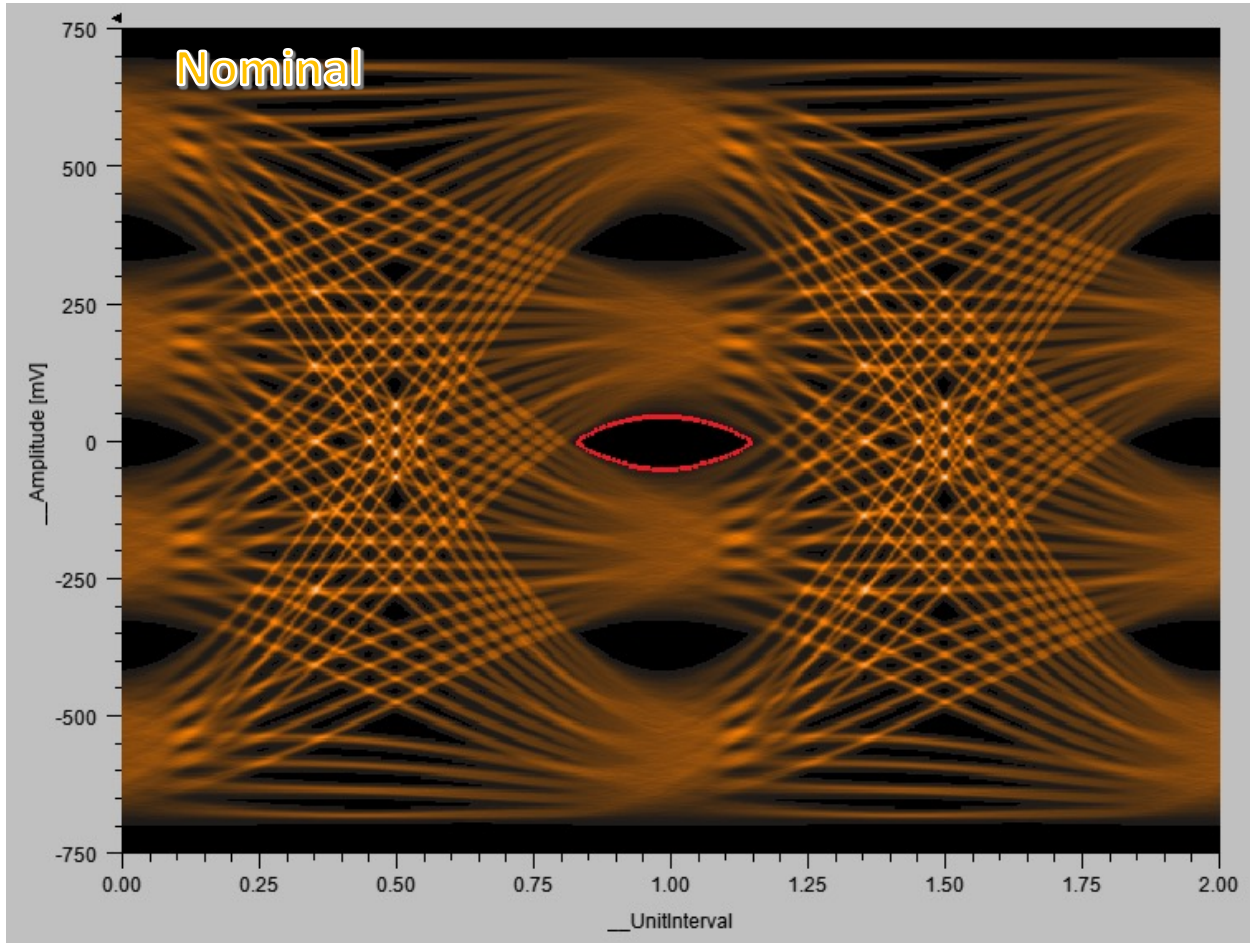


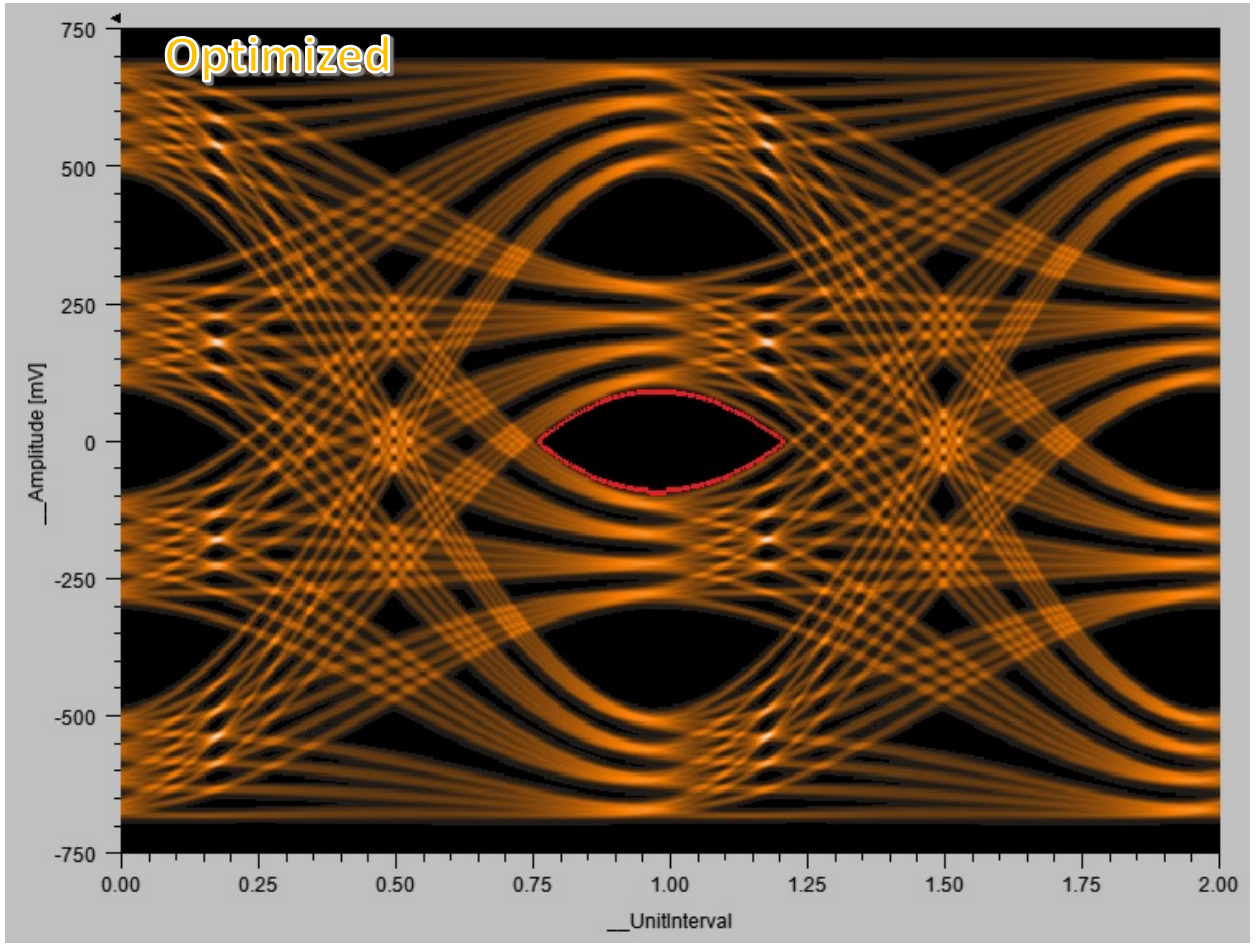




Interposer on Package on PCB System results

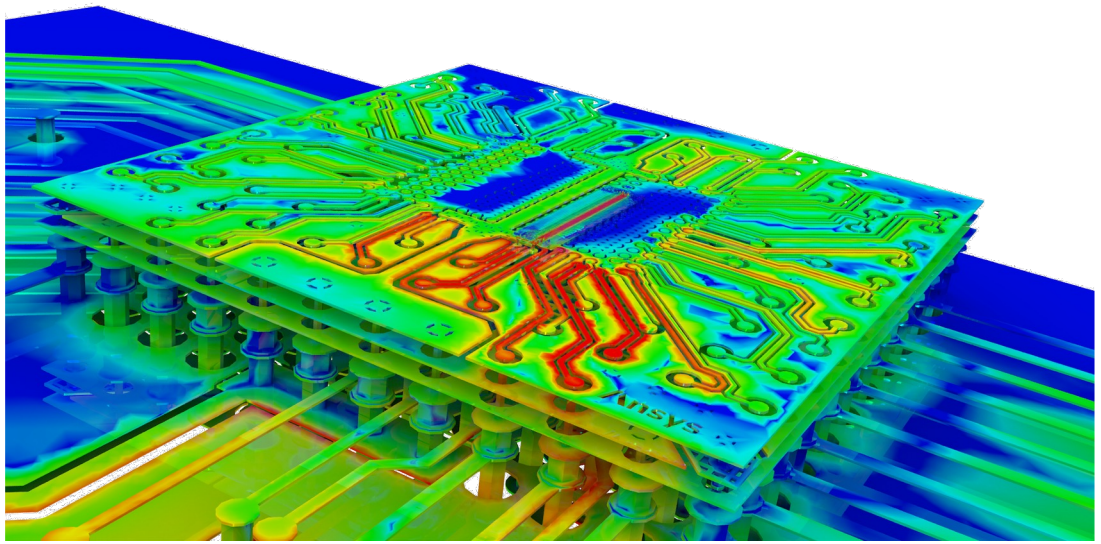
- PAM4 IBIS AMI models generated by Ansys SPISim evaluate signal integrity

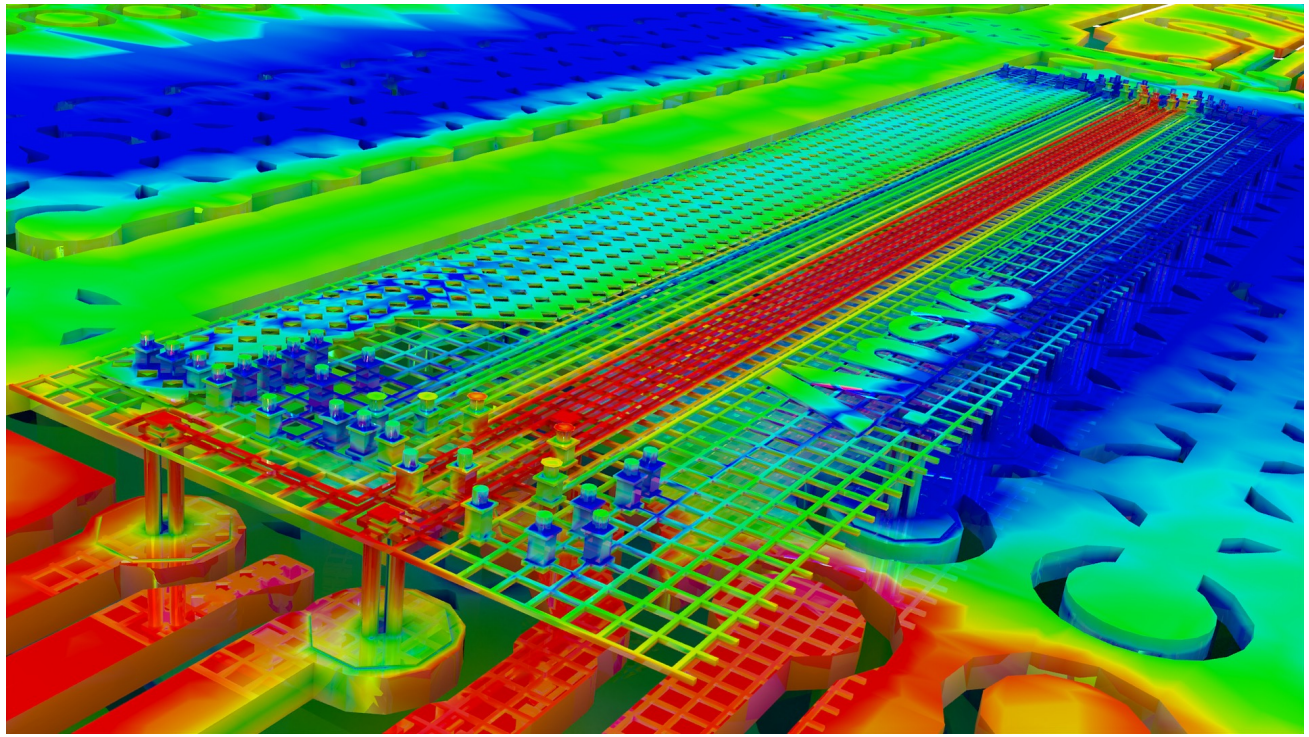


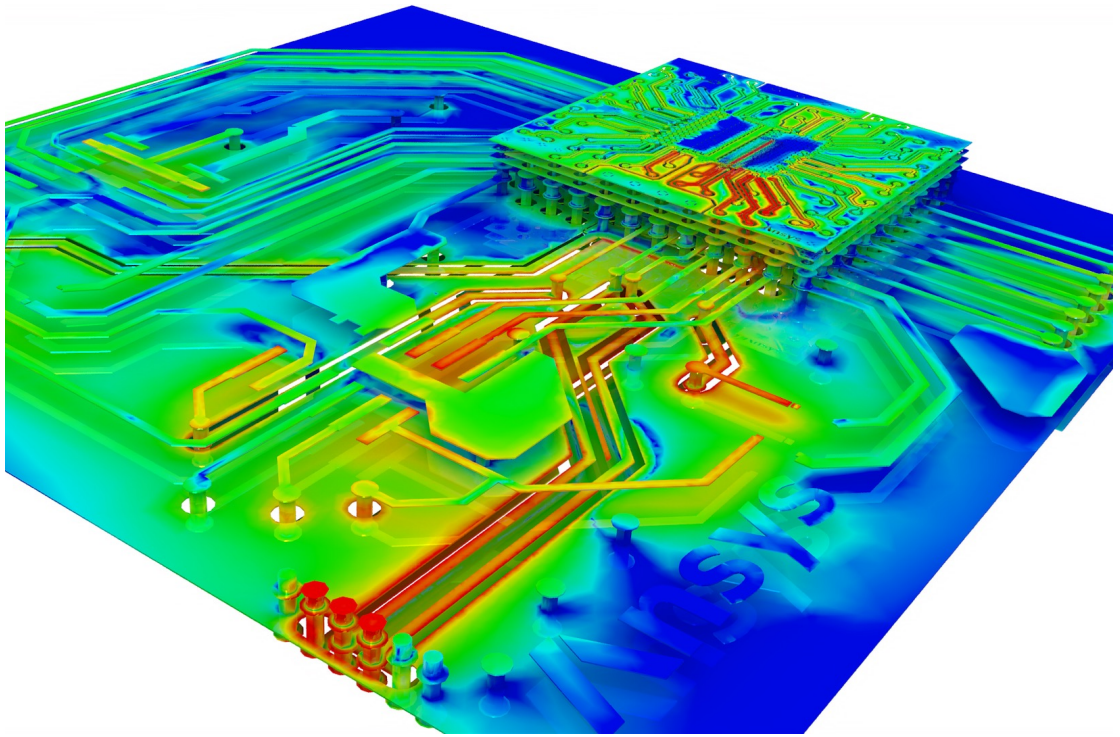


Final sign-off

- For a final sign-off, HFSS is used to simulate the entire system in a single fully coupled full wave simulation using Mesh Fusion







Conclusions

Simulate Early for Future Success

- Interposer design require multidisciplinary approach to extract the best performance
  - Analyze the different parts of the heterogeneous design as one

- SPICE-only signoff with separate EM analysis after failed fabrication and testing no longer a market or economically viable option
  - Signoff on circuit design with SPICE analysis is a standard approach
  - Must be expanded to include a full electromagnetic signoff

- **Simulate early with electromagnetic accuracy to predict success!**

- **Ansys rises to the challenges and delivers golden accuracy with chip- and system-centric design flows**


Ansys

COPYRIGHT NOTICE

MEPTEC
THE NEXT GENERATION