



Road to Chiplets: Design Integration

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Advanced Packaging Design Platform for Chiplets and Heterogeneous Integration

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Outline

- ❖ **Motivation**
 - Semiconductor trend and Chiplets Integration
- ❖ **Advanced Packaging Technology Platforms**
 - Introduction of advanced packaging technology solutions
- ❖ **ASE Design Platforms for Chiplets & Heterogeneous Integration**
 - Design platform & Packaging design kit
 - Electrical performance validation
- ❖ **Summary**

Key Semiconductor Growth Drivers

IoT/IoE



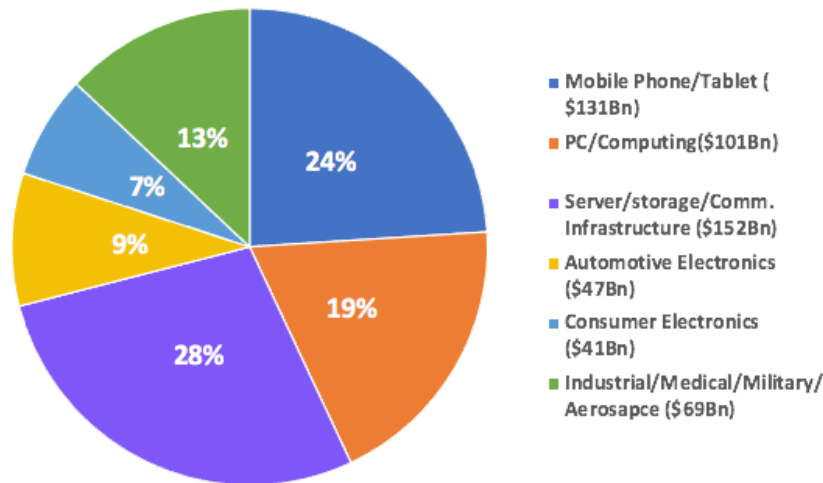
Automation



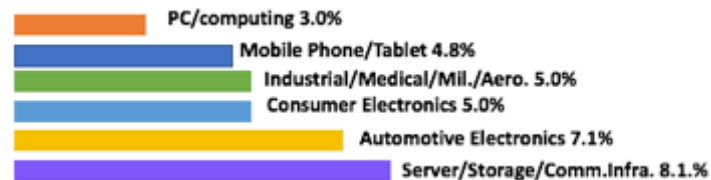
5G/Edge



2024 Semiconductor Market Forecast



CAGR 2019~2024



Source Prismark 2020 in IMAPS

HPC



Smart Everything

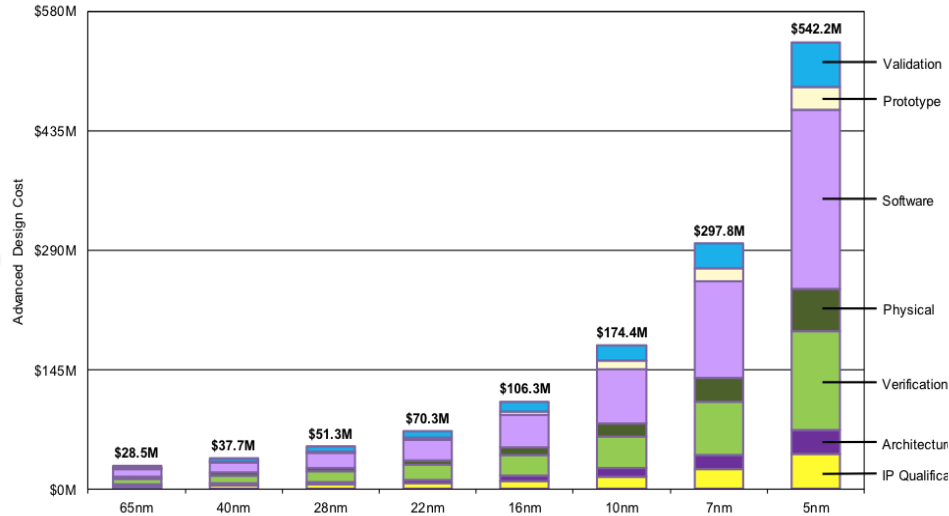


AI/ML



Barriers & New Technology Innovation Drivers

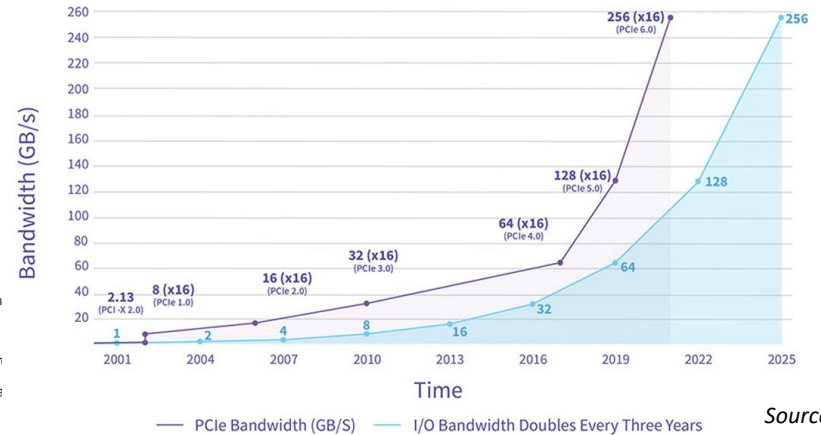
Si Node Dev Cost



Source: IBS

High performance requirement

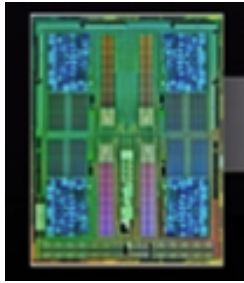
I/O Bandwidth Doubles every 3 years



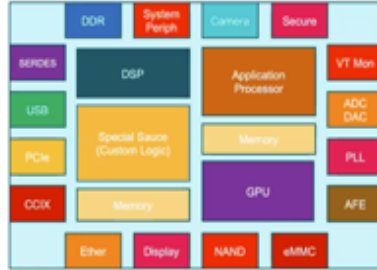
Source: PCI-SIG

Chiplets and Heterogeneous Integration

- **New Logical partitioning and Disaggregated SoC**
- **Heterogeneous integration offers a solution for performance scaling following Moore's Law**



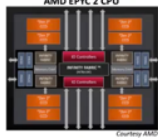
Monolithic SoC



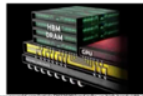
Modularized SoC (Chiplets)

- ☐ Mix & Match systems--*Different Si Nodes*
- ☐ Reuse IPs
- ☐ System flexibility--*Processors, accelerator*
- ☐ Performance optimization--*Low latency & high BW*
- ☐ Time to Market
- ☐ Low Cost

Split by function: I/O and Memory Controller



Combination of functions: Compute & Memory



Combination of functions: Compute & Accelerator



Source: IBM ECTC 2020

Outline

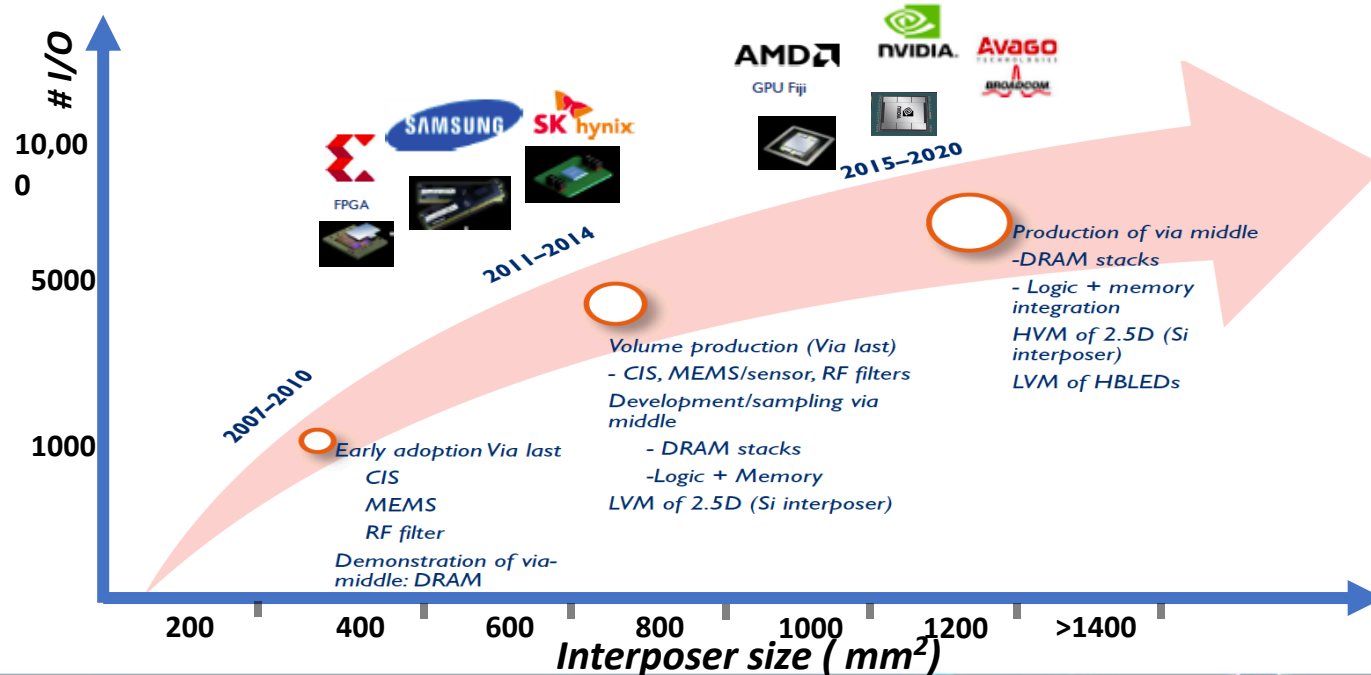
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Advanced 2.5D Si Interposer Packaging Technology

➤ 2.5D Si TSV Technology Development Milestones

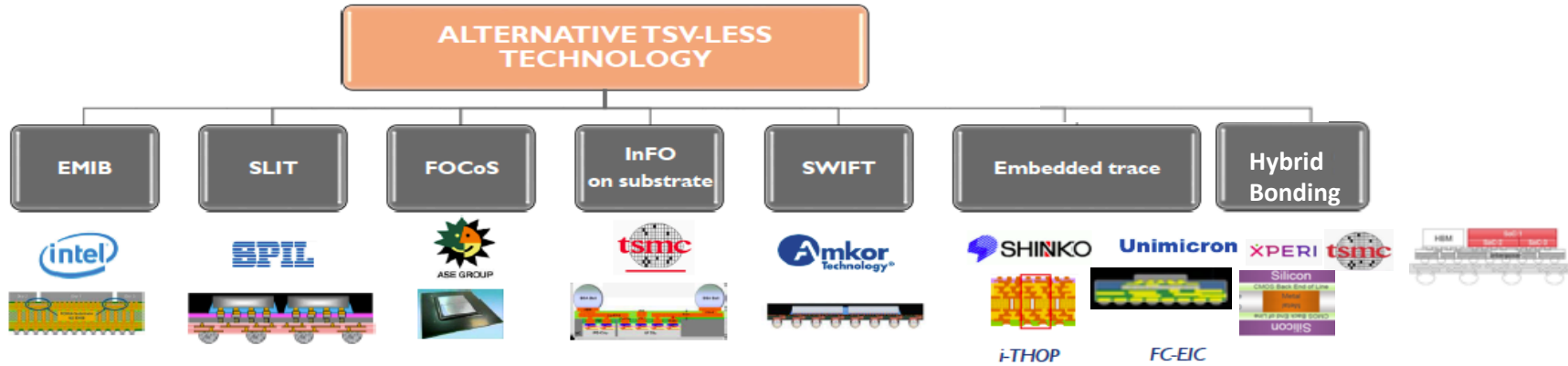
- Enable chip-partition for heterogeneous Integration to support Moore's Law extension
- Scale-up function and performance for AI/deep learning and HPC in HVM for over 10 years

➤ High Cost for 2.5D Si TSV interposer

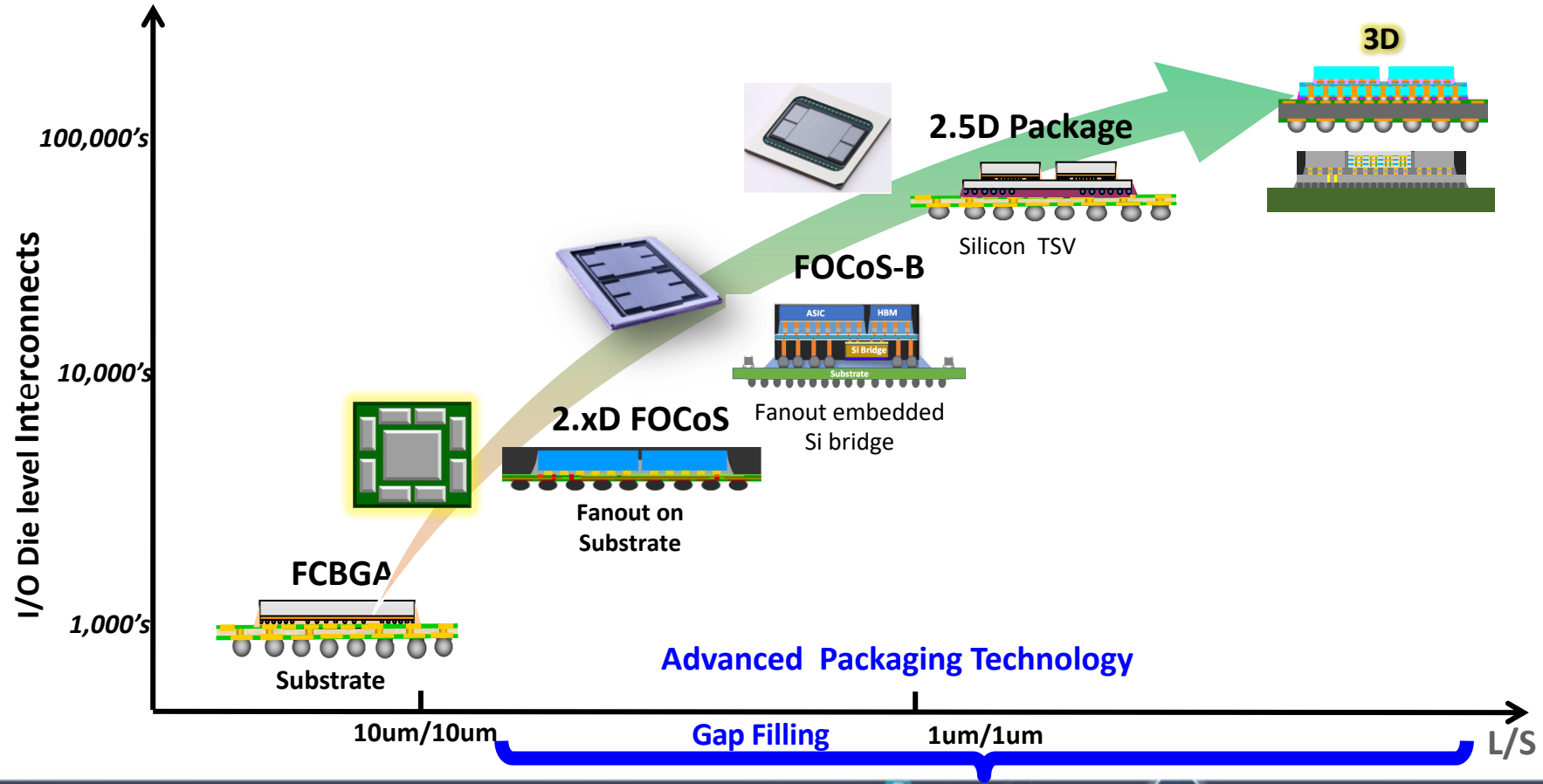


Advanced HD Fanout and 3D Packaging Technology

- **Alternative Si TSV-Less or RDL interposer solutions to reduce cost**
 - Embedded Si die to replace large Si interposer
 - Fanout RDL interposer with $L/S > 1/1\mu m$
 - Better electrical performance (less insertion loss) due to no Si TSV
- **3D Hybrid bonding for higher interconnect density**

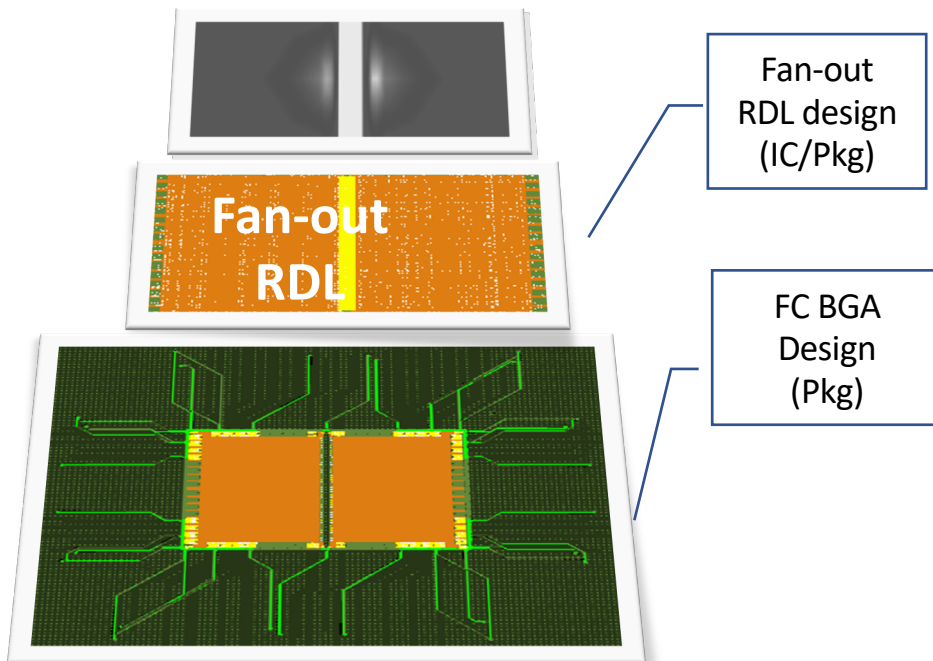


ASE Advanced Packaging Technology Platforms

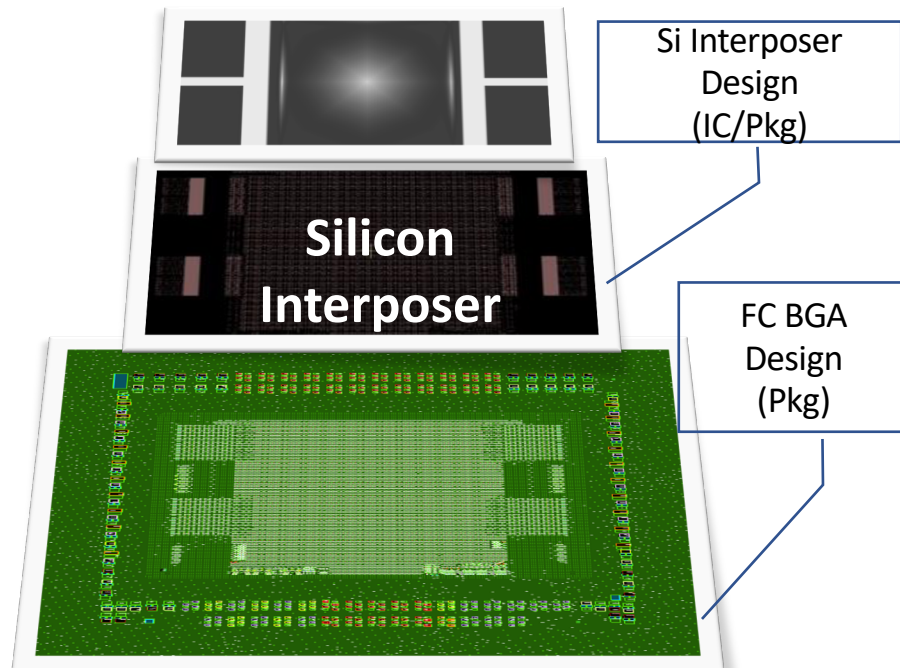


Hybrid Design of Advanced Packaging for Chiplets Integration

❑ Fan-Out Chip on Substrate (FOCoS):



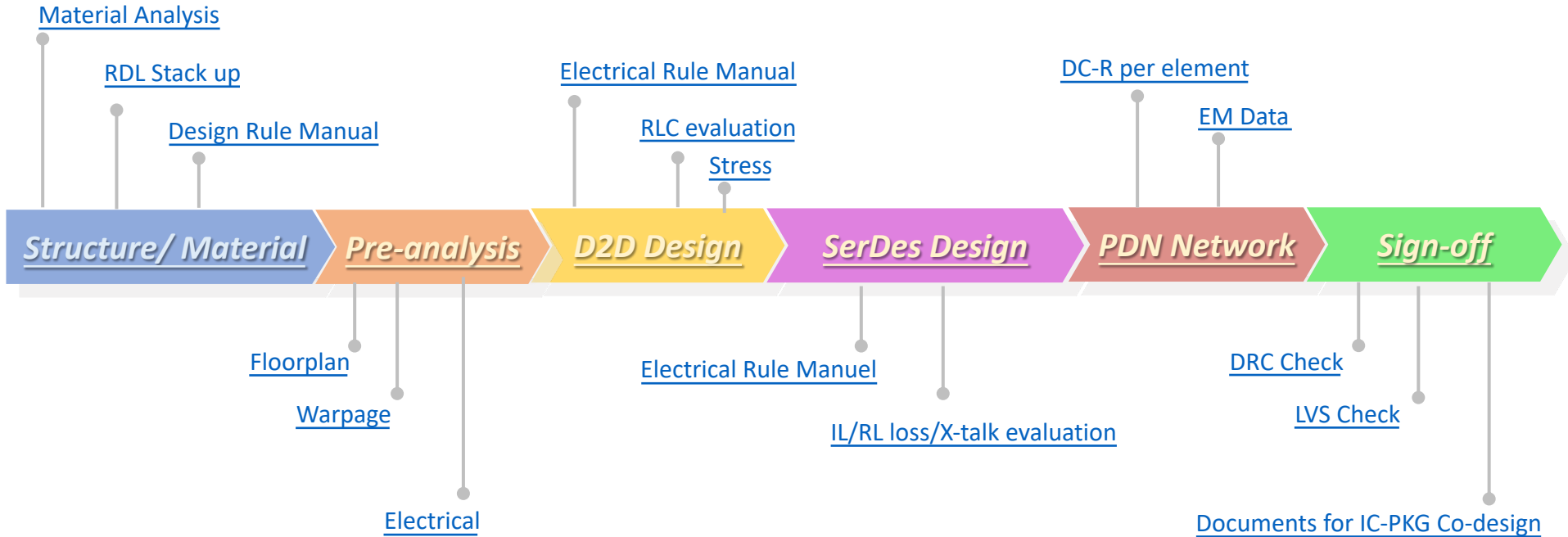
❑ 2.5D Package:



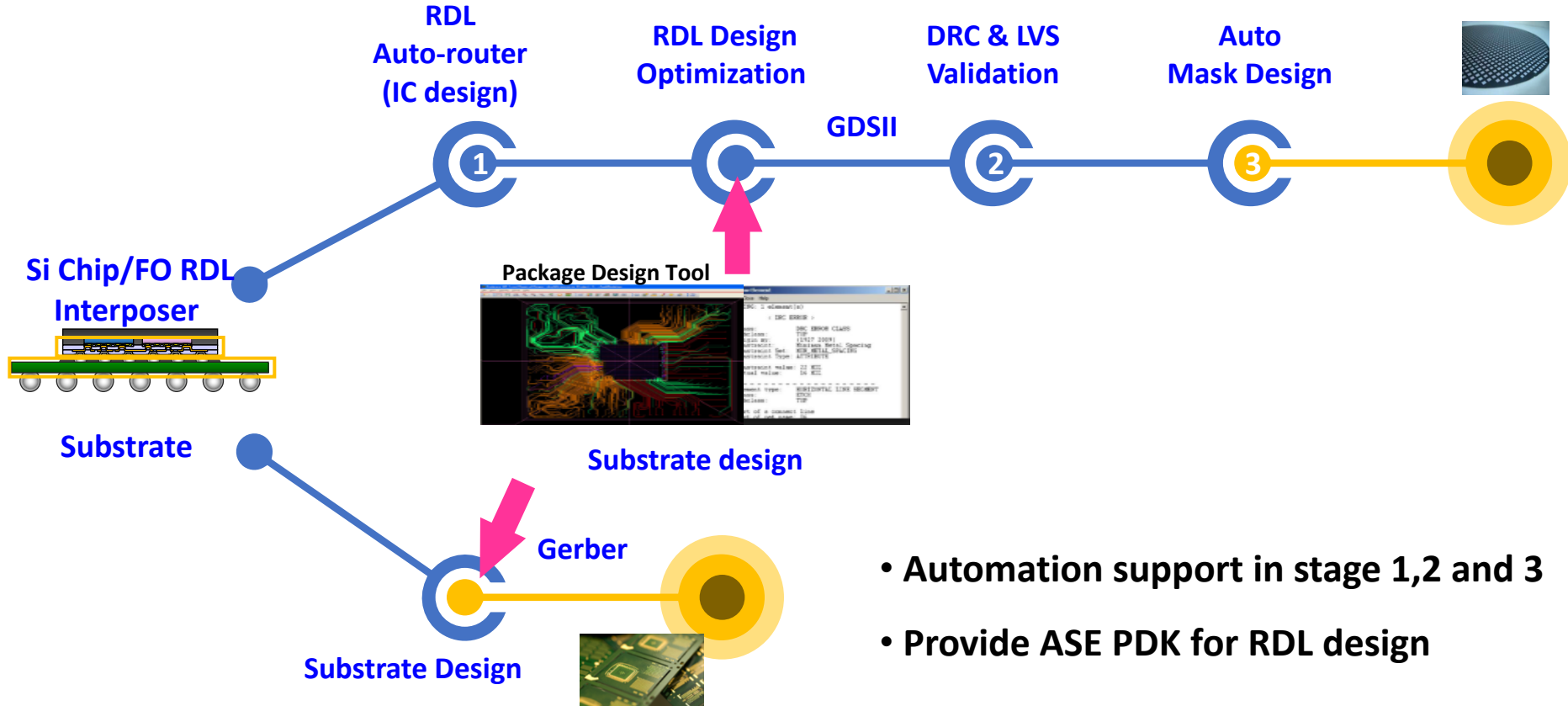
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ASE Advanced Packaging Design PDK

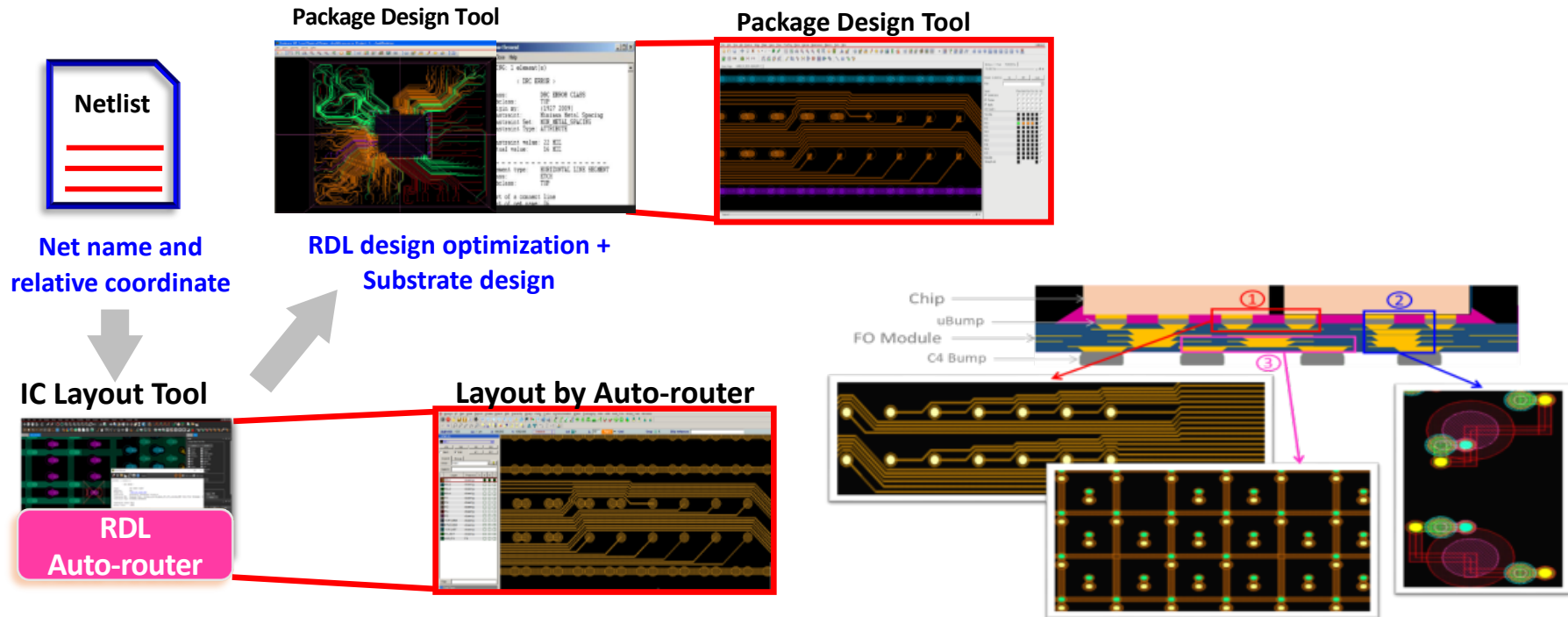


ASE High Density FOCoS Hybrid Design Flow



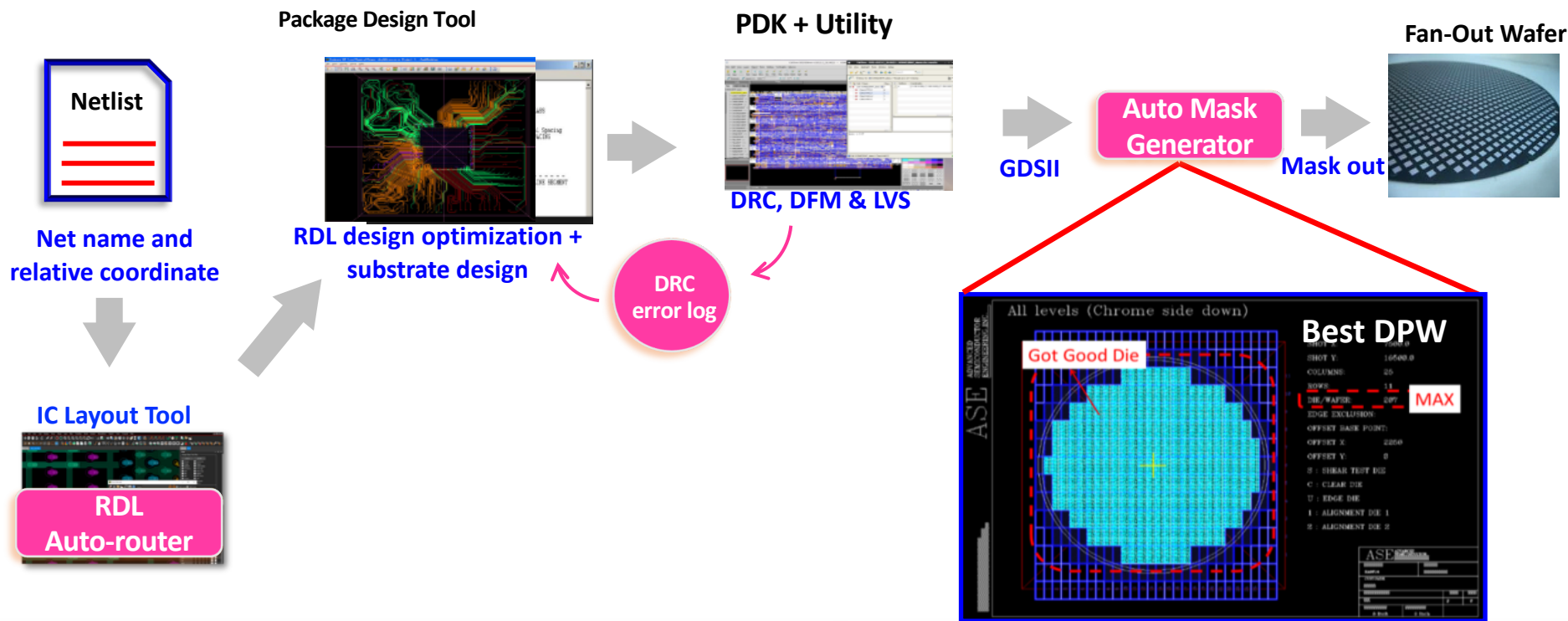
ASE High Density FOCoS Hybrid Design with RDL Auto-router

- More than 50% layout cycle-time saving by auto-router compared to conventional packaging design
- Auto-router can be used for D2D, ubump (chip to FO) and C4 bump (FO chip to substrate) design



ASE High Density FOCoS Hybrid Design with Auto-mask Generator

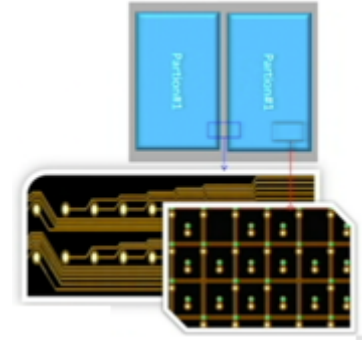
- Design lead-time from 3 days to < 1hr
- Best DPW (for large FO Die)



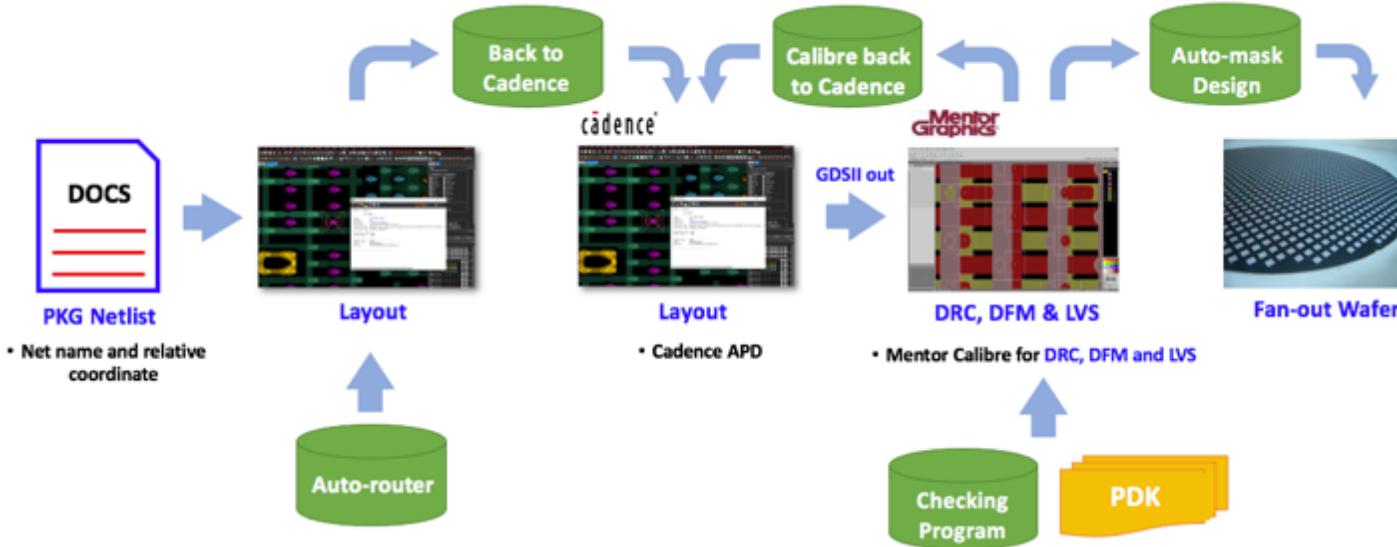
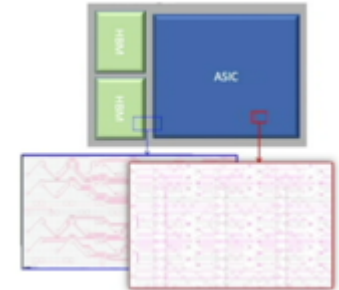
ASE Advanced Packaging Hybrid Design Solutions

- Homogeneous Design & heterogeneous Design
- Speed up design C/T: 50% C/T saving by Auto-router

- Homogeneous Design
ASIC+ASIC; FO: 27.5x22.5mm²
4RDL 2/2um

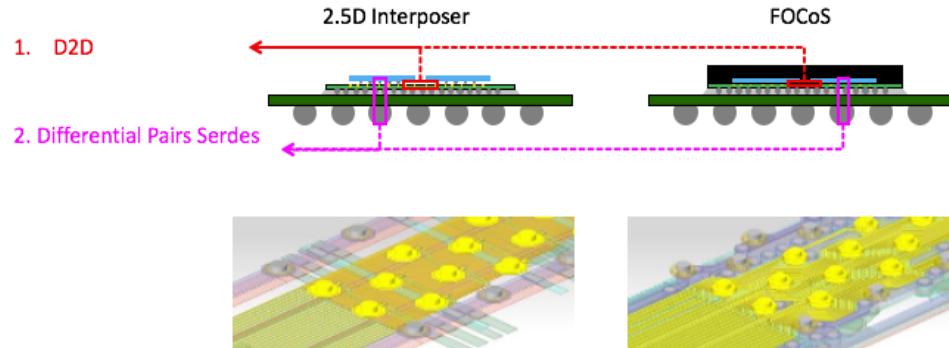
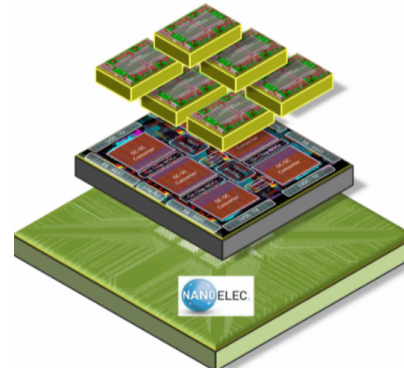


- Heterogeneous Design
ASIC+2 HBMs; FO: 45x25mm²
4RDL 2/2um



Signal Integrity and Power Domain Network

- **Many different Die to Die interconnects**
 - Serial I/O (XSR), Serdes—56Gb/s PAM4;
 - Parallel I/O (BoW, openHBI, UCIe)
- **Optimization for SI**
 - Low insertion loss
 - High frequency, high speed and high bandwidth
- **PDN optimization**
 - Low Power (<1pj/bit)
- **Critical I/O**

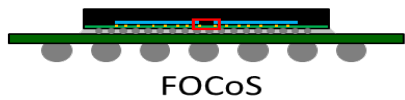


ASE Design Optimization on SI for Advanced Packaging

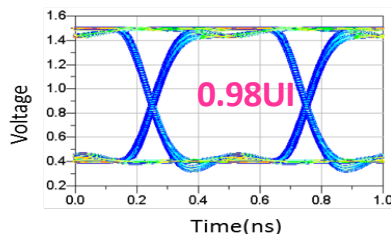
D2D SI optimization

Structure

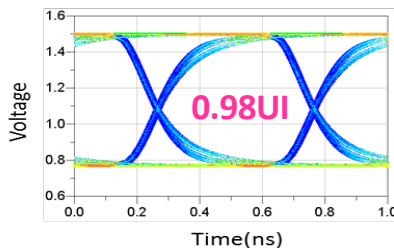
2Gbps/pin



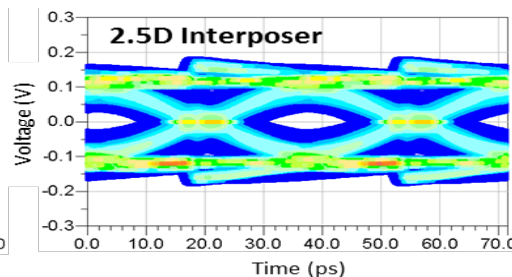
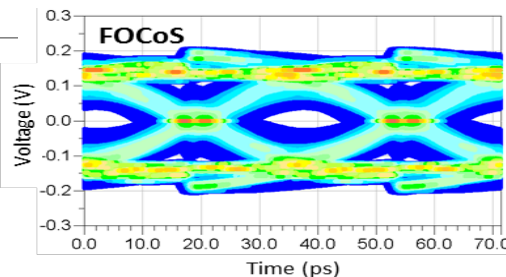
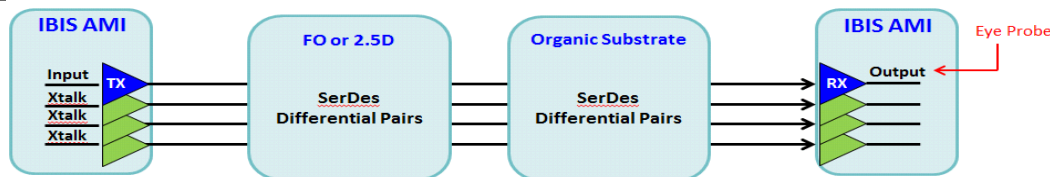
FOCoS



2.5D Interposer

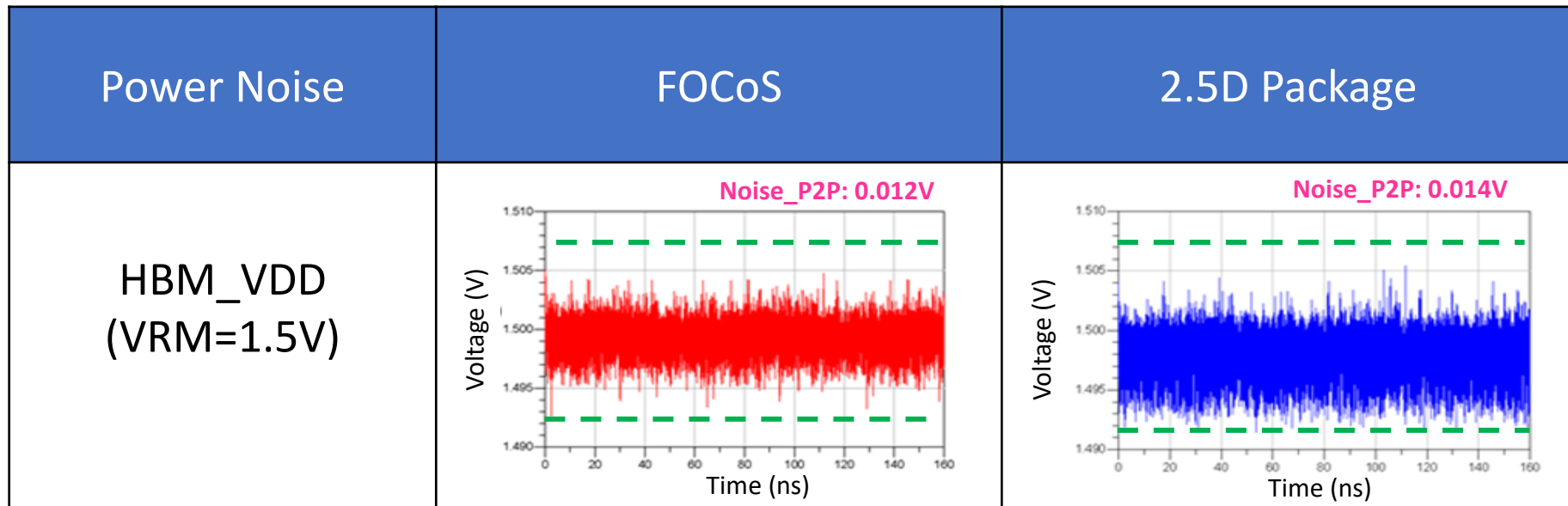


28Gbps SerDes Channel Signal Integrity



ASE Design Optimization on PI for Advanced Packaging

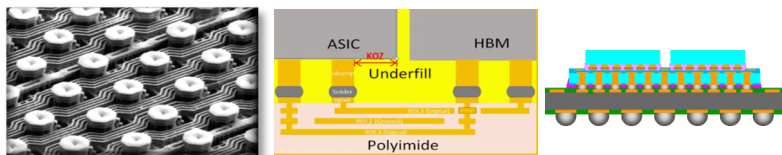
- Design optimization enable dynamic power noise to meet system specification ($V_{p2p} < 0.015\text{ V}$)



Design Challenges for Chiplets and Heterogeneous Integration

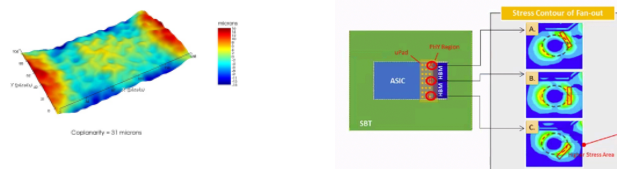
Driver 1- High Density Scaling

- Smaller Si node
- Interconnect scaling (small pitch) & high density
- Advanced packaging Technology (3D)
- **New Si, advanced package & substrate co-design**



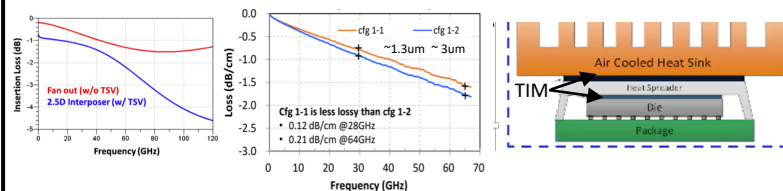
Driver 2- Manufacturing Feasibility

- Warpage & coplanarity
- Stress, thermal and good reliability;
- **New DRC, LVS and electrical Co-simulation, DFM & DFT**
- **Short design cycle time**



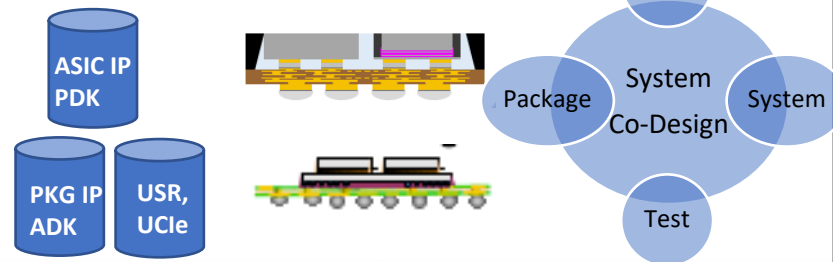
Driver 3- High performance & D2D Standardization

- High speed, Low loss, high bandwidth & low power
- High current capability & good EM & good thermal
- **D2D interface standardization (BoW, openHBI, UCIe)**



Driver 4 – Design Ecosystem & Collaboration

- Architectural & IP designers
- Packaging & Assembly Manufacturers & System integrators
- **Design Ecosystem**



Summary

- **Chiplets and Heterogeneous integration optimize performance and cost**

- Advanced Packaging offer solutions for chiplets and heterogeneous integration.

- **ASE provides advanced packaging solutions and design kits for chiplets integration**

- High density Fanout FOCoS , 2.5D Si Interposer and SIP in many formats
- Design solutions in place for efficient hybrid design from devices to package & package to system
- DFM and verification (DRC/LVS/PDK) play important roles to ensure manufacturability
- SI & PI simulations for FOCoS & 2.5D are demonstrated within hybrid design flow

- **System co-design & collaboration**

- New Si, advanced package & substrate Co-design
- New DRC, LVS and electrical Co-Stimulation, DFM & DFT
- Design ecosystem and collaboration among IDMs, manufactures, EDA tool suppliers and system integrators

Thank You

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