After 30 Years Why Are We Still Talking about Known Good Die?

- TRACK INNOVATION
- IDENTIFY TRENDS
- ANALYZE GROWTH
- INFLUENCE DECISIONS

RELEVANT, ACCURATE, TIMELY

E. Jan Vardaman,

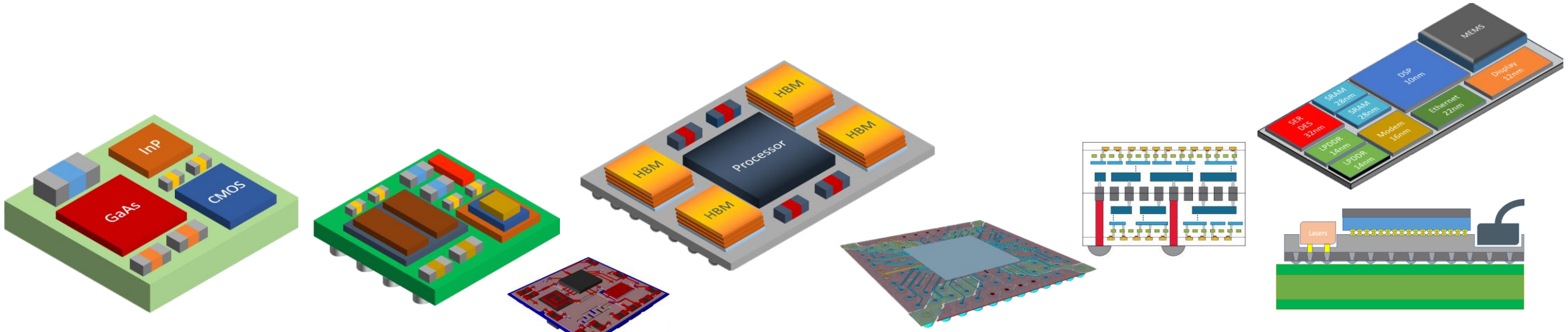
President and Founder

TechSearch INTERNATIONAL

Multichip Modules (MCMs)

- **Survey results of merchant MCM vendors from 1993**
  - Single most important barrier to MCM use was the availability of affordable know good die (KGD)
  - Majority of bare die sold processed through parametric or continuity electrical testing
  - Problem: small, but significant number of ICs that passed parametric testing have latent defects that do not show up until being in operation for some time
  - Low module yield that increased the cost of repair and rework was one of the greatest concerns
- **Vertically integrated companies had some advantages (they could use their internally fabricated die)**

Evolution of Advanced Multi-Chip(let) Packaging Technologies



Multi-Chip Module (MCM)

System in Package (SiP)

RF Module

2.5D-IC (Silicon Interposer)

Embedded Bridges

High-Density RDL/FOWLP

3D-IC (Bump-less)

Heterogeneous Integration (Disaggregated SoC) Photonics

1980 1990 1998 2005 2010 2014 2016 2018 Now

cadence

Source: Cadence Design Systems.

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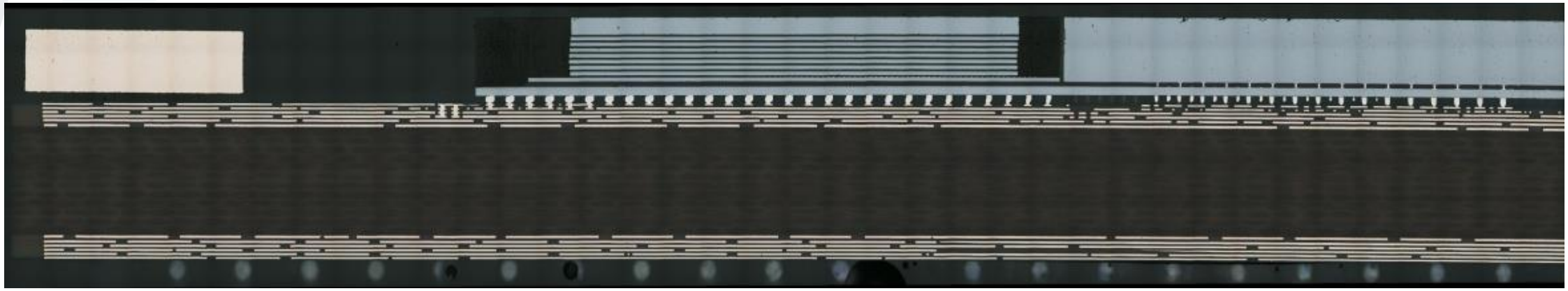
A New 3D Era is Emerging

- **A new era in 3D will provide advantages to optimize system power, performance, area, and cost**
  - It is possible to continue scaling, but cost advantages are achieved with advanced packaging innovations
- **Potential solutions for high-performance packaging (partition the die)**
  - Homogeneous integration (split die to reduce die size and improve yield at wafer level)
  - Heterogeneous integration (interposers, FO-on-substrate or other multi-die solutions such as “chiplets,” and some variation of 3D stacking)
  - Introduction of 3D chip stacking with bumpless bonding
- **Heterogeneous integration provides a solution that can be in many formats!**
  - Silicon interposers (called 2.5D but HIR refers to this as 2DS)
  - Alternatives such as Intel’s EMIB or Fan-out on Substrate or Organics (2DO)
  - “Chiplets” where substrate interconnect provides in package communication between different functions
  - 3D structures with TSVs or direct bond interconnect

Challenges for Heterogeneous Integration

- **Requires new architectures and co-design**
  - EDA tools required
  - Need good thermal and electrical modeling
- **Large body sizes = large laminate substrate body sizes (some request for future 100 mm x 100 mm) make board-level assembl difficult**
  - Warpage changes during reflow
- **Thermal challenges**
  - Need new designs with lower power dissipation
  - Need new thermal interface materials and cooling methods
- **Test Challenges**
  - Known Good Die (KGD)
  - Need more comprehensive test content that can be run at wafer-level
  - Need new methods to probe fine pitch bumps or test coverage without touching µbumps

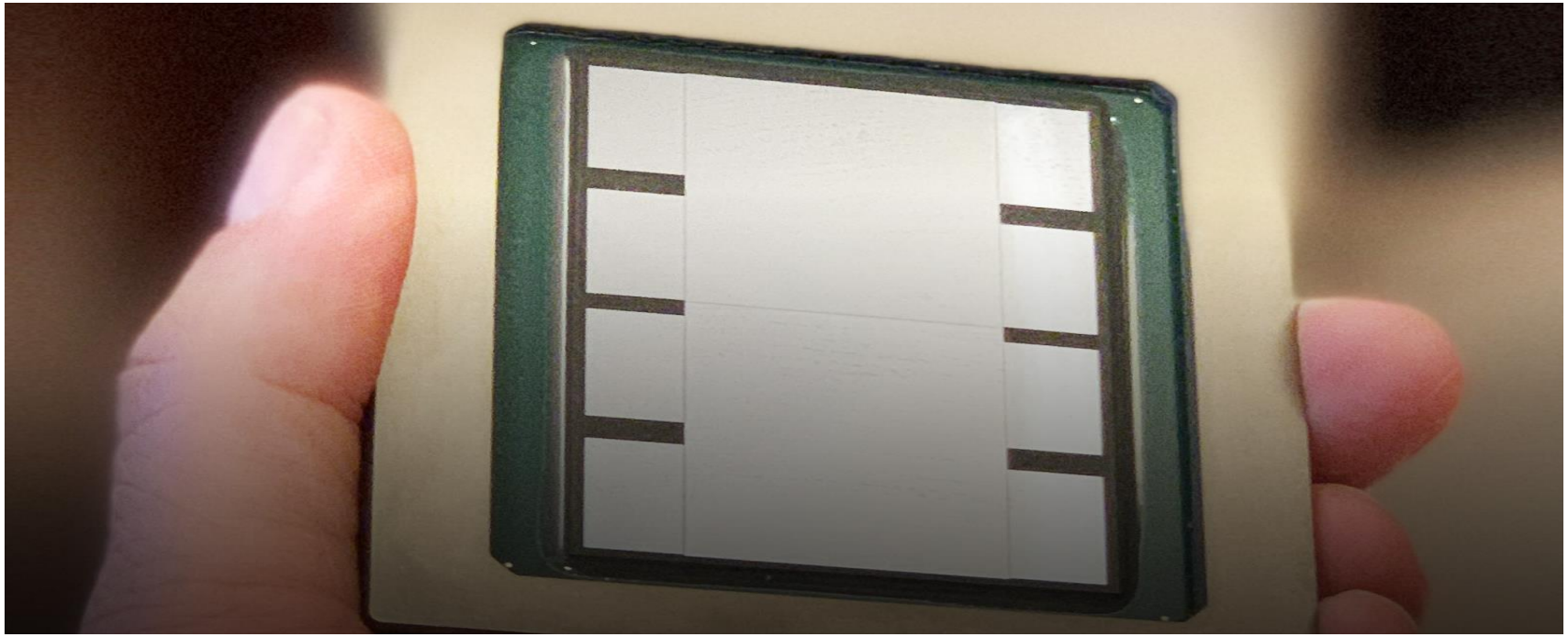
NVIDIA's GPU + HBM



- **NVIDIA's GPU with 4 HBMs (8 high stack + logic layer) mounted on Si interposer**
  - HBM with wide bus (1,024 I/Os, ~4,000 bumps, 55µm micro bump pitch)
  - Silicon interposer is 34 mm x 43 mm with 1.1µm lines and 1.6µm space
- **NVIDIA's latest A100 uses GPU + 6 HBMs**
- **HBM cost ~$200 each, Si interposer $1,000+, expensive solution requires high reliability,**

Source: NVIDIA.

TSMC CoWoS

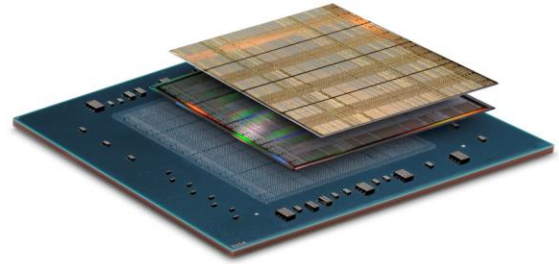


Source: TSMC.

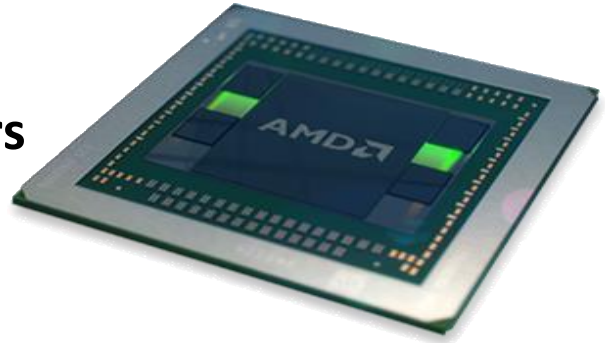
- **Largest silicon interposer from TSMC in production is 2,500 mm^2**
  - >2X reticle size
- **Room for two, 600mm^2 processors + 8 HBMs in 75mm x 75mm package**

Early Examples with Si Interposers: What Have We Learned

- **FPGA shipments started (HVM 2012)**
  - Xilinx has many products
  - Partition die so that the large die can me fabricated into “slices’ providing better yield, improved performance
  - Binning die provided a big advantage
- **ASIC designs moving into production**
- **GPU + stacked memory**
  - Provide higher performance for applications such as gaming
  - Memory stack + logic
- **Applications expanded to include network systems, AI accelerators for datacenters, servers**

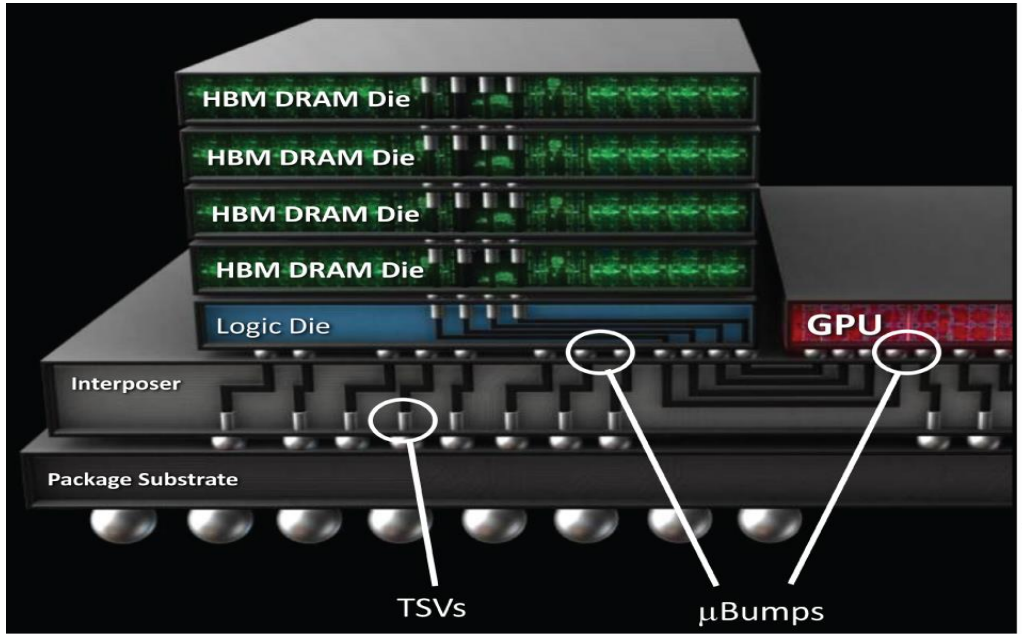


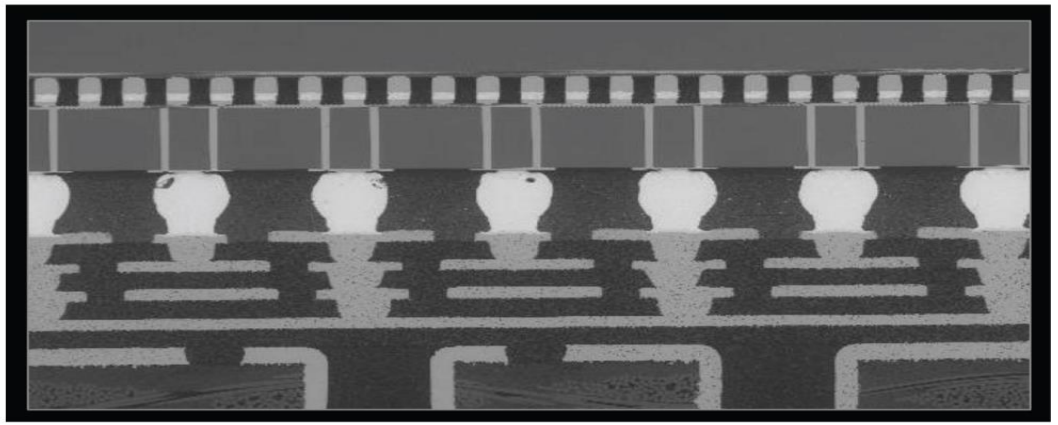
Source: Xilinx.



Source: AMD.

AMD's "Fiji" with Silicon Interposer and HBM

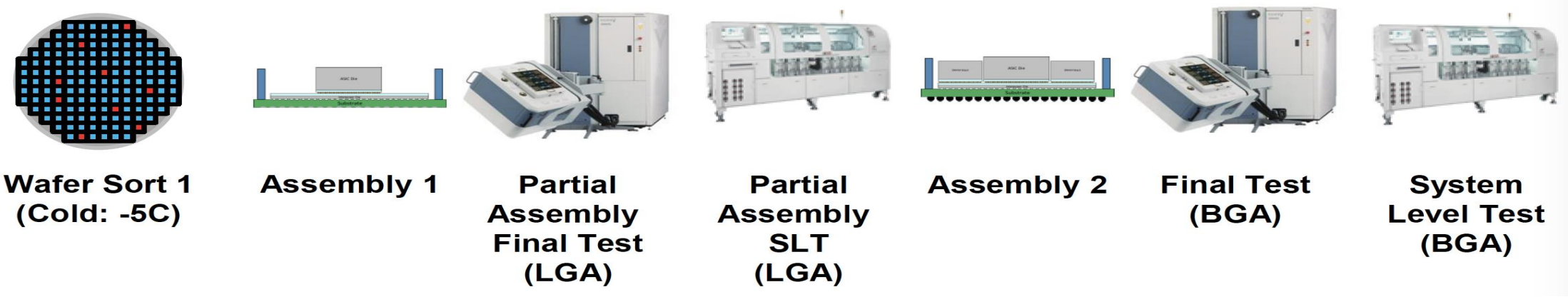




Source: AMD.

- **AMD "Fiji" solution for the graphics market**
- **Four HBM stacks, each containing stacked DRAMs and a logic die with TSVs mounted on a 1,011mm² Si interposer**

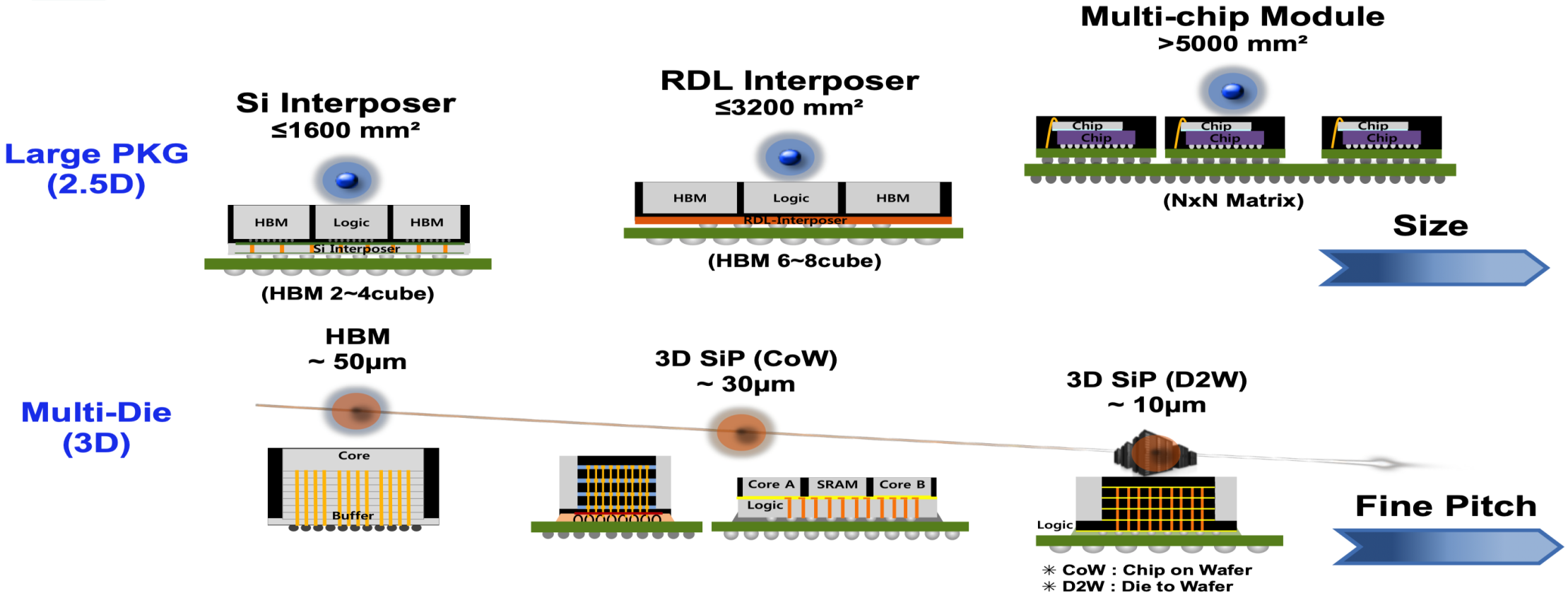
Test Strategy: Key To AMD Success



Source: ASE and AMD.

- **Wafer sort, binning**
- **Partial assembly test (unique to this application, LGA pad surface finish, contact force control, yield repeatability, and contamination control)**
- **Final test**

Samsung's Package Integration Solutions for AI/Server/HPC

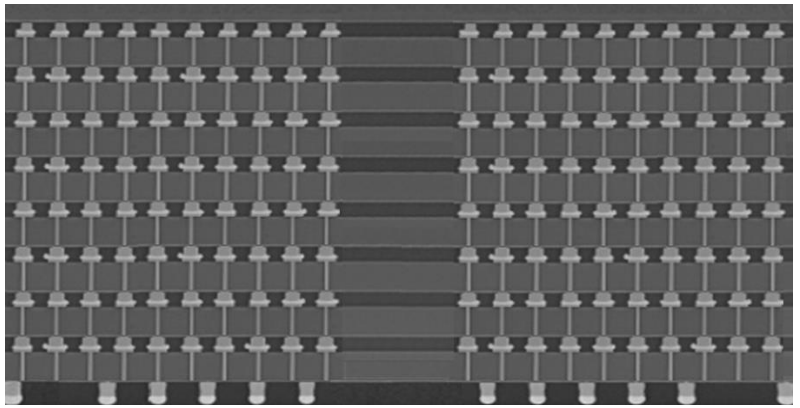


Source: Samsung.

- **Samsung offers multiple solutions for high-performance applications and has an advantage in supply of HBM with its own internal production**

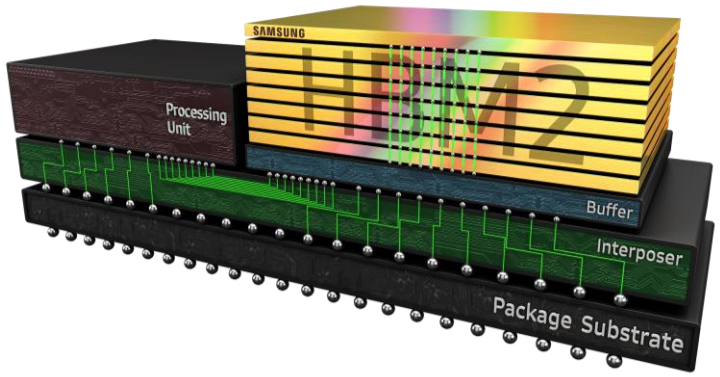
HBM Development

- **Stacked die with TSVs requirements**
  - Well joined TSV/micro bumps
  - Well aligned micro bumps
  - No underfill delamination or voids
- **Test vehicles TSV stacked memory**
  - Robustness of TSVs and micro bumps important
  - All test patterns electrically tested in test vehicles
- **Key factors in success**
  - BIST
  - Redundancy

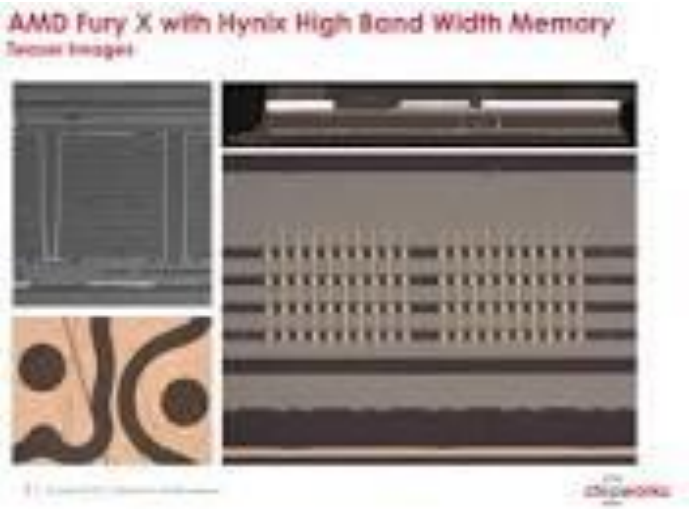


High Bandwidth Memory

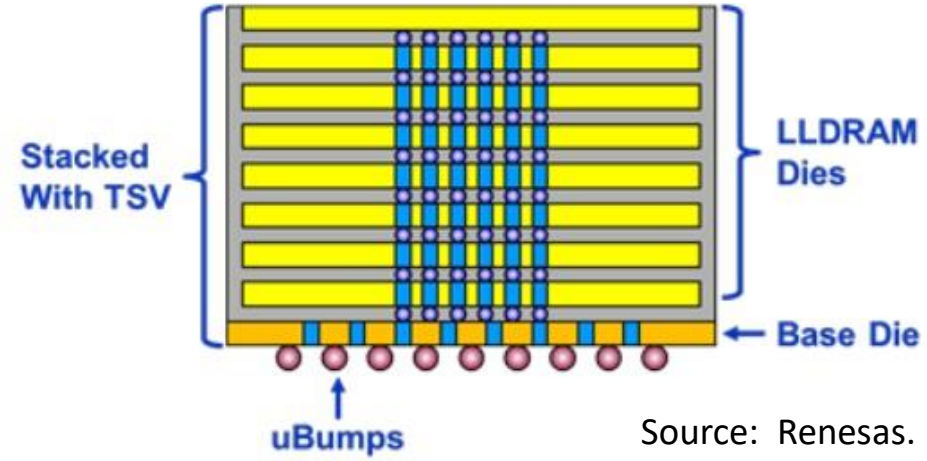
- **Advantages**
  - Higher bandwidth
  - Lower latency
  - Lower power consumption
- **Micro bumps used to connect die**
- **Suppliers**
  - Samsung (HBM)
  - SK Hynix (HBM)
  - Micron (future HBM)
  - Renesas (Low-latency HBM)



Source: Samsung.



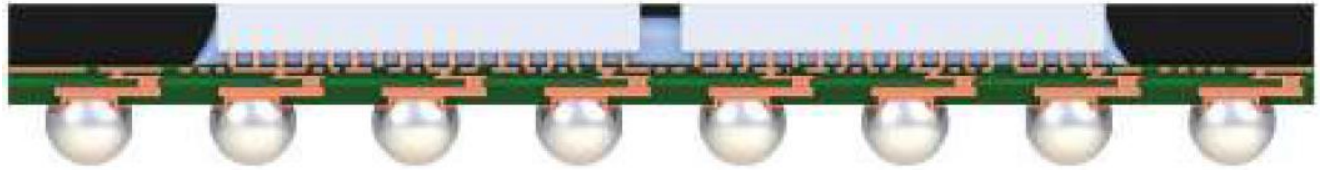
Source: Chipworks.

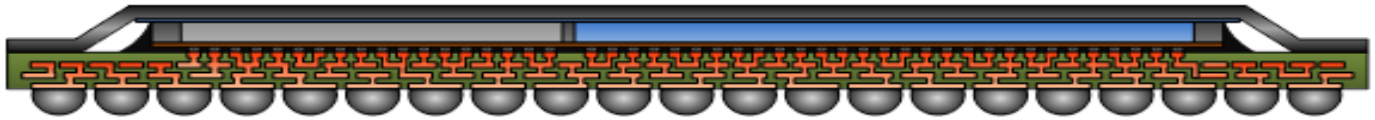


Source: Renesas.

Fan-out on Substrate: Future Use with HBM

- **ASE's Fan-Out Chip on Substrate (FOCoS)**
  - RDL with 2/2µm L/S
  - Up to 3 RDLs plus UBM
  - High I/O (>1,000)
  - Production with chip first since 2016 (Hi-Silicon Network Switch)
  - Chip last qualified
- **TSMC Integrated Fan-Out on Substrate (InFO_oS) and InFO_MS**
  - RDL with 2/2µm L/S
  - Up to 3 RDLs plus UBM
  - Production of InFO_oS (MediaTek Network Switch)
- **Amkor's Silicon Wafer Integrated Fan-out Technology (SWIFT®)**
  - RDL with 2/2µm L/S
  - Up to 3 RDLs plus UBM





FOCoS – Fan Out Chip on Substrate (FO FCBGA)

Source: ASE.

Source: Amkor.

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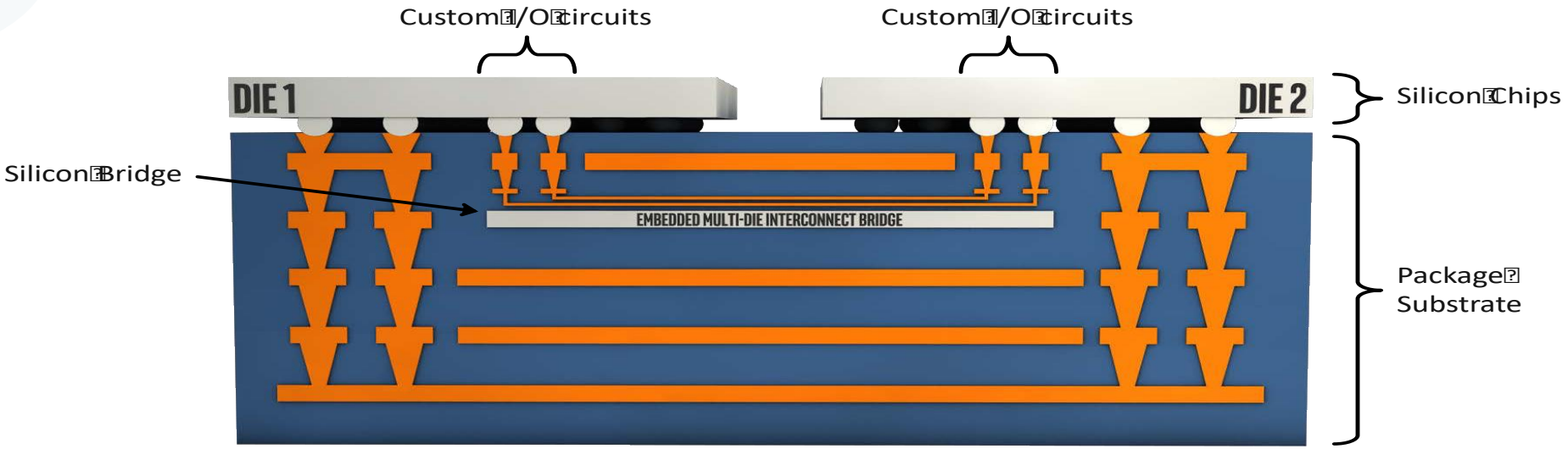
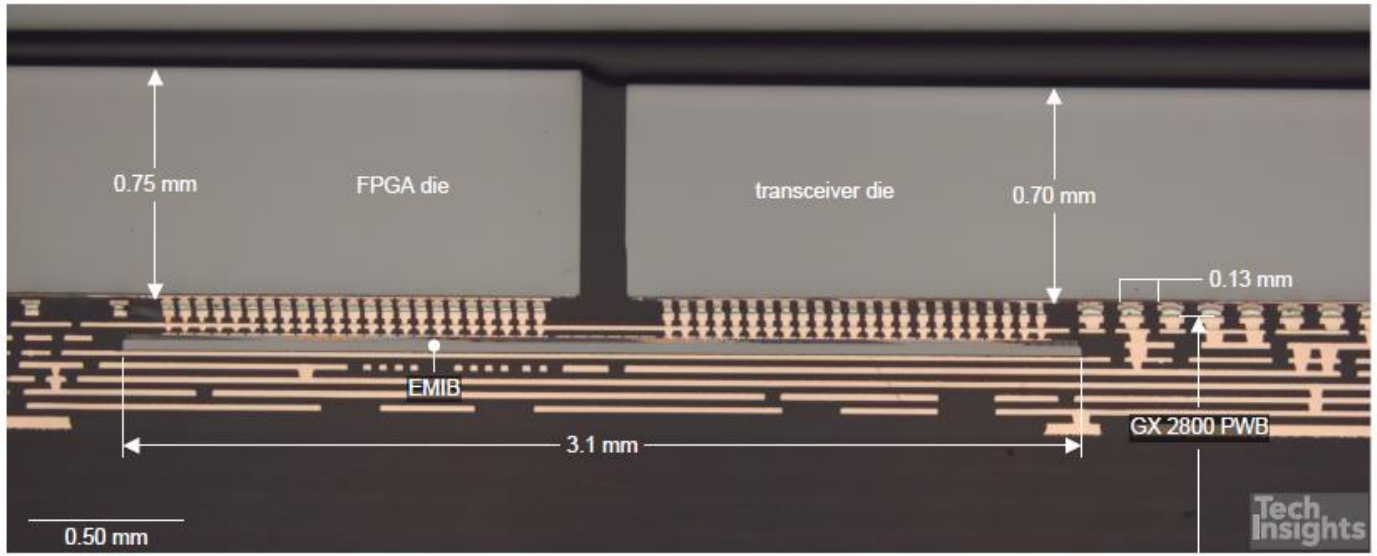
Intel's EMIB Package Cross Section



Source: Intel.

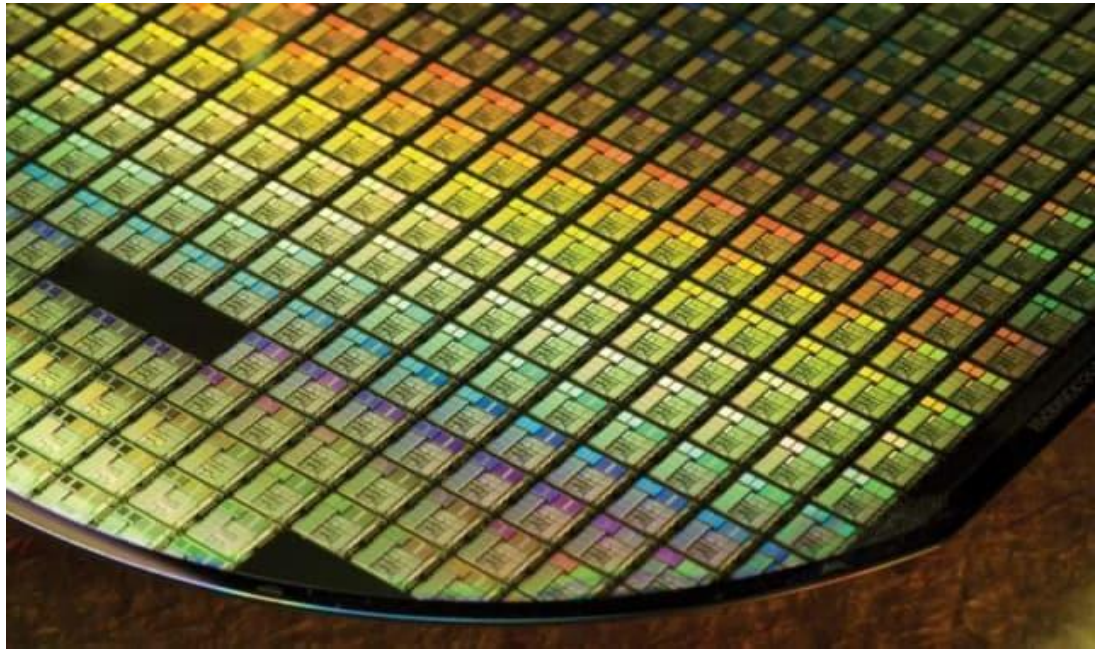
- **Embedded Multi-die Interconnect Bridge (EMIB) A small silicon bridge chip is embedded into the package (no TSVs)**
  - Package substrate provided by substrate supplier (does Si bridge embedding)
  - Micro bumps on chips, communication between chips through bridge in interposer
  - provides a 2.5D localized high-density interconnect between the FPGA and the transceiver die



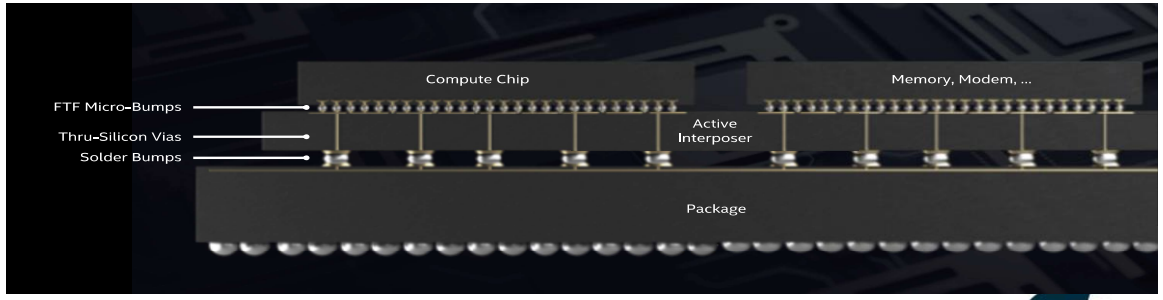
Intel.Stratix-10 Source: TechInsights

3D Integration

- **More 3D memory stacking**
  - HBM2 in production today at Samsung and SK Hynix
  - HBM from Micron sampling
- **Intel's Foveros**
  - Micro bump in first production
  - Future hybrid bonding
- **TSMC's SoIC and WoW**
  - System on Integrated Chip (SoIC) 3D stack using CoW process to handle <10µm pad pitch between chips
  - Use of hybrid bonding
- **New forms of 3D stacking (die-to-die interconnects) are coming**
  - Die-to-wafer attach
  - Wafer-to-wafer attach
- **Co-design is essential**

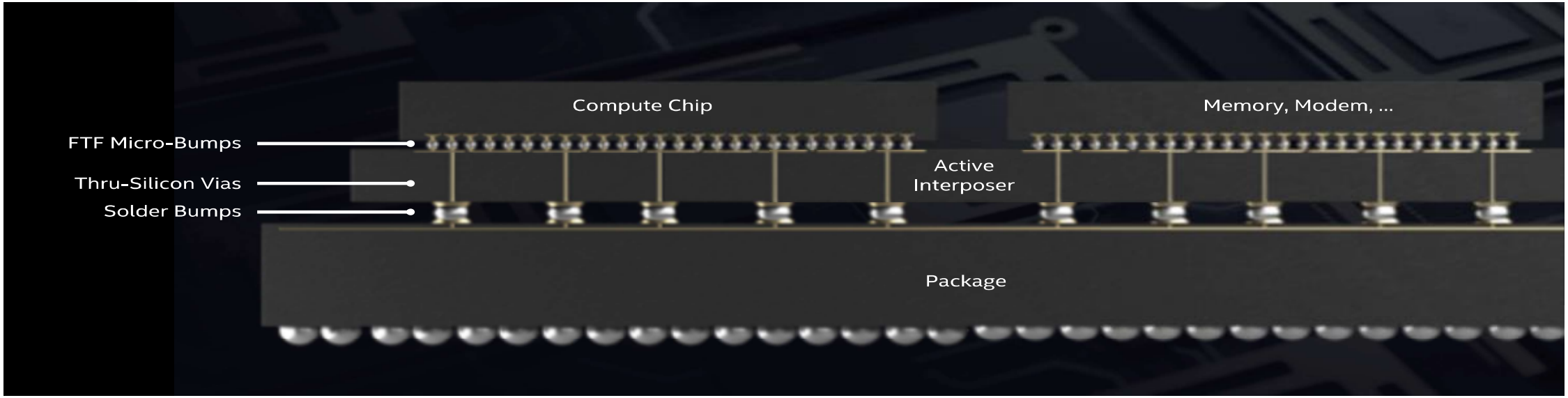


Source: TSMC.



Source: Intel.

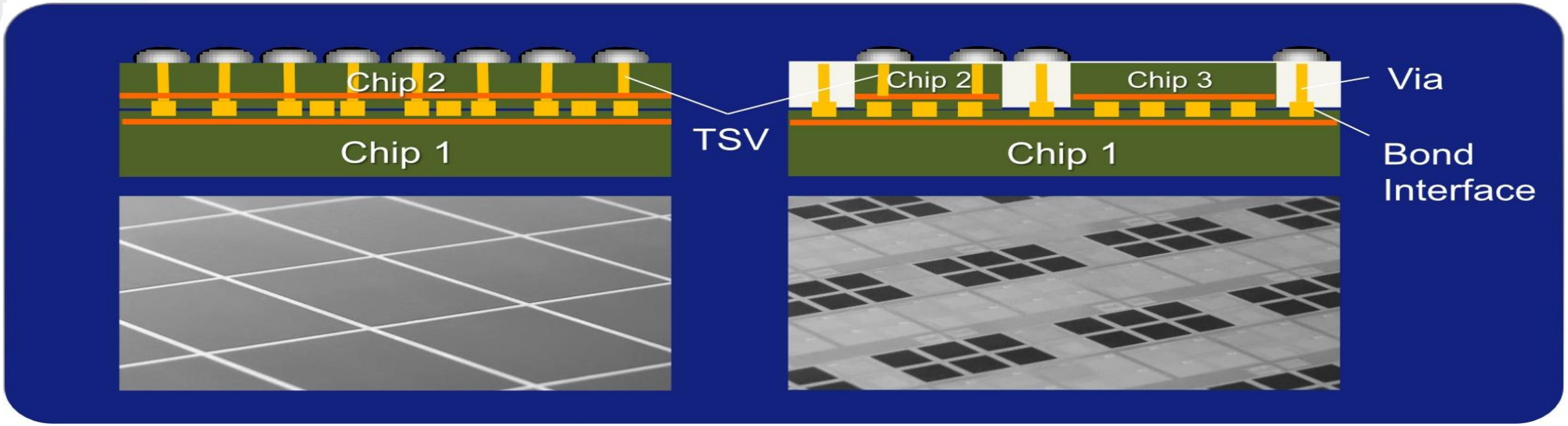
Intel Foveros 3D Face-to-Face Stacking



Source: Intel.

- **Intel's Foveros technology is considered 3D because die are stacked on an active interposer**
- **Gives designers greater flexibility to mix and match IP blocks with various memory and I/O elements into new form factors**
- **Mounting memory on active interposer removes the bottleneck of memory proximity**
- **Technology uses 3D face-to-face stacking process**
  - Large die are bumped and mounted on an active interposer next to memory or die with other functions
  - Active interposer can contact platform controller hub (PCH) that manages I/O for the system
  - Active interposer is attached to the package substrate with solder bumps

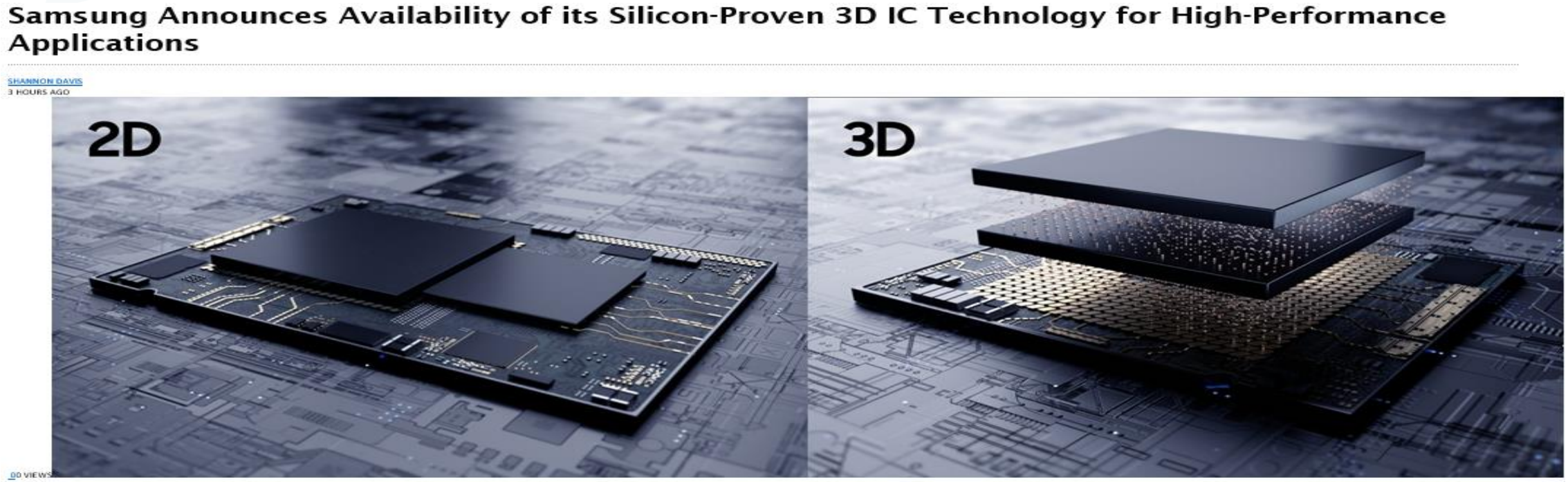
TSMC SoIC™ Technology



Source: TSMC.

- First commercial products with SoIC expected in 2021, designs in Q4 2020
- Commercial products with up to 10 chiplets expected in 2-3 years
- Advanced silicon nodes of 7nm or 5nm could be used
- Possible to stack III-V components as long as Cu damascene process is applied to wafer
- SoIC could be placed next to HBM on RDL substrate or SoIC could be mounted next to HBM on CoWoS

Samsung 3D IC Heterogeneous Integration



Source: Samsung.

- **Samsung introduction of logic and memory stack**

Test Challenges for Heterogeneous Integration

- **Known Good Die (KGD) required**
  - BIST and redundancy
- **Known Good Substrate needed**
  - AOI used for inspection
- **Know Good Interconnect (assumed)**
- **Need more comprehensive test content that can be run at wafer-level**
- **Need new methods to probe fine pitch bumps or test coverage without touching µbumps**

Thank you!

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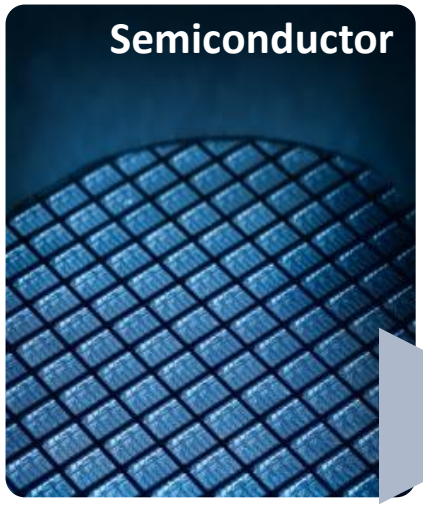

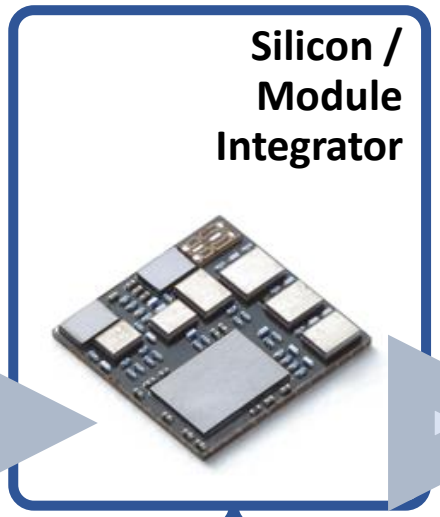

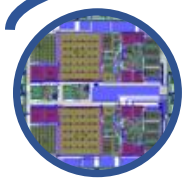
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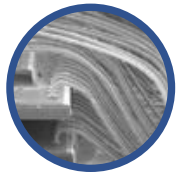
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