ADVANTEST

Shift Left

Dave Armstrong

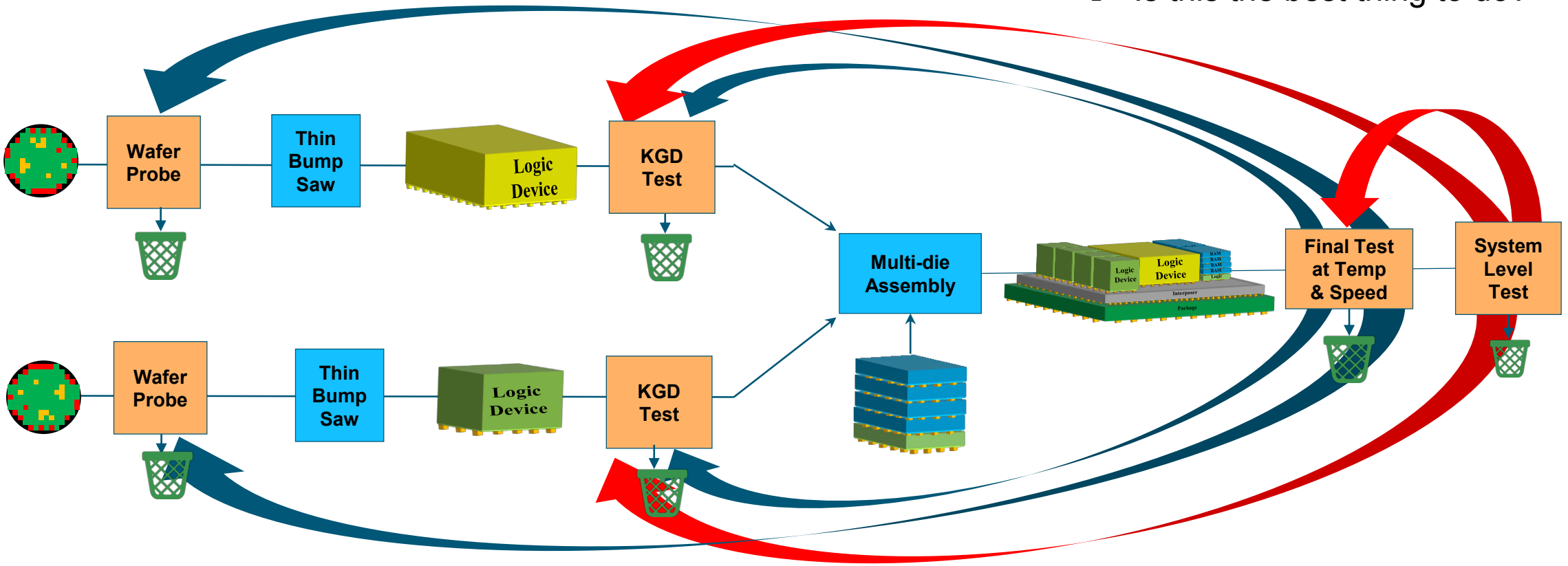
Goals

1. What are the trends?
2. What industry changes are driving this shift?
3. What are the financial implications of this shift?
4. How is this shift implemented?
5. Risk of over-testing.
6. Contributions of this approach.

What is the Trend?

Some people are shifting logic level test content to the right - into system level test.

➔ Is this the best thing to do?



Lower Cost Solution = Shift Left

Description of Typical Un-Shifted Test Steps

Test Step	Typical Goals	Test Cell
Wafer Test Step	• Find hard rejects. • Confirm scan & functionality at one temp.	Automatic Test Equipment (ATE) + Wafer Prober
KGD Test Step	• Confirm scan & functionality at a second temp • Find assembly defects	ATE + Reconstituted die prober or ATE + Singulated die prober
Final Test Step	• Packaged device test • Extended scan tests • Parametric performance test • At-speed tests • High-power tests • Stress tests	ATE + Active Thermal Control (ATC) ATC + Device/Die Handler
System Level Test Step	• Packaged device test • Boot up tests • Fuse blowing	System Level Tester (SLT) + ATC + Device handler

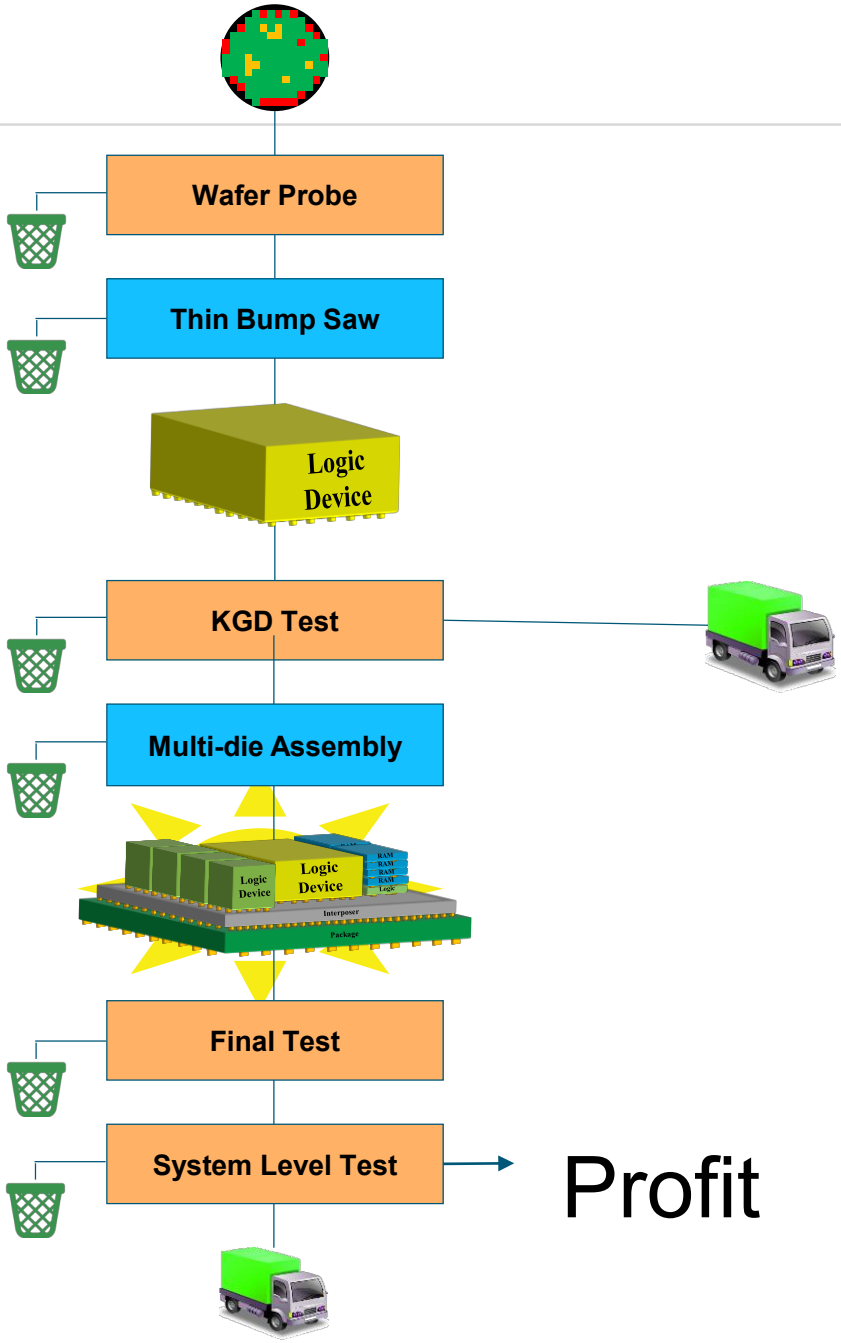
Shift Left

Why is “Shift-Left” Happening?

1. More test sooner ➔ more profitable products.

2. More heterogeneous integration ➔ Parts need to be of a higher quality level (KGD)

3. Shippable unit is changing ➔ Final Test or SLT need to be done on raw die.



Unfortunate KGD Realities . . .

Question: If I get a 90% yield at wafer probe – what percentage of the possible faults did I cover?

Answers: Yield only states what percentage of the parts tested were bad.
The passing parts may or may not be 100% good.

Question: If I spend 10s of test time to get a 90% yield with a high fault coverage, how much time and fallout must I spend to find all the failing devices?

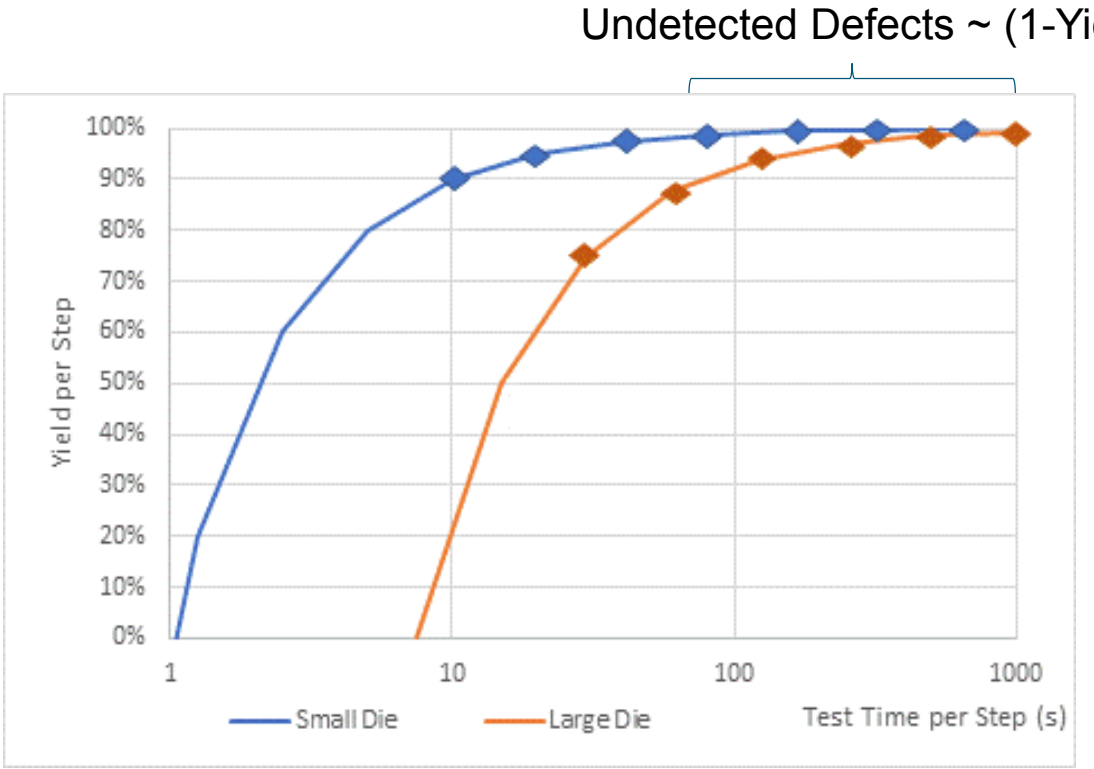
Answers: The law of diminishing returns suggests more time is needed for more coverage.
Exponential coverage curve asymptotically approaches 100% but never gets there.

“Reasonable” Assumptions

1. For the sake of this presentation let’s assume that half the remaining faults are detected in the next step which is twice as long.

Test Step	Yield	Test Time
1	90%/75%	10s/30s
2	95%/87.5%	20s/60s
3	97.5%/93.75%	40s/120s
4	98.75%/96.9%	80s/240s

The faults found per test step is proportional to the area over the curve.



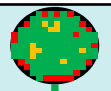
2. This presentation scales the cost estimates based on the raw cost of a small 10x10 mm die cost. All cost estimates are shown relative to this cost in recognizing that cost ratios tend to be more consistent while absolute costs may vary from technology to technology and/or company to company.

How Much Cost Savings – Small Device Shipping as KGD

Assumptions

	Small Device
Technology	10 nm
Die per wafer	650
Wafer Probe Test Time	10
Sites	4
Wafer Probe Yield	90%
Next step Test-time & Yield	Per Assumption on Previous slide

Note:
Values given for example only.
Your results will vary.

	Without Shift-Left					With Shift-Left				
	# Out	# Fail	Test Time	Yield	$$	# Out	# Fail	Test Time	Yield	$$
	650	0	-	-	1x	650	0	-	-	1x
Wafer Probe	585	65	10	90%	1.14x	556	94	30	85.5%	1.24x
Thin Bump Saw	579	6	-	99%	1.15x	550	6	-	99%	1.25x
KGD Test	550	29	20	95%	1.25x	536	14	40	97.5%	1.36x
	550	27	-	-	-	536	13	-	-	-

Shifting left reduced unfound failures shipped by 51%

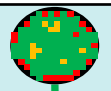
Shift left cost 9% more to manufacture

How Much Cost Savings – Large Device Shipping as KGD

Assumptions

	Large Device
Technology	10 nm
Die per wafer	85
Wafer Probe Test Time	30
Sites	1
Wafer Probe Yield	75%
Next step Test-time & Yield	Per Assumption on Prior slide

Note:
Values given for example only.
Your results will vary.

	Without Shift-Left					With Shift-Left				
	# Out	# Fail	Test Time	Yield	$$	# Out	# Fail	Test Time	Yield	$$
	85	0	-	-	7.4x	85	0	-	-	7.4x
Wafer Probe	64	21	30	75%	10.2x	56	29	90	65.6%	12.4x
Thin Bump Saw	63	1	-	99%	10.3x	55	1	-	99%	12.5x
KGD Test	55	8	60	87.5%	12.4x	52	3	120	93.8%	14.3x
	55	7	-	-		52	3	-	-	

Shifting left reduced unfound failures shipped by 53%

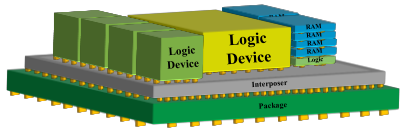
Shift left cost 16% more to manufacture

How Much Cost Savings – Multi-Chip Module

Assumption:

1. Zero cost attributed to packaging & assembly (Shift-left did save the cost of 13x interposers & substrates.)

2. Test costs attributed based on test-time and typical hourly costs for ATE, prober, and SLT.



Note:
Values given for example only.
Your results will vary.

	Without Shift-Left				
Goal: Assemble 100x Devices	**# Out**	**# Fail**	**Test Time**	**Yield**	**$$**
10x Small Die/MCM	1000	-	-	-	1.25x
1x Large Die/MCM	100	-	-	-	12.4x
Multi-die Assembly	99	1	-	99%	41.3x
Final Test	72	27	520	72.8%	61.9x
System Level Test	61	11	1040	85.4%	73.3x
	61				

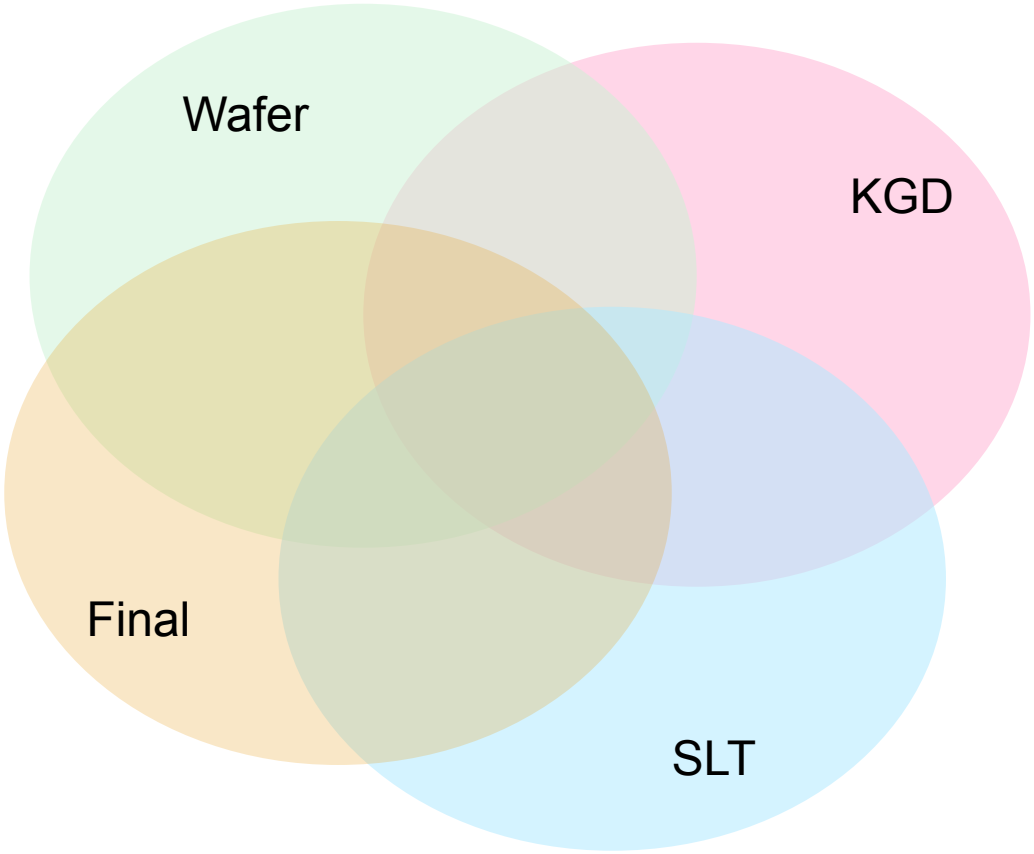
With Shift-Left				
# Out	**# Fail**	**Test Time**	**Yield**	**$$**
1000	-	-	-	1.36x
100	-	-	-	14.3x
99	1	-	99%	44.4x
85	14	1040	85.4%	52.8x
Reduced SLT Focused on Reliability Testing				
85				

Shift left cost 28% LESS cost to manufacture
Shipped 37% more parts shipped.

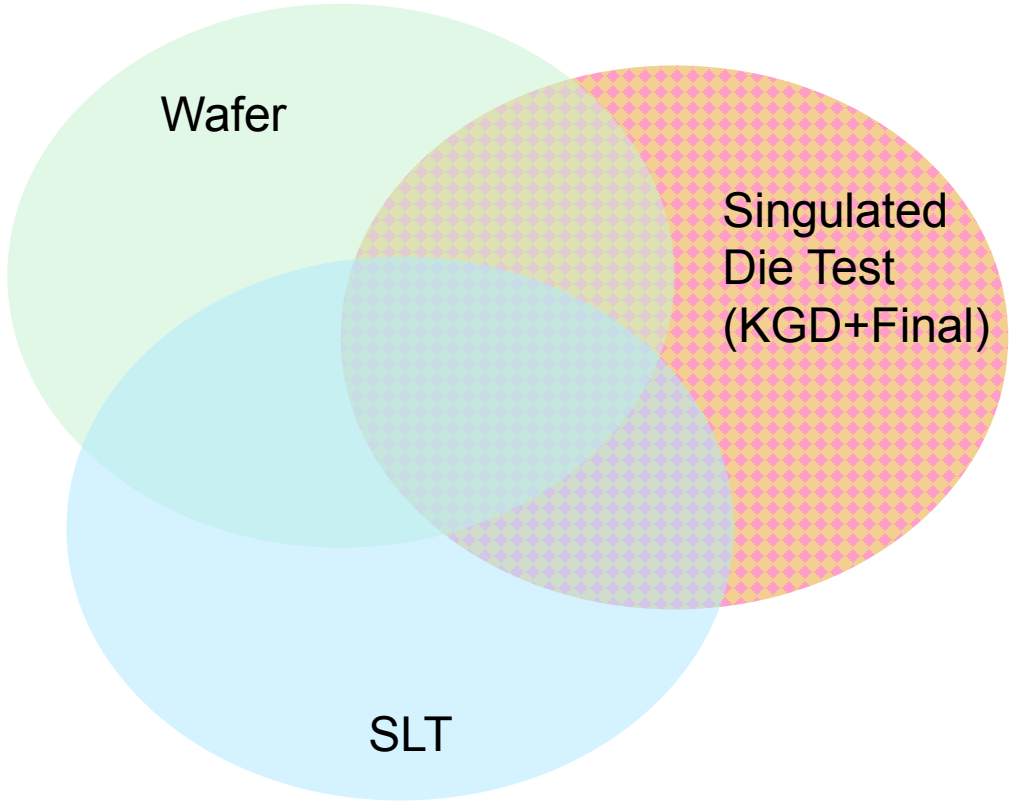
What System Changes are Needed to Do This?

Shift-Left Change	Key Capabilities	Necessary Changes
Final-Test ➔ KGD Test	At-speed tests High-Power ATC	ATE: High-speed instruments ATE: Higher power supplies ATC: T-Junction feedback per DUT Probes: Higher Current Carrying Capacity (CCC) probes Probes: Higher-frequency probes Prober: Singulated Die Handler or Frame Handler if temp not too high.
KGD Test ➔ Wafer Test	Two temp testing. Crack detection.	ATE: Extended test sequence ATC: High & Low temp testing
System Level Test ➔ Final-Test	High-Power ATC High-speed interfaces Device boot-up	ATE: System focused environment. Software: System focused code.

What About Over-Testing?



Without Shift-Left



With Final Test - Left Shifted into KGD

Fewer Test Steps ➔ Less Over-Testing (and less handling)

This Presentation Has …

a. Shown how test content is a valuable resource which is best deployed where it can provide the maximum value.

b. Confirmed what may be obvious, that by doing more tests sooner you can ship significantly higher quality die-level products for a small increase in product cost.

c. Calculated that “KGD” product quality can improve significantly for a small incremental cost by shifting test content to the left.

d. Shown that by shifting test-content to the left, one can ship more multi-chip modules sooner, with a lower cost.

e. Pointed out some of the test-sequence changes and equipment enhancements which need to be considered when exploring this concept.

Backup

Assumptions

Wafer Test Step

Parameter	Value
$/Hour	$140
Wafer Load	225s
Utilization	85%
Index time	0.75S

KGD Test Step

Parameter	Value
$/Hour	$140
Wafer Load	225s
Utilization	85%
Index time	0.75S

Final Test Step

Parameter	Value
$/Hour	$145
Sites	1
Utilization	85%
Index time	1.5s

System Level Test

Parameter	Value
$/Hour	$50
Sites	8
Utilization	85%
Index time	4s

Un-shifted Assumptions

Small Test Time / Sites	10s / 4	20s / 1	40s / 1	80s / 1
Large Test Time / Site	30s / 1	60s / 1	120s / 1	240s / 1
MCM Test Time / Site	N/A	N/A	N/A	1040s (10*80+240) / 8

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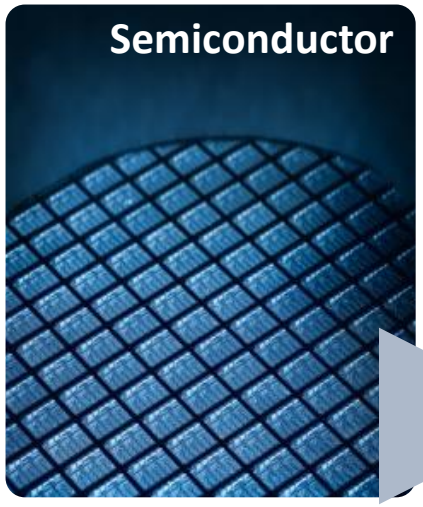

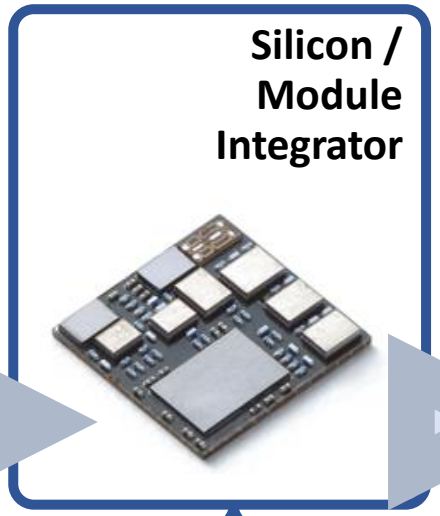

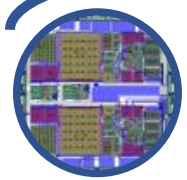
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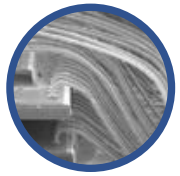
Assembly


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