



CHALLENGES OF ADVANCED PACKAGING FAILURE ANALYSIS

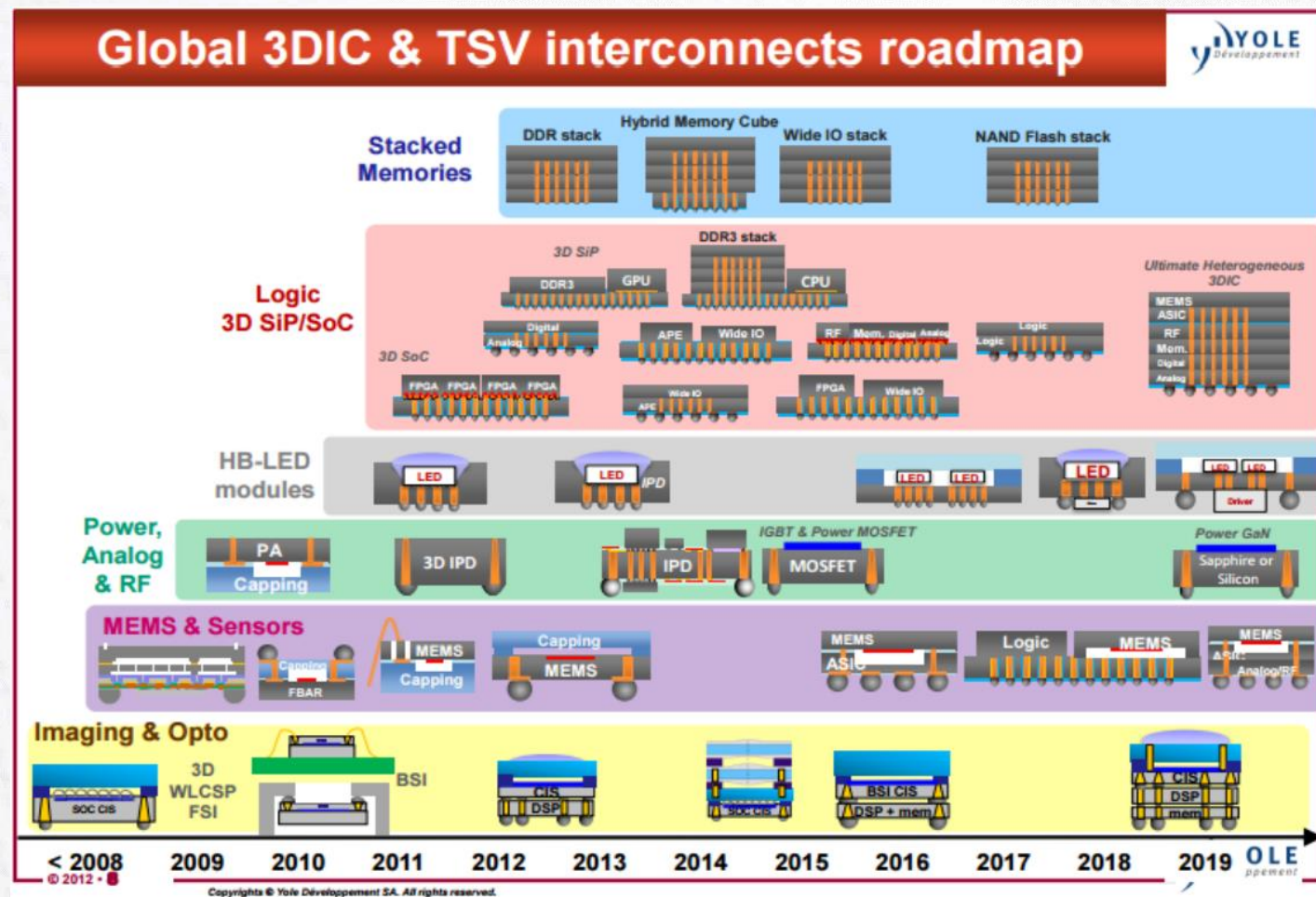
BERNICE ZEE & JIANN MIN CHIN

FOUNDRY TECHNOLOGY AND PRODUCT ENGINEERING, AMD

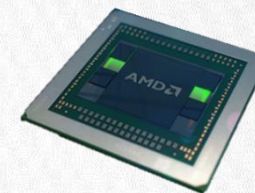
OUTLINE

- Introduction – Heterogenous Integration
- Emerging Next Generation Packaging Technologies
- Importance of Failure Analysis (FA)
- Failure Mechanisms in Next Generation Packaging Technologies
- Requirements for Next Generation Package FA
- FA Capabilities Development
- Case Studies
- Conclusion

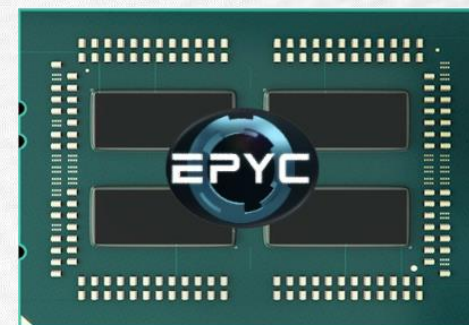
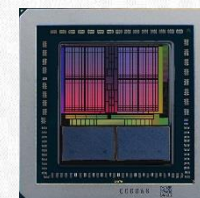
INTRODUCTION - HETEROGENEOUS INTEGRATION



AMD Radeon™
R9 FURY X



RADEON RX
VEGA

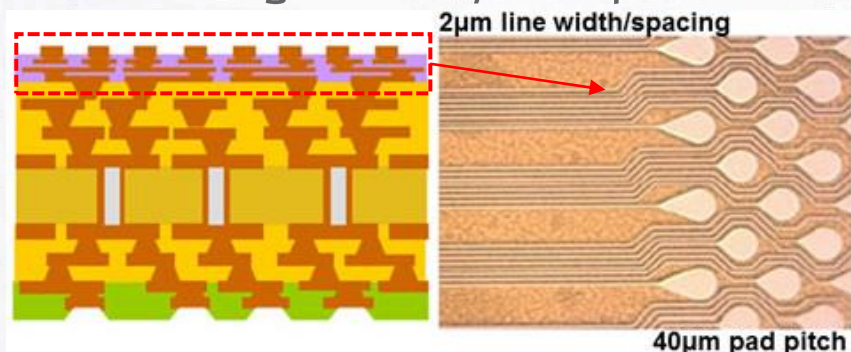


Source: Trehwella, J., EPTC 2016. "Lunchtime Talk - Acceleration of Electronic Packaging Innovation through Collaboration".
<https://eptcieeedotorg.wordpress.com/author/rikoimade/>

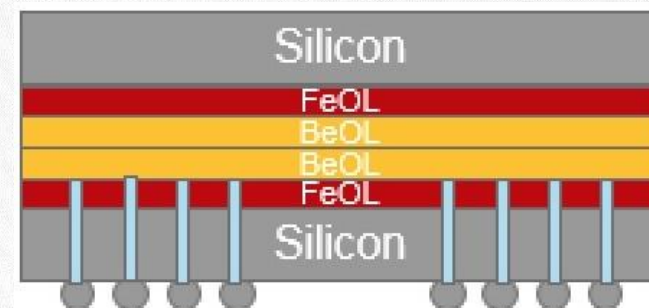
- Advance packaging innovations to enable functionality diversification at lower cost.
- The trend for next generation packaging: (1) stacking (2) "dis-integration".

EMERGING NEXT GENERATION PACKAGING TECHNOLOGIES

- High-density organic substrate:
 - Low cost alternative to Si interposer.
 - Enable high density, fine pitch interconnects.
- 3D Wafer-on-Wafer Stacking:
 - High aspect ratio TSV, fine pitch bonding for true 3D packaging.

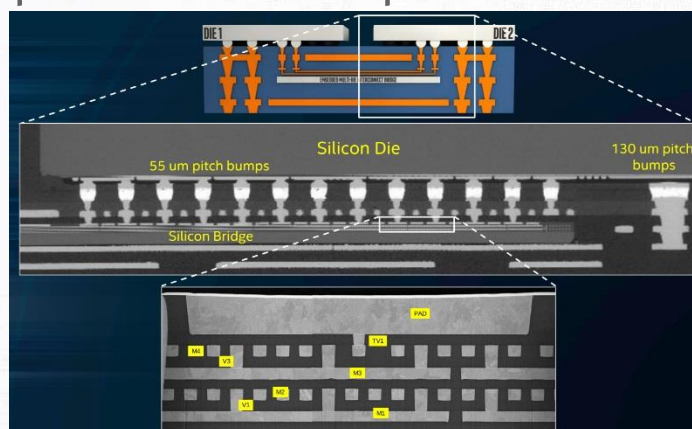


Source: Lau, John H., CSR Jul-Aug 2014. "The future of interposers for semiconductor IC packaging". http://www.chipscalereview.com/legacy/tech_monthly/csrtm-1213-front.php.htm



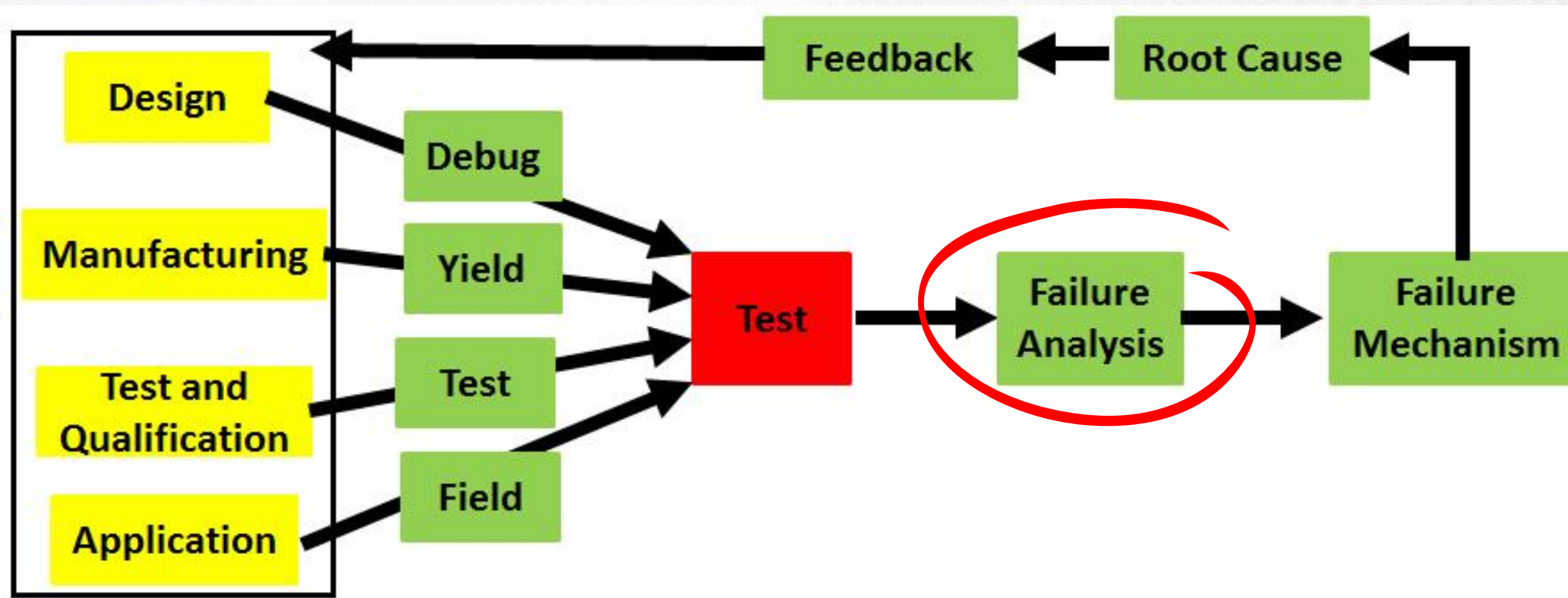
Source: McLellan, P., 2018. "WoW! TSMC Sticks Whole Wafers Together" https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/tsmc-placeholder

- Embedded interconnect bridge
 - Improved electrical performance between chiplets.



Source: Alcorn, P., 2017 "Hot Chips 2017: Intel Deep Dives Into EMIB". <https://www.tomshardware.com/news/intel-emib-interconnect-fpga-chiplet.35316.html>

IMPORTANCE OF FAILURE ANALYSIS (FA)



Source: http://www.sandia.gov/mstc/_assets/images/failure/intro.jpg

- Failure analysis is key to the product time-to-market cycle.
- Needed at every step of the market cycle → Iterative!
- Robust & efficient Failure Analysis is essential to having the highest possible die quality to make any KGD / advanced packaging approach work.

FAILURE MECHANISMS IN NEXT GENERATION PACKAGING TECHNOLOGIES

μ -bump

- Delamination
- Cracks
- Misalignment
- Shorts
- Damage in underlying MEOL
- Warpage

MCM Organic Package

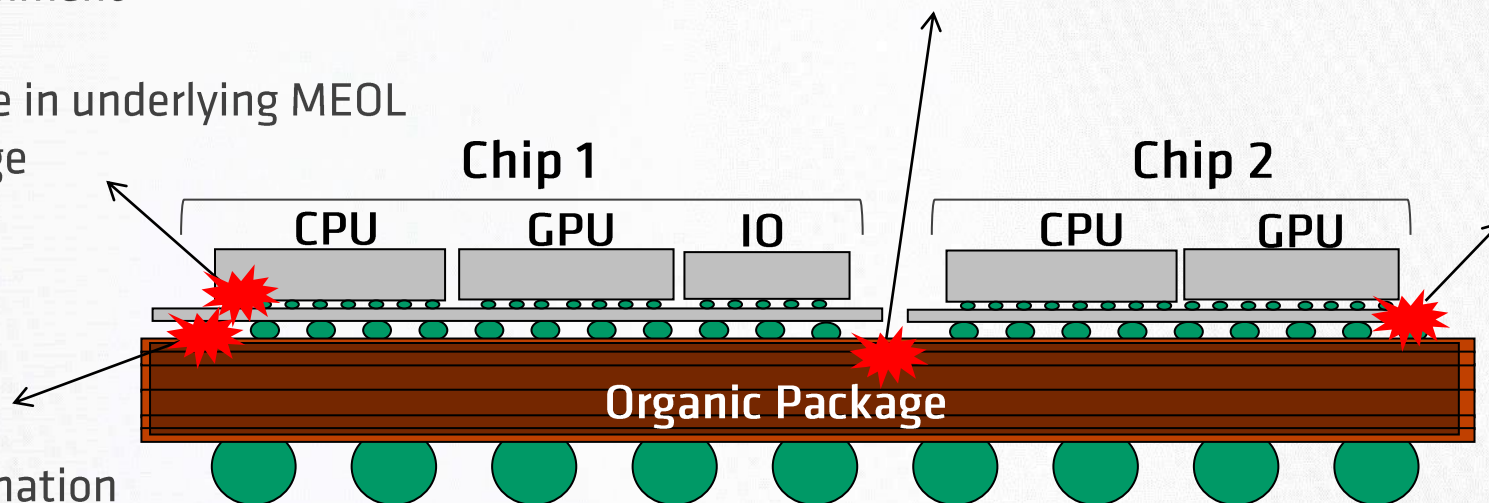
- Copper trace damage
- Cracks

Interposer/TSV

- Delamination
- Pin holes/ breakdown in liner
- Voids
- Cracks
- Electro migration

C4 Bump

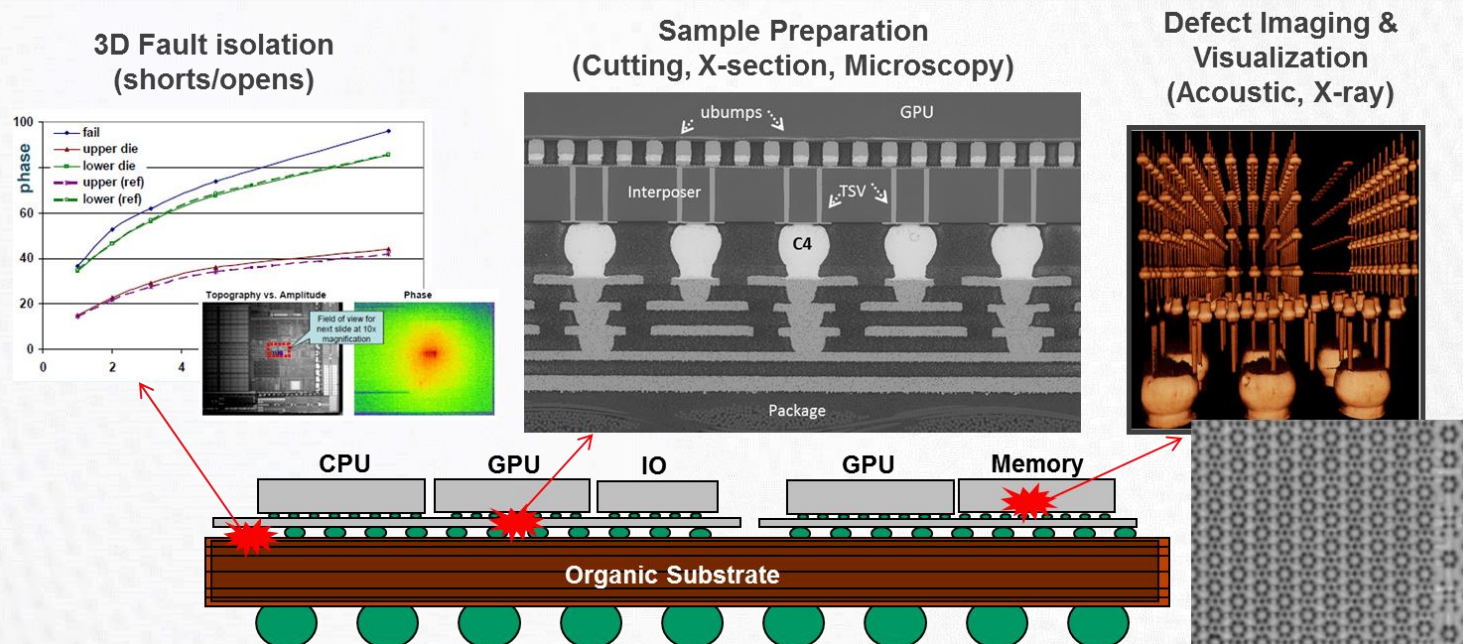
- Delamination
- Cracks
- Misalignment
- Shorts



- If there are defects, need to find them all.

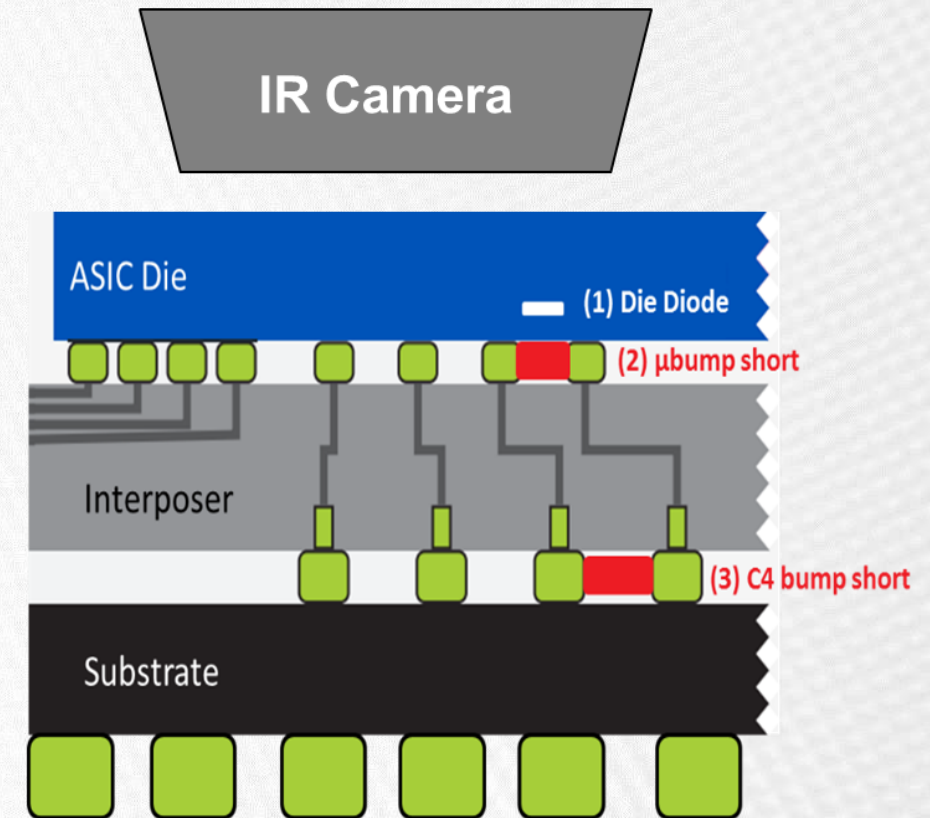
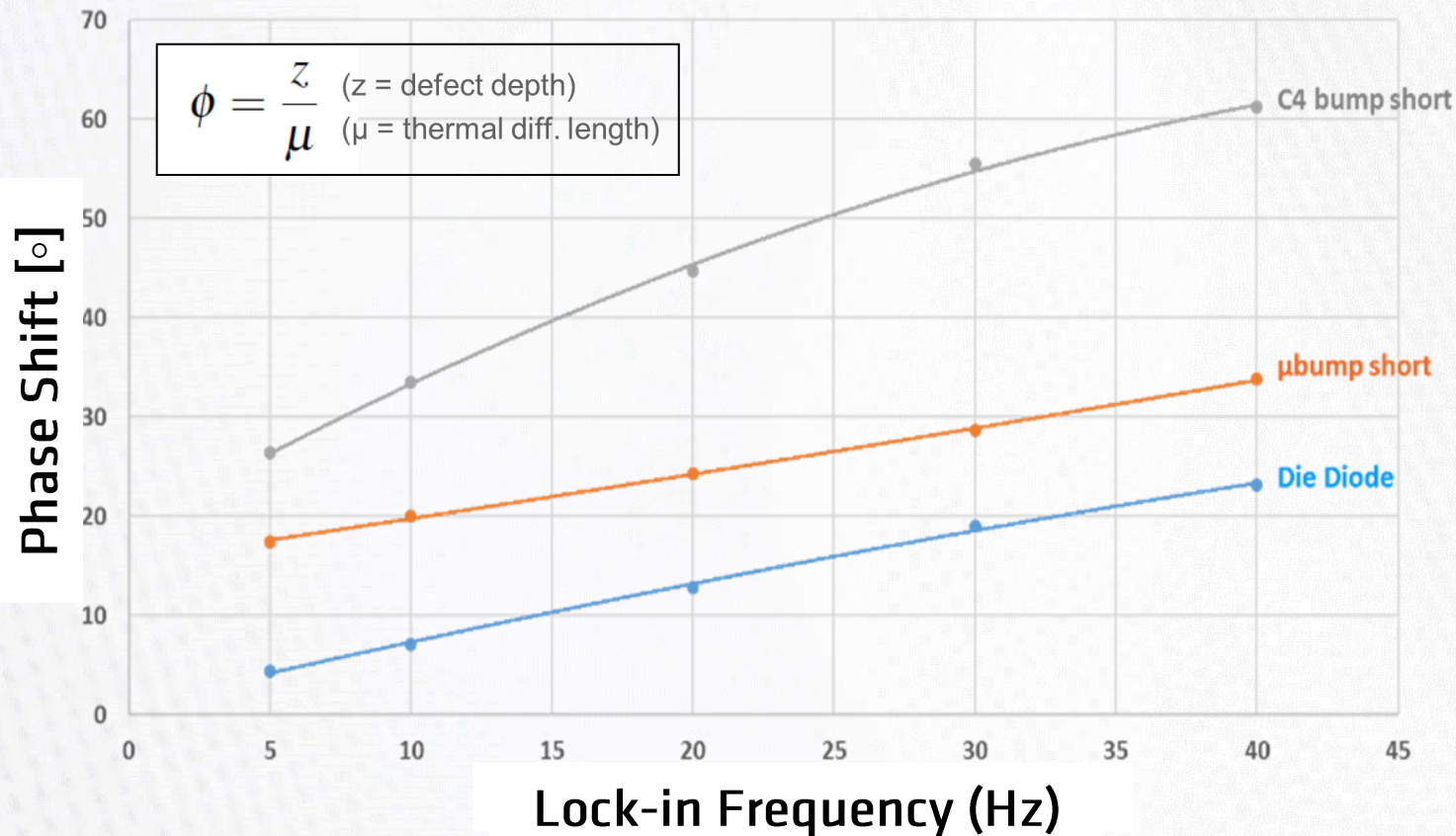
REQUIREMENTS FOR NEXT GEN PACKAGE FA

- Nondestructive Testing and Fault Isolation:
→ High Spatial / Axial Resolution; Improved Electrical Sensitivity.
- Nondestructive Defect Visualization Capabilities:
→ High Spatial / Axial Resolution; Acquisition Speed.
- New Sample Preparation and Materials Characterization Methodologies:
→ High Precision and Throughput; Improved Analytical Sensitivity.
- Time to results / resolution limitations / sensitivity limitations / cost of ownership?



LOCK-IN THERMOGRAPHY (IR-LIT)

Defect Z-depth Determination Using Lock-in Thermography for Stacked Devices:

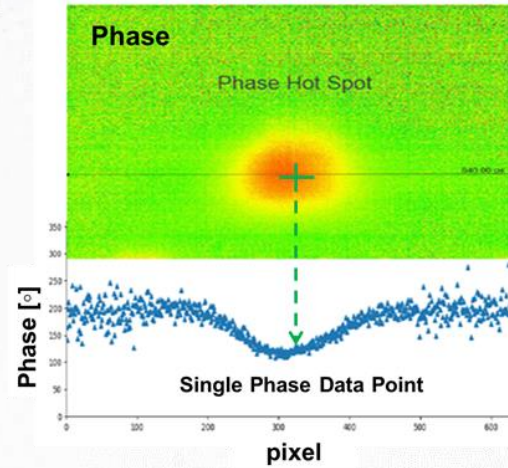
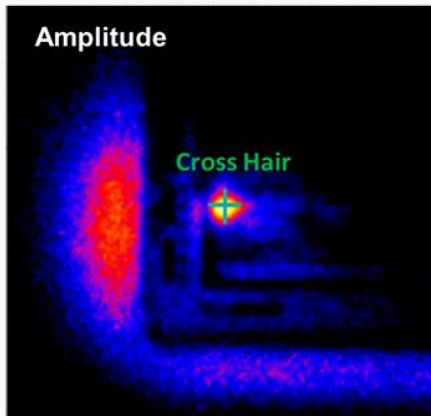


Source: Zee, B. *et al.*, ISTFA 2018. "Improved Phase Data Acquisition for Thermal Emissions Analysis of 2.5D IC"

- Phase Shift (ϕ) is used to calculate defect depth.
- Challenge: how to improve phase data acquisition consistency, accuracy, and time to results?

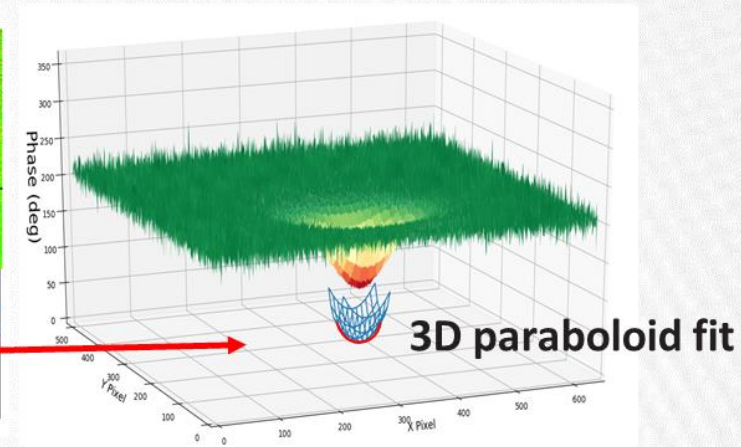
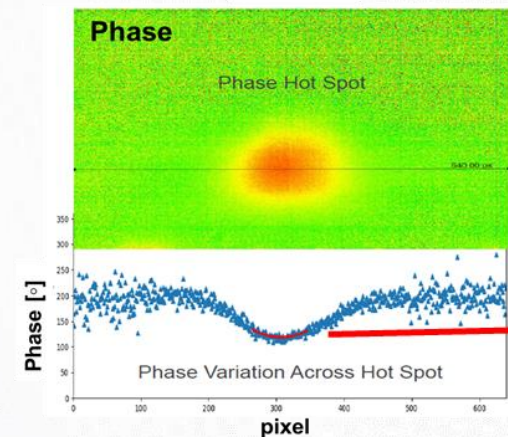
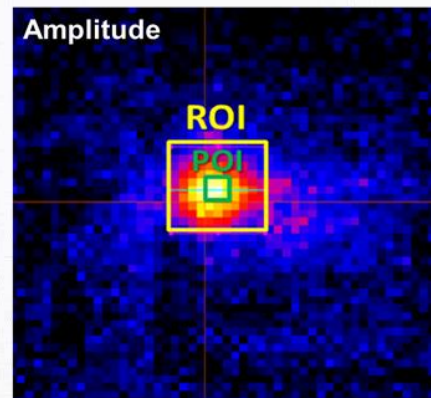
LOCK-IN THERMOGRAPHY (IR-LIT)

Legacy Software



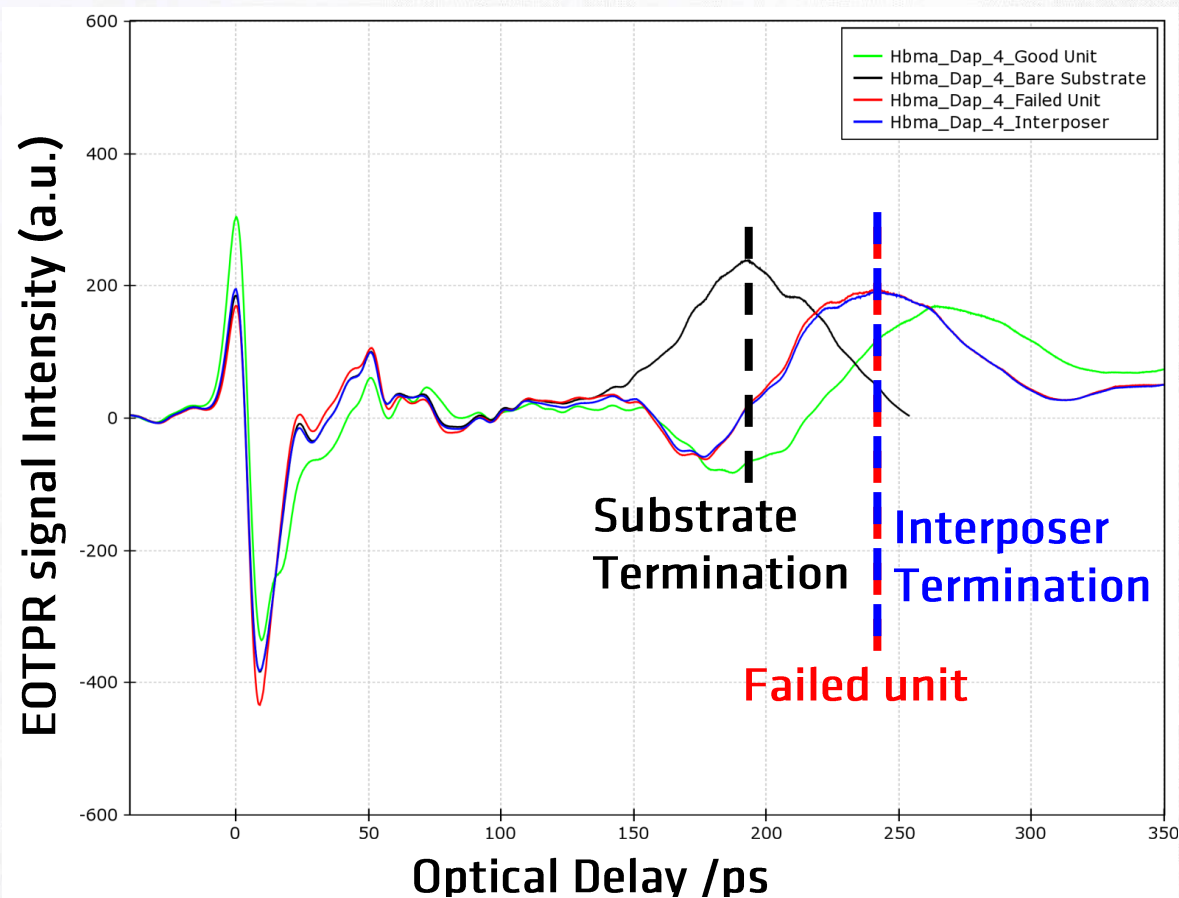
Source: Zee, B. *et al.*, ISTFA 2018. "Improved Phase Data Acquisition for Thermal Emissions Analysis of 2.5D IC"

Express 3D Software



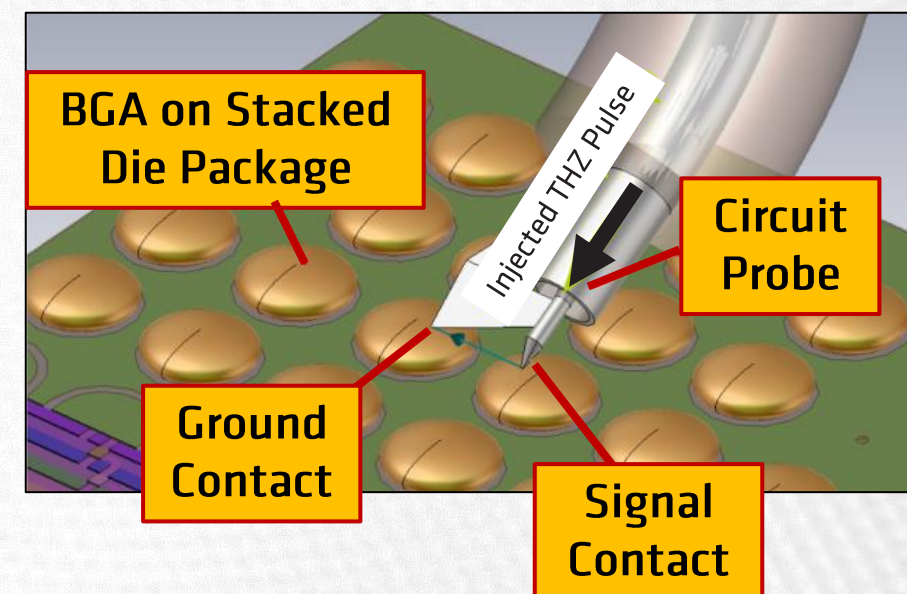
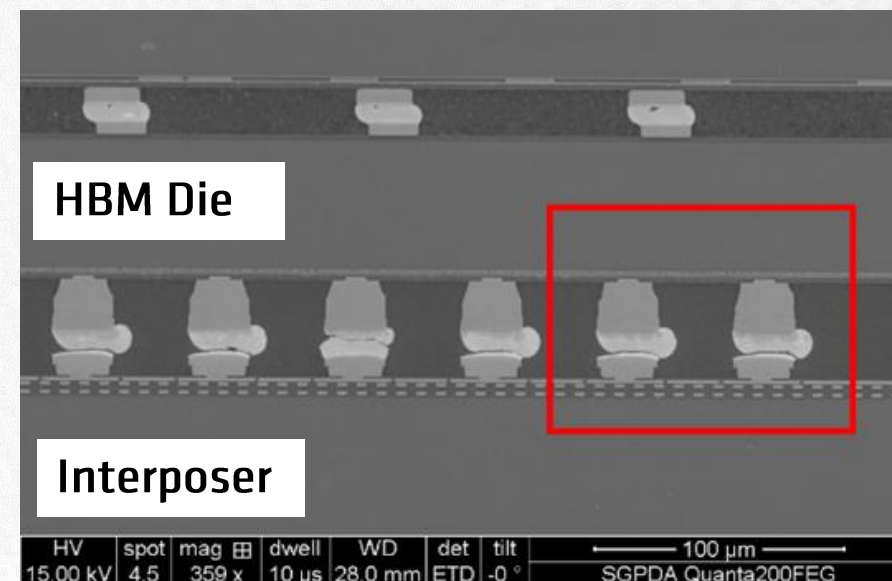
- Real-time 3D parabolic curve fitting automatically extracts the lowest calculated phase value.
- Auto-stop lock-in measurements when a pre-defined goodness of fit is reached.

ELECTRO OPTICAL TERAHERTZ PULSE REFLECTOMETRY (EOTPR)



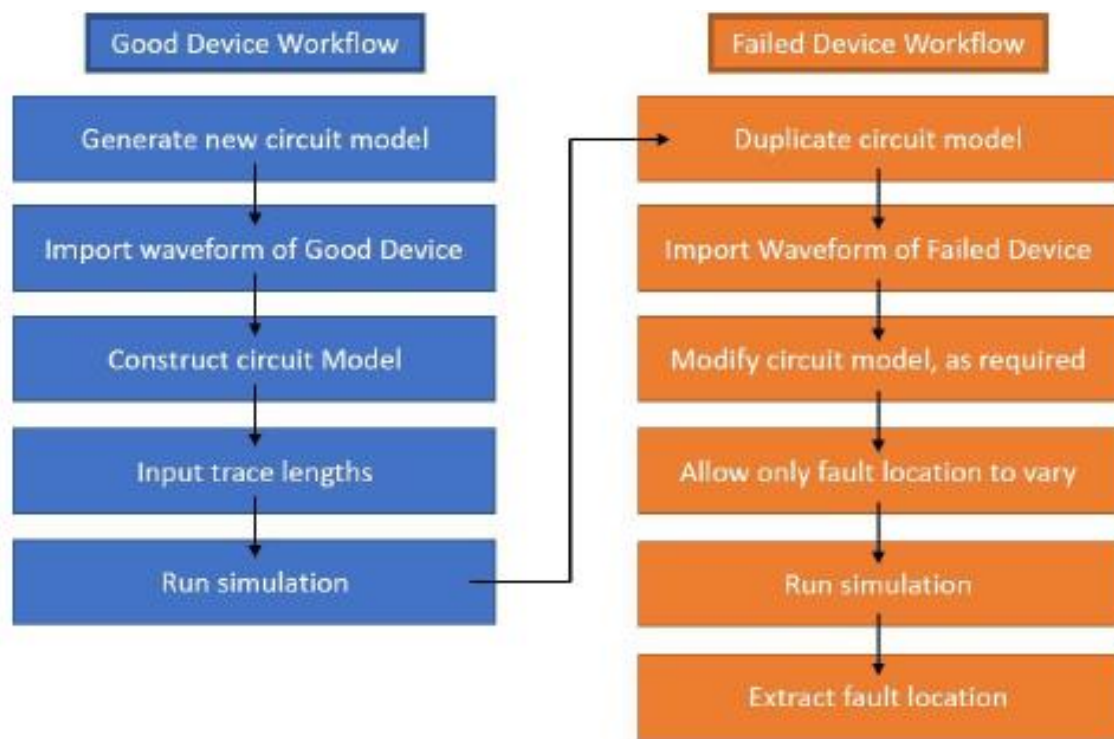
Source: Alton, J. *et al.*, ISTFA 2017. "Non-Destructive Fault Localization in 2.5D Packages Using Electro Optical Terahertz Pulse Reflectometry".

- Fault location is determined by measuring the time of flight to a suspect peak in the waveform.
- Challenge: how to find references for comparison?

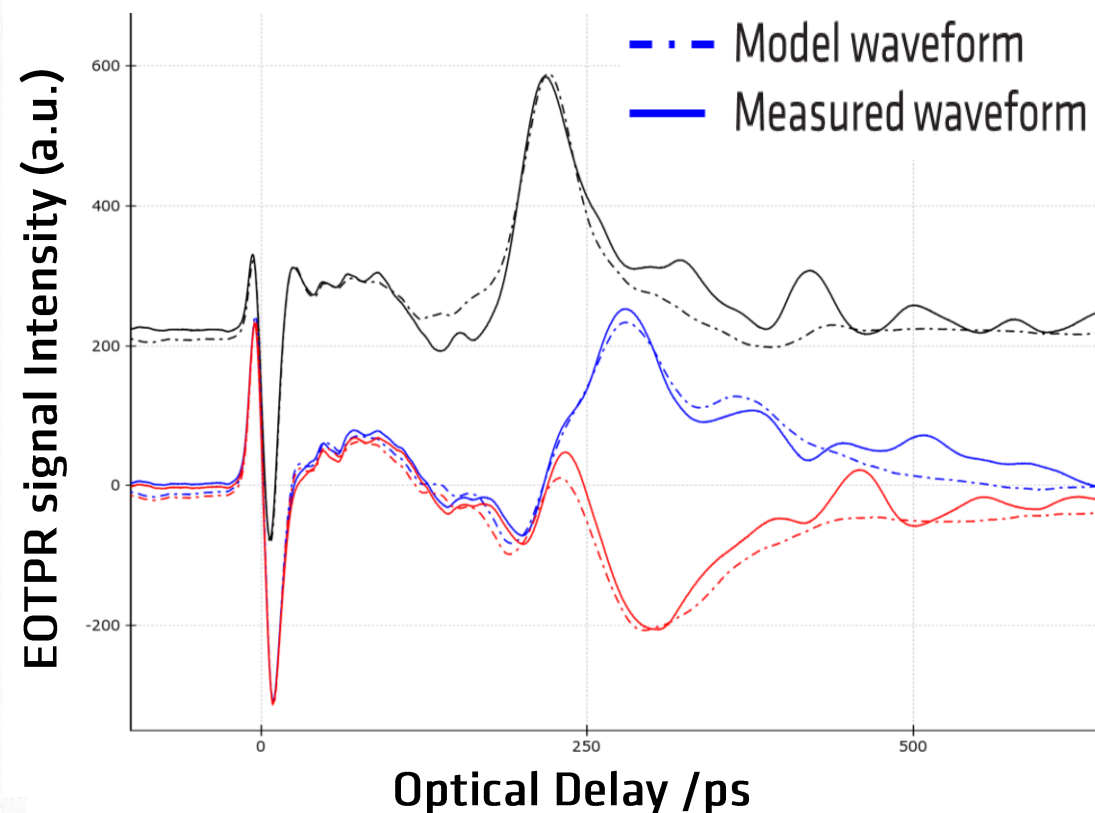


EOTPR – WAVEFORM SIMULATION TO ESTIMATE DEFECT LOCATION

Simulation workflow overview



Waveform comparison

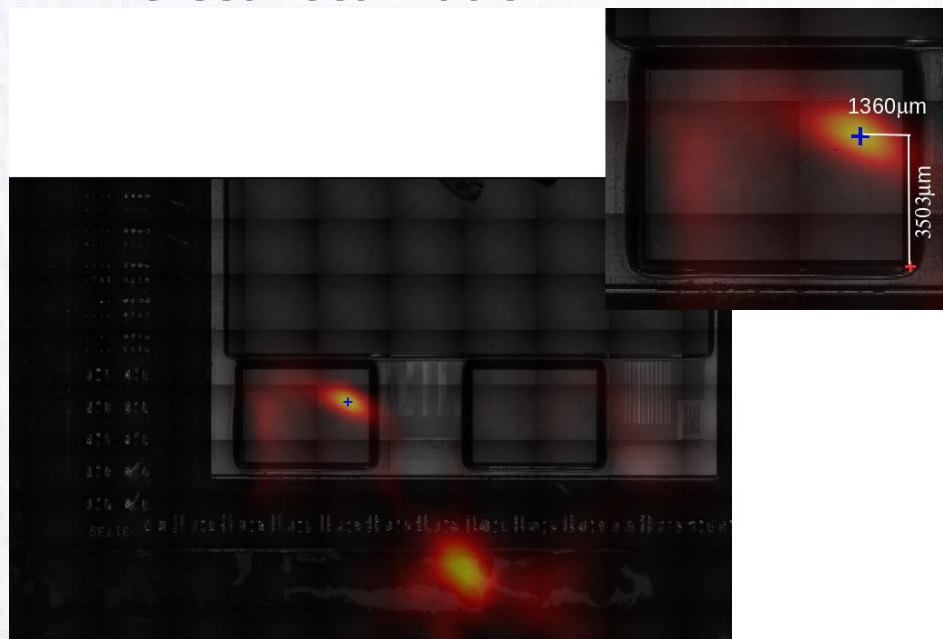


- Known good device (KGD) used to generate model using lumped circuit elements → trace length inputted to generate simulated waveform to match KGD waveform.
- Waveform of failed device is measured, and software runs simulation to fit and extract fault location after waveform optimization.

MAGNETIC FIELD IMAGING

Magnetic Field Imaging (MFI) 3D Path Solver:

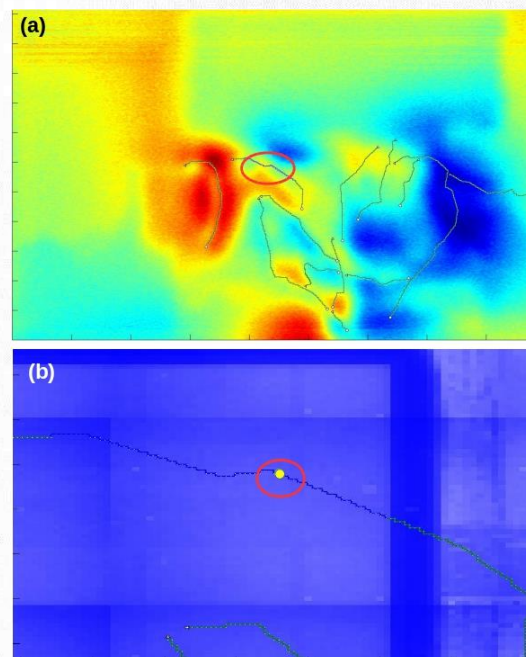
XY Defect Localization:



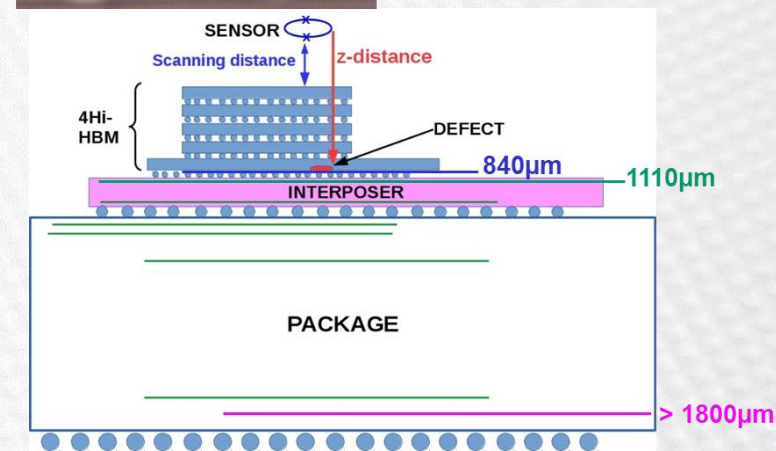
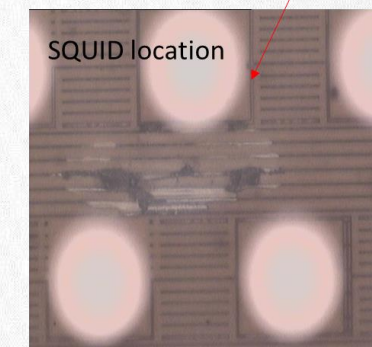
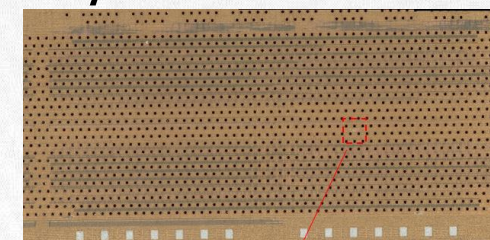
Source: Orozco, A., *et al.*, ISTFA 2016. "3D Fault Isolation in 2.5D Device comprising High Bandwidth Memory (HBM) Stacks and Processor Unit Using 3D Magnetic Field Imaging".

- Using a current path extracted from the current density image as a starting point, the 3D solver adjusts that path in a way that matches the observed magnetic field in the acquired scans.
- From these adjustments, a true 3D current path can be constructed.

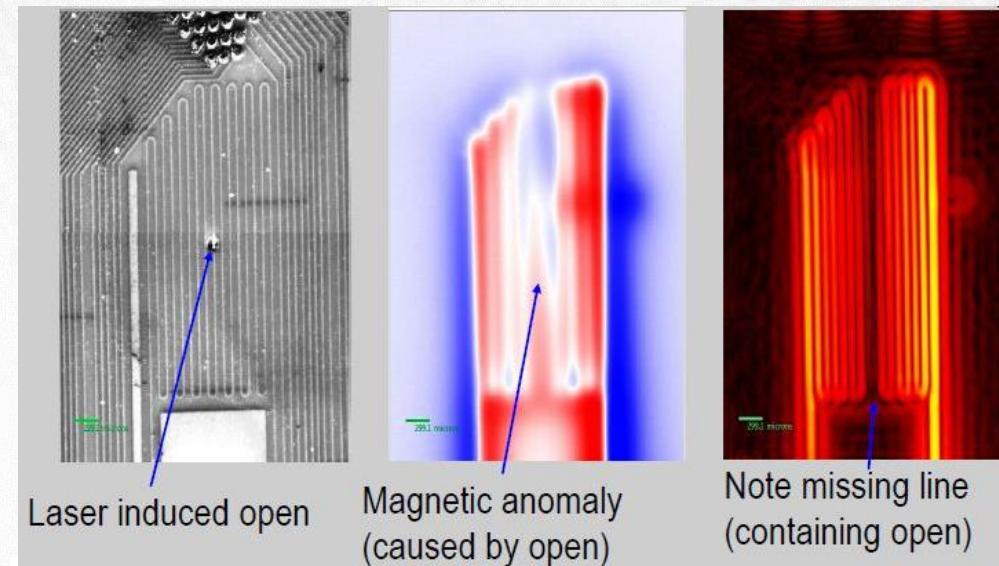
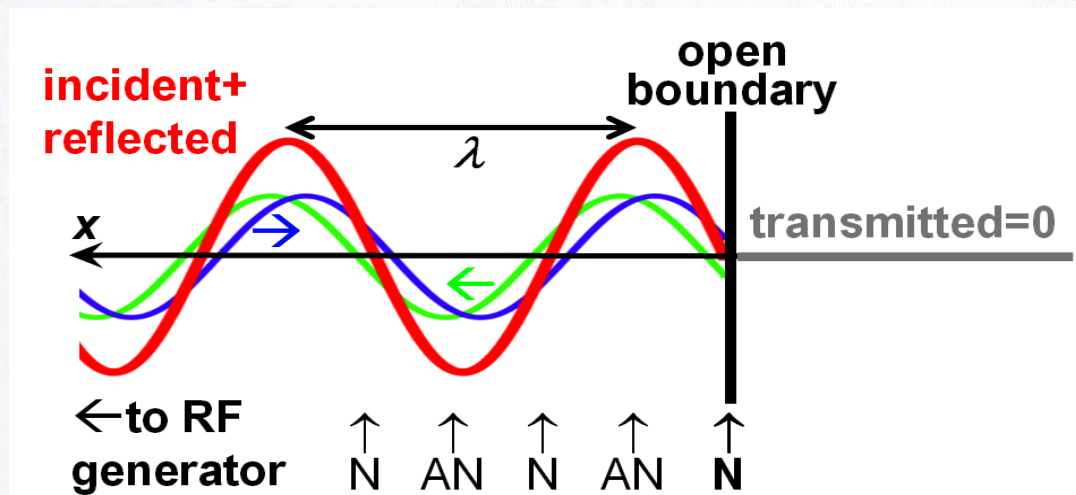
Z Defect Localization:



Physical Failure Analysis:



SPACE DOMAIN REFLECTOMETRY (SDR)

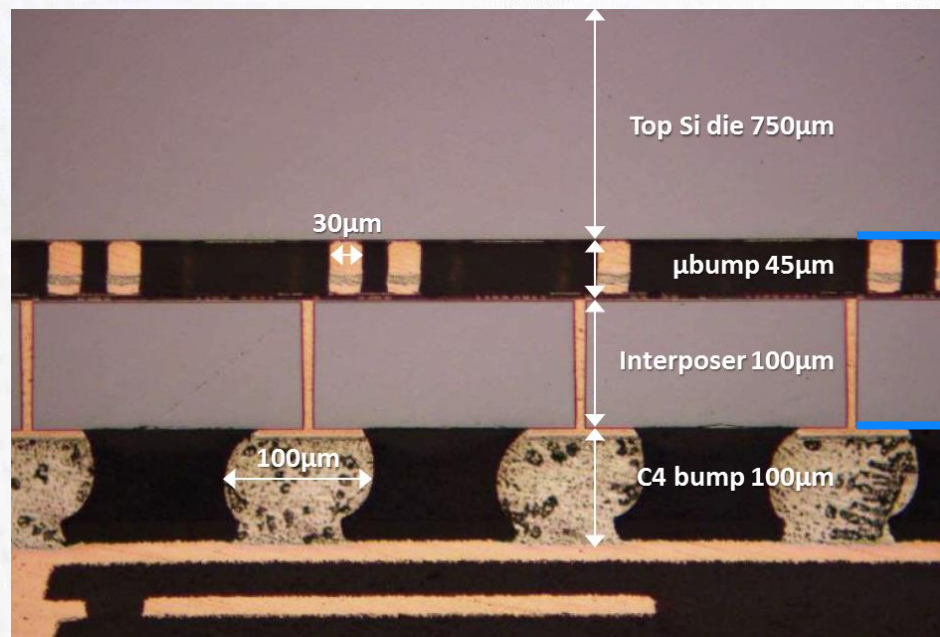


Source: Gautestad, J., *et al.*, IPFA 2012. "Space Domain Reflectometry for open failure localization".

- Space-domain reflectometry (SDR) utilizing SQUID sensor is a FA technique for open fault isolation that directly displays a physical 2D image of an open failures.
- A continuous wave RF signal is injected into the defective trace and the sensor acquires a 2D image of the induced RF magnetic field.
- At RF frequencies the open impedance, Z_{open} (typically in $M\Omega$ range), is much greater than the trace characteristic impedance, Z_0 ($\sim 50\Omega$), thus, the open boundary reflects back nearly all the incident power while no RF power is transmitted past the open.

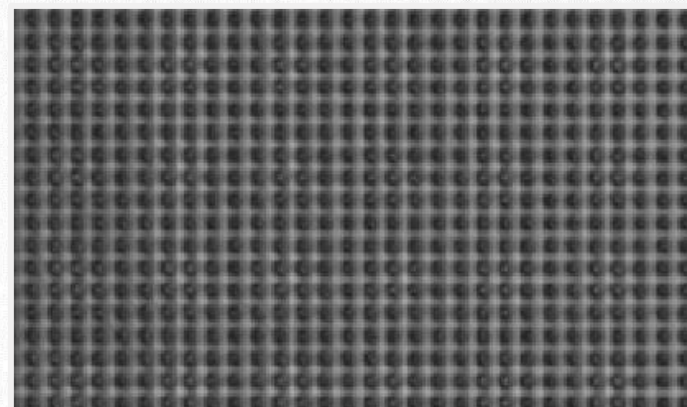
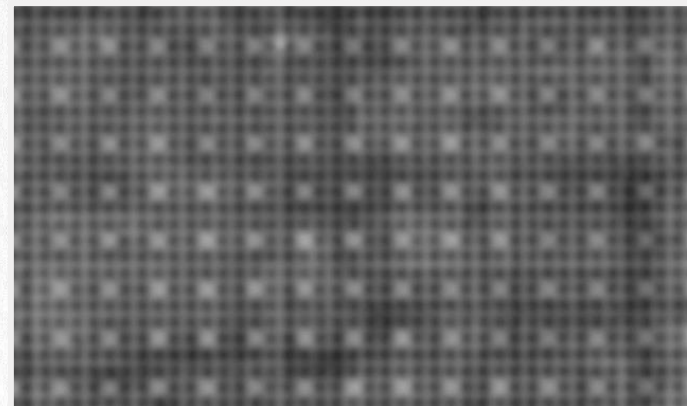
ACOUSTIC IMAGING

Optimization of Acoustic Imaging for High Resolution imaging:



Silicon/μ-bump interface

Interposer/C4-bump interface

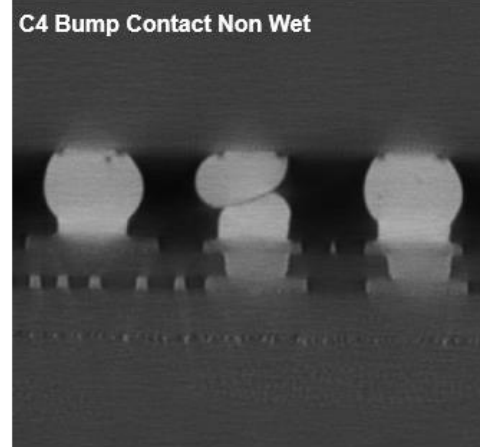
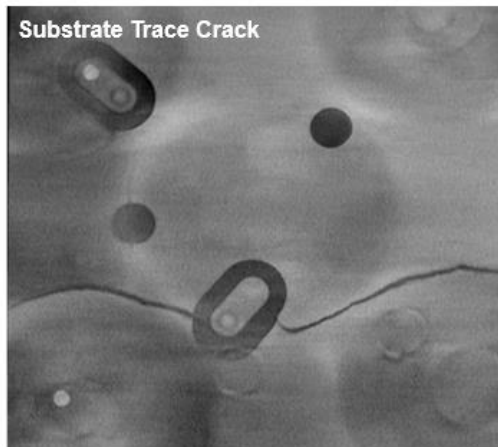
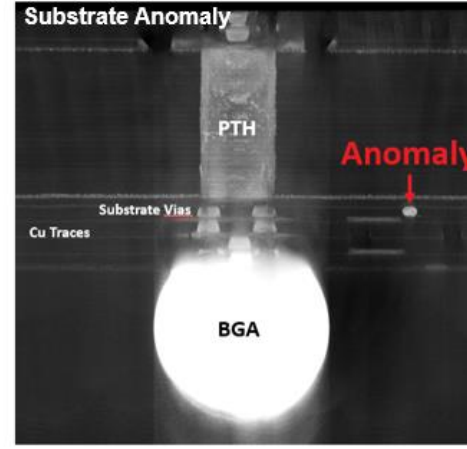
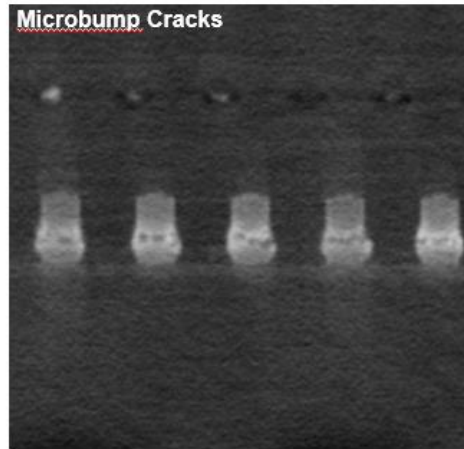
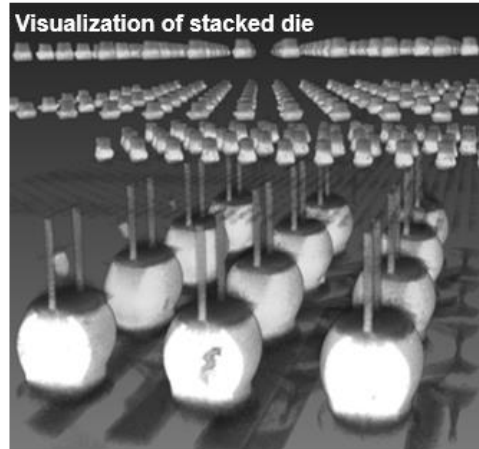


Source: Oh, Z.Y. *et al.*, IPFA 2018. "Optimization and Application of Acoustic Imaging for Defect Detection in Stack Die Packages".

- High speed data processing.
- Mid high- f broadband transducer.
- Minimize water path between transducer and sample.
- Constant TOF during scan.
- Challenge: how to image through a memory stack to the μ-bump interface?

3D X-RAY MICROSCOPY

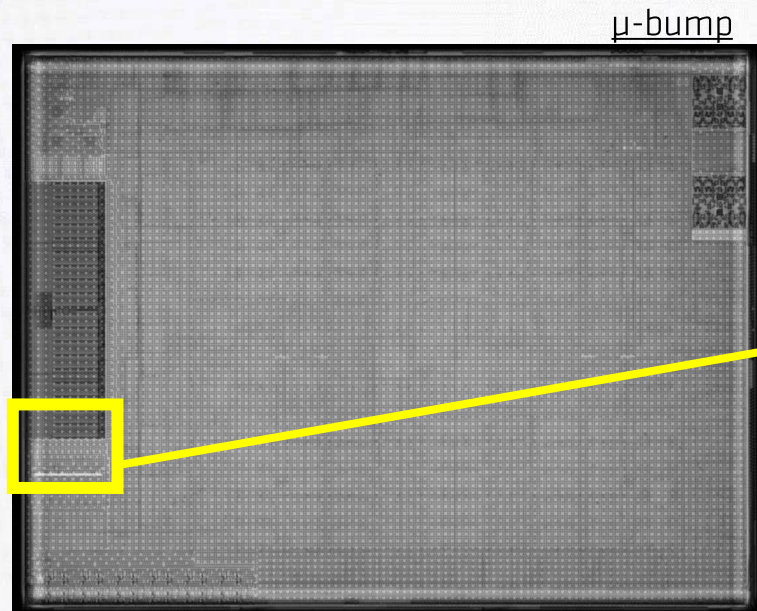
Nondestructive High Resolution Imaging with 3D X-Ray Microscopy:



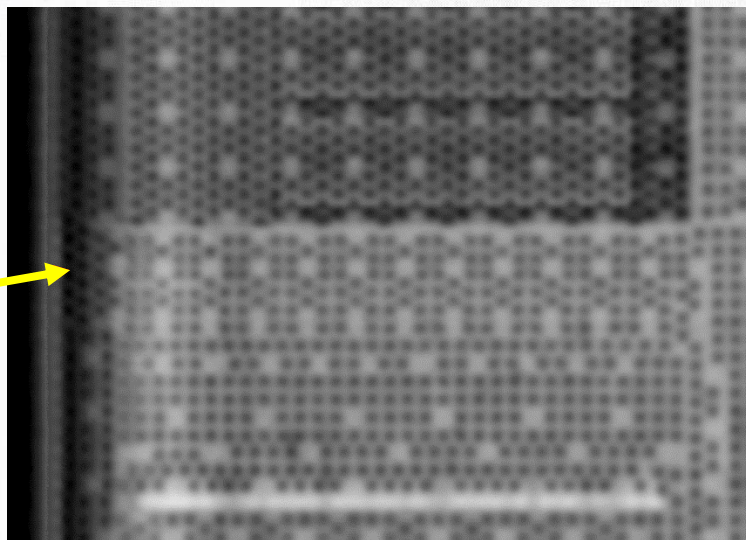
- Nondestructive high resolution image of internal structures and defects.
- Locate and isolate defects difficult to find with traditional FA techniques.
- Challenge: how to get faster time to results and better resolution for smaller features?

Source: Md Zulkifli, S., *et al.*, IPFA2017. "High-Res 3D X-ray Microscopy for Non-Destructive Failure Analysis of Chip-to-Chip Micro-bump Interconnects in Stacked Die Packages

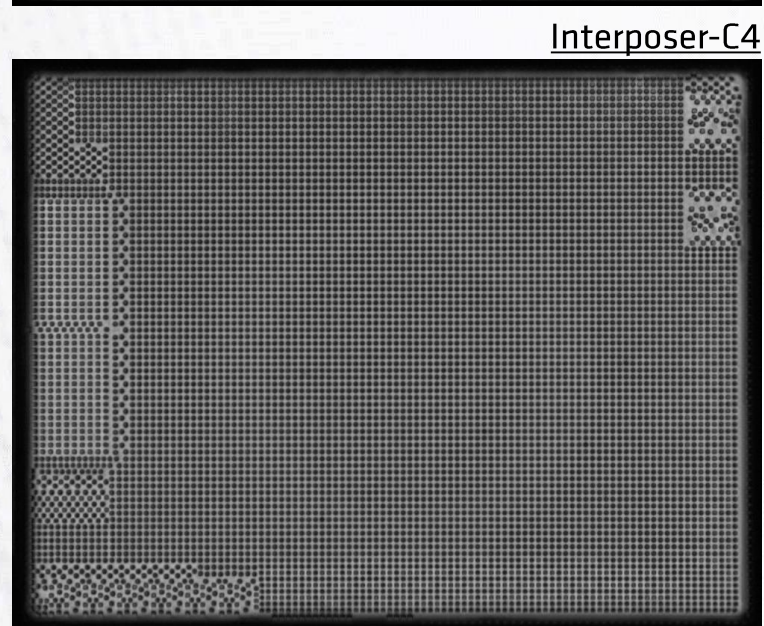
CASE STUDY 1 – SHORT FAILURE (CSAM/LIT)



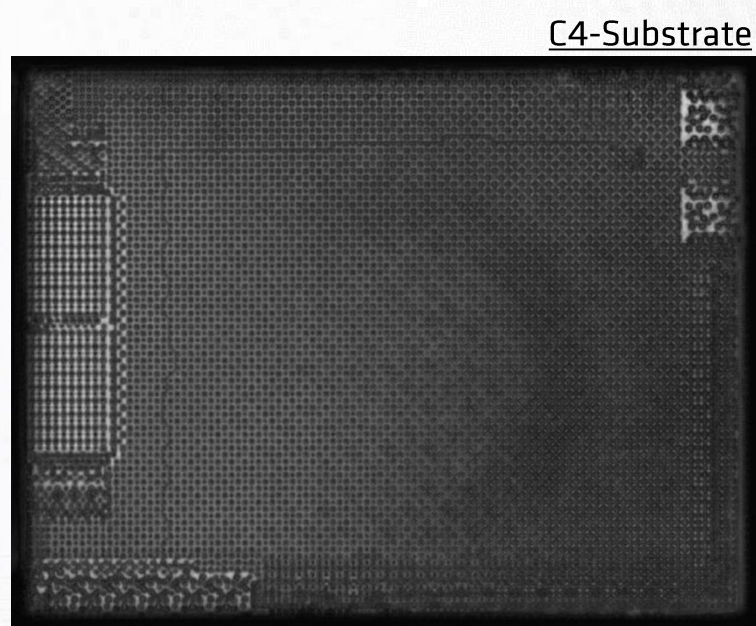
μ -bump



- No significant anomaly was observed in the unit under CSAM.



Interposer-C4

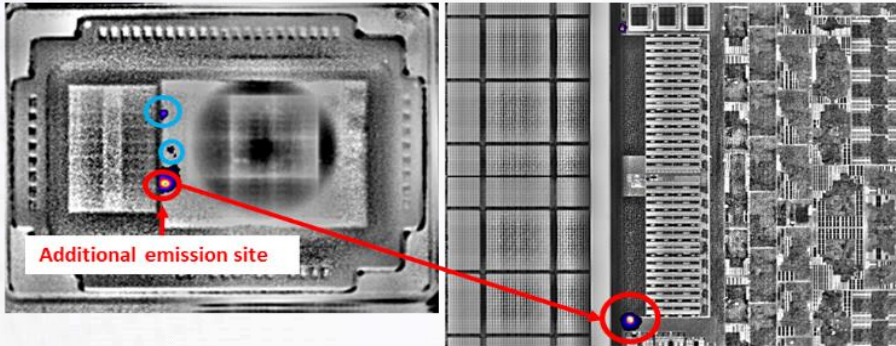


C4-Substrate

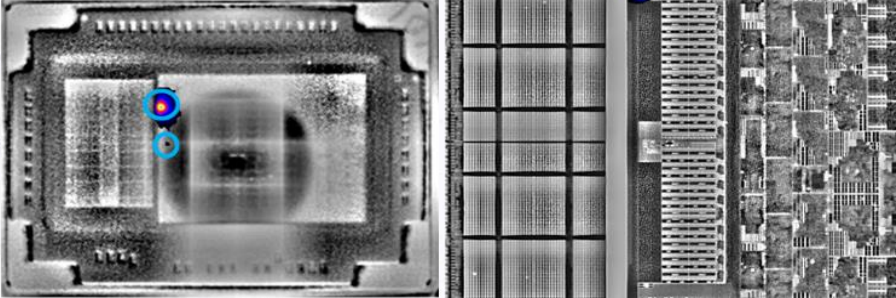
CASE STUDY 1 – SHORT FAILURE (CSAM/LIT)

Thermal Emission (LIT) Site in XY space detected in full camera frame:

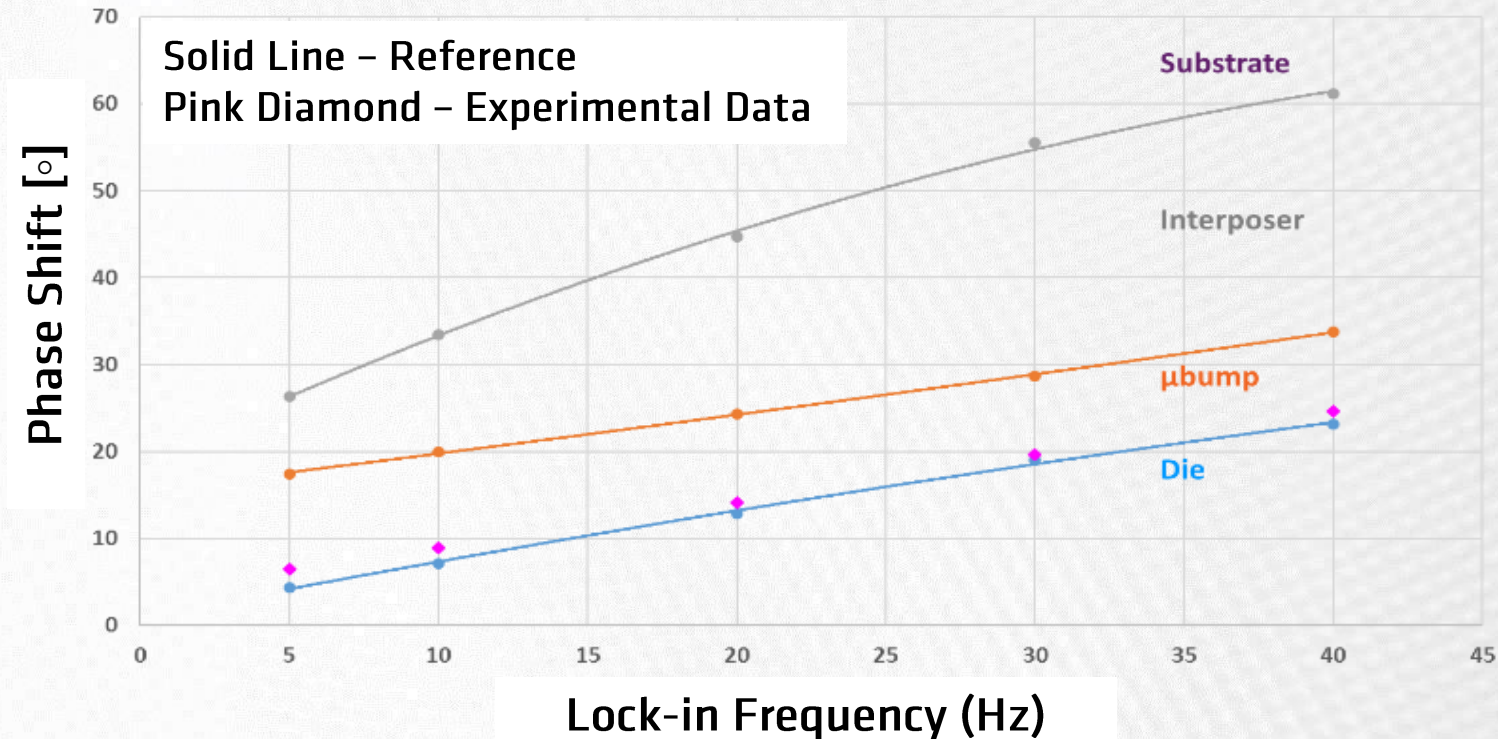
Reject unit:



Good unit:



Phase shift measurement results for Z depth localization:



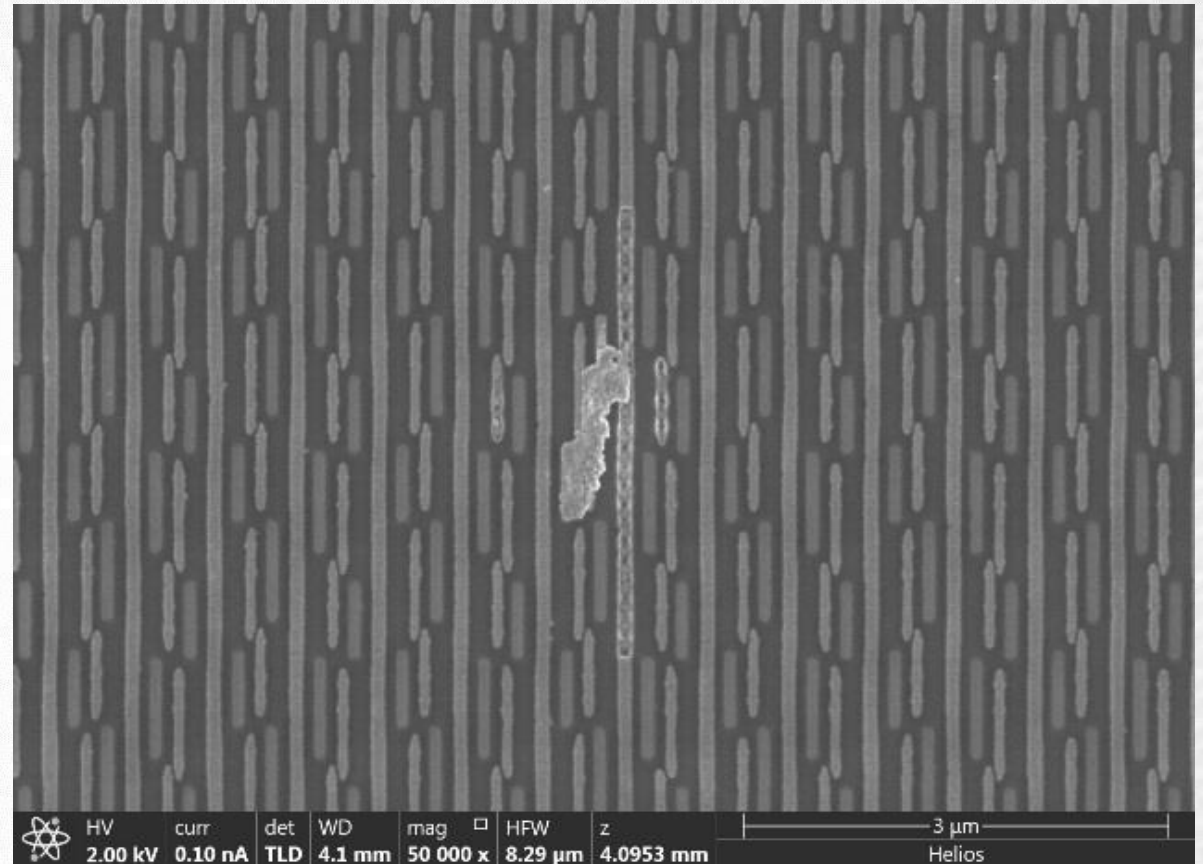
- Phase shift measurement results: defect was possibly located in the die metal and/or active circuitry.

CASE STUDY 1 – SHORT FAILURE (CSAM/LIT)

TIVA:



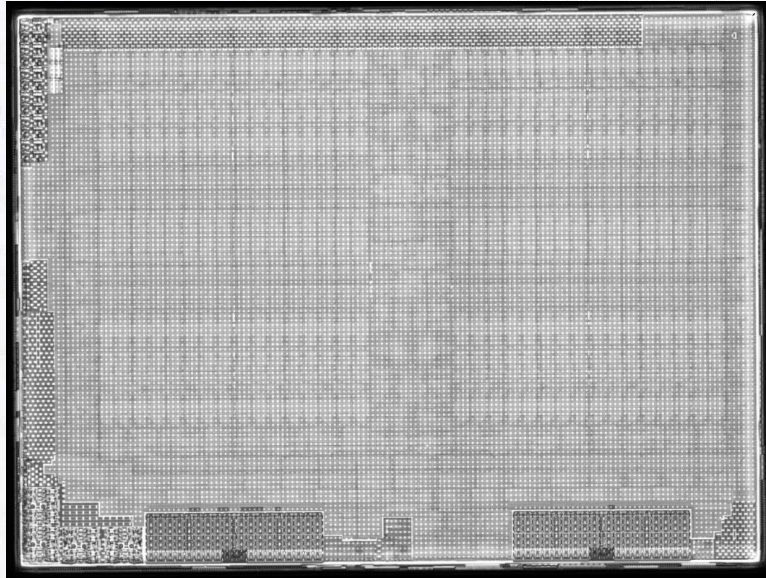
PFA results:



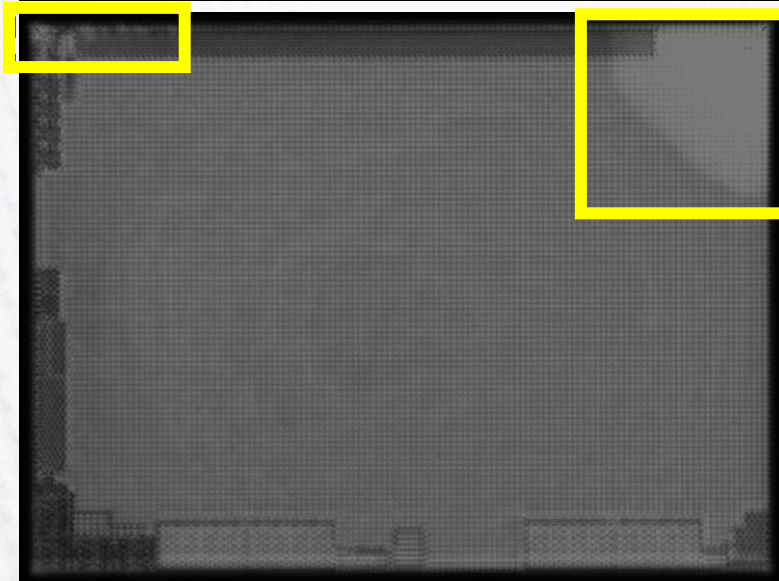
- Root cause: M3 metal damage.

CASE STUDY 2 – SHORT FAILURE (CSAM/LIT/3D X-RAY)

μ-bump



- Delamination was observed under CSAM inspection.



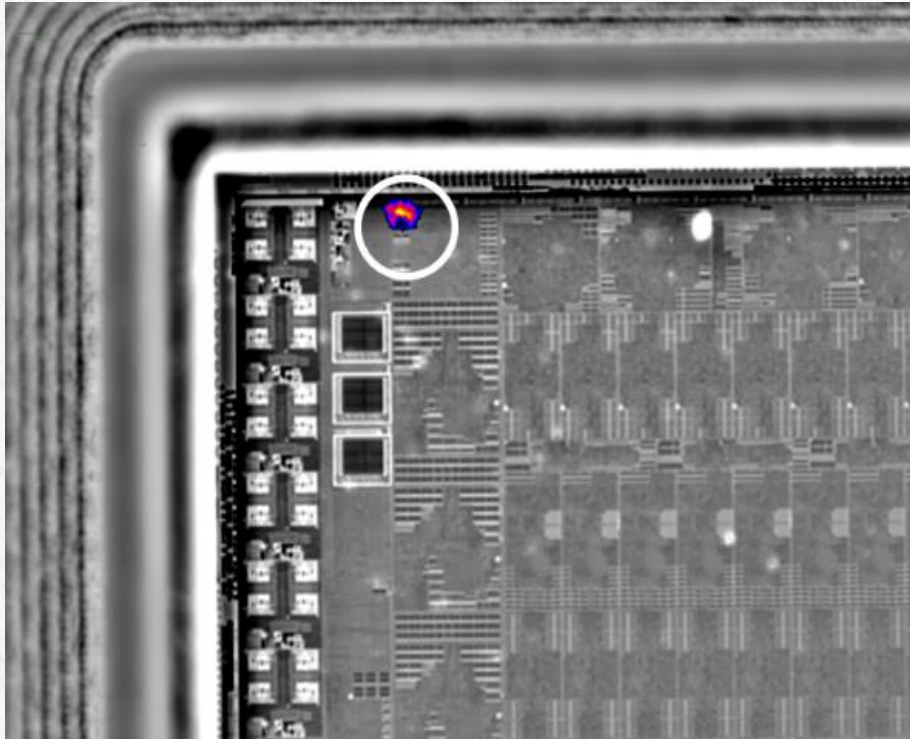
Interposer-C4



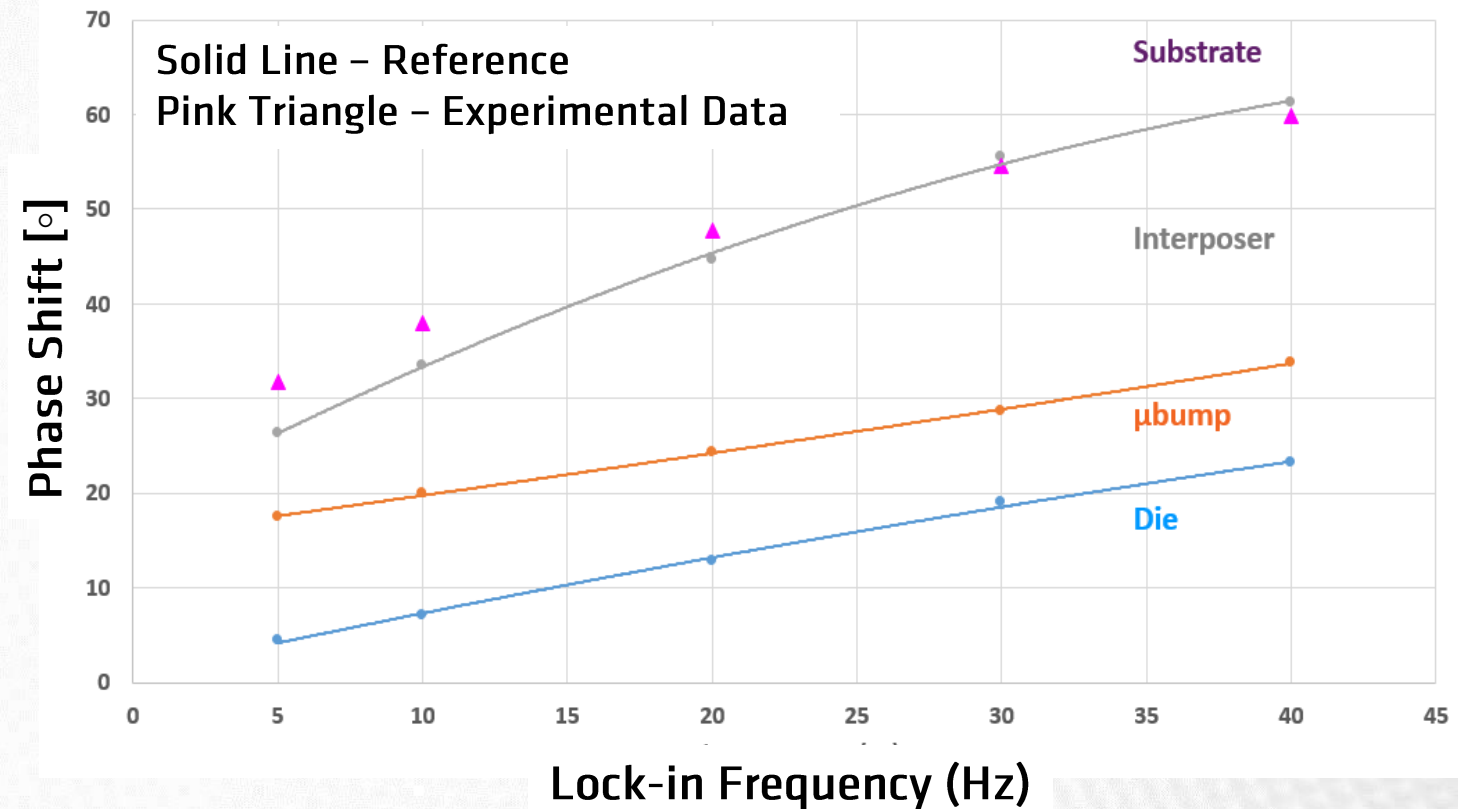
C4-Substrate

CASE STUDY 2 – SHORT FAILURE (CSAM/LIT/3D X-RAY)

Thermal Emission Site (LIT) in XY space detected in full camera frame:

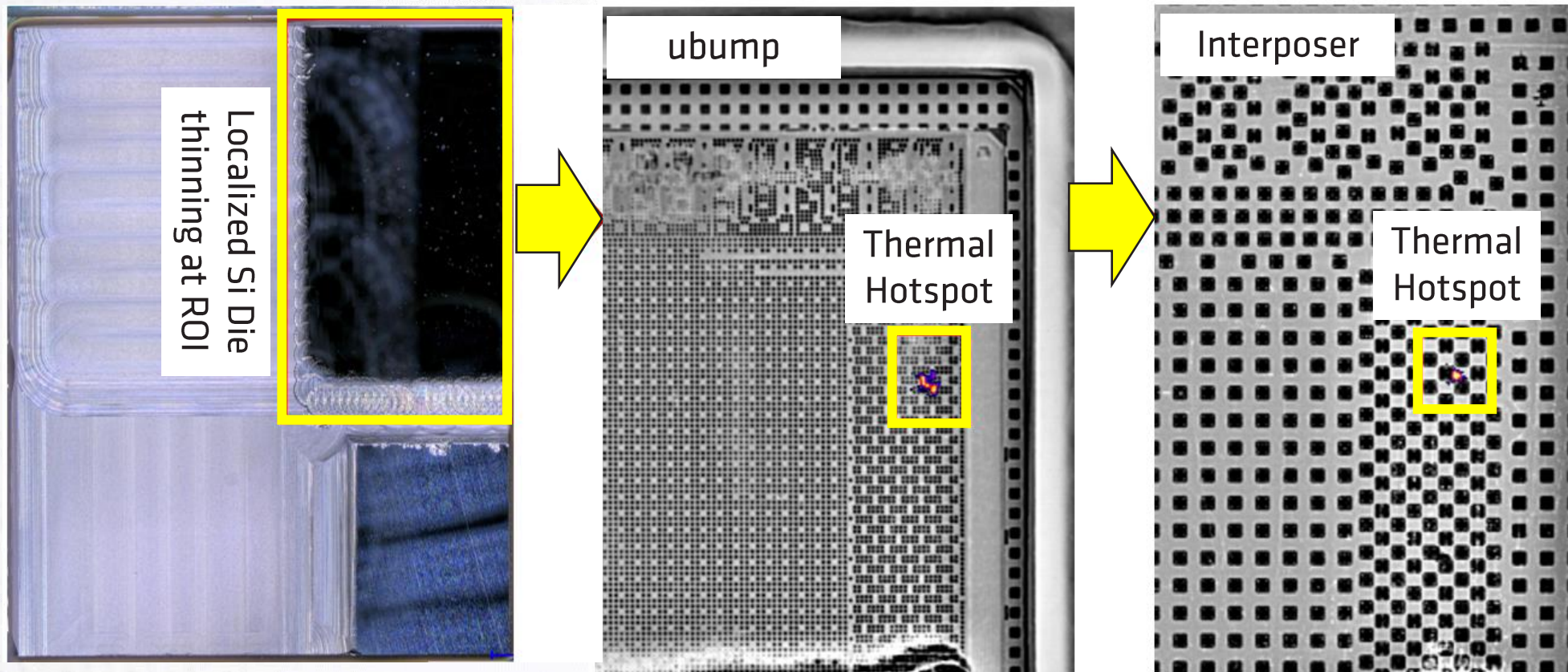


Phase shift measurement results for Z depth localization:



- Phase shift measurement results: defect was possibly located at C4 bump interface.

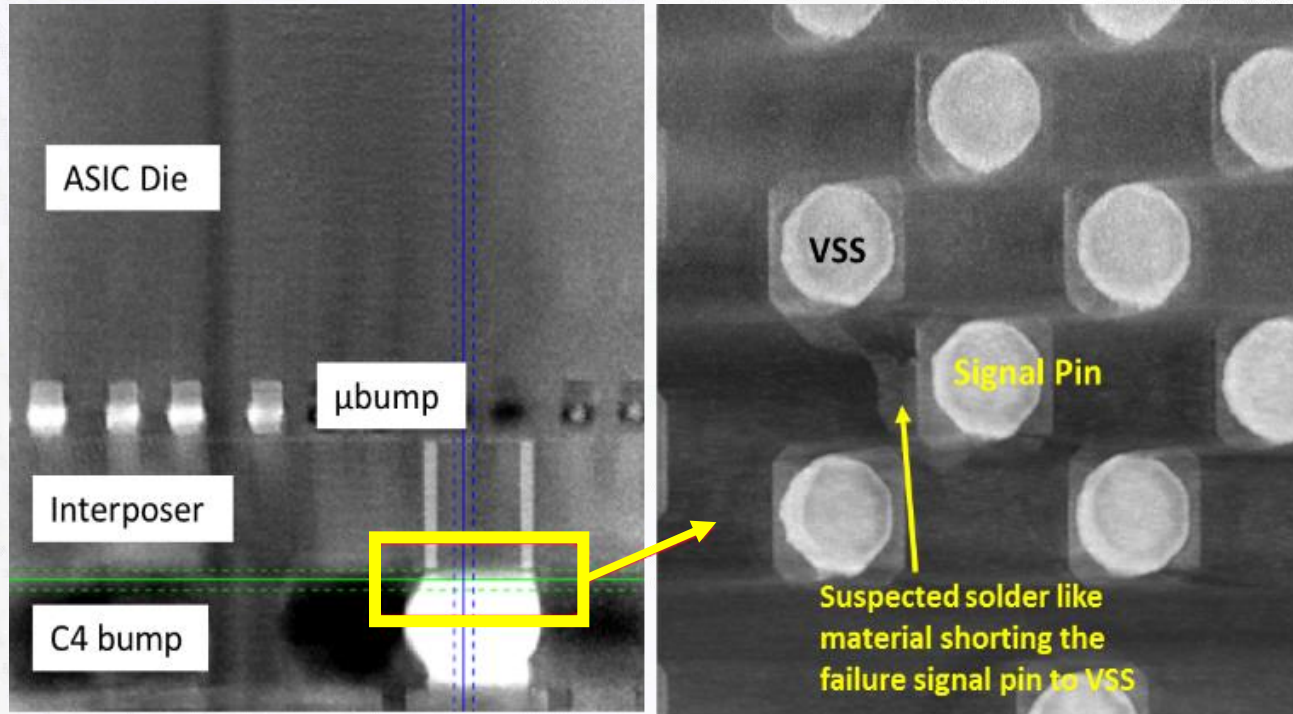
CASE STUDY 2 – SHORT FAILURE (CSAM/LIT/3D X-RAY)



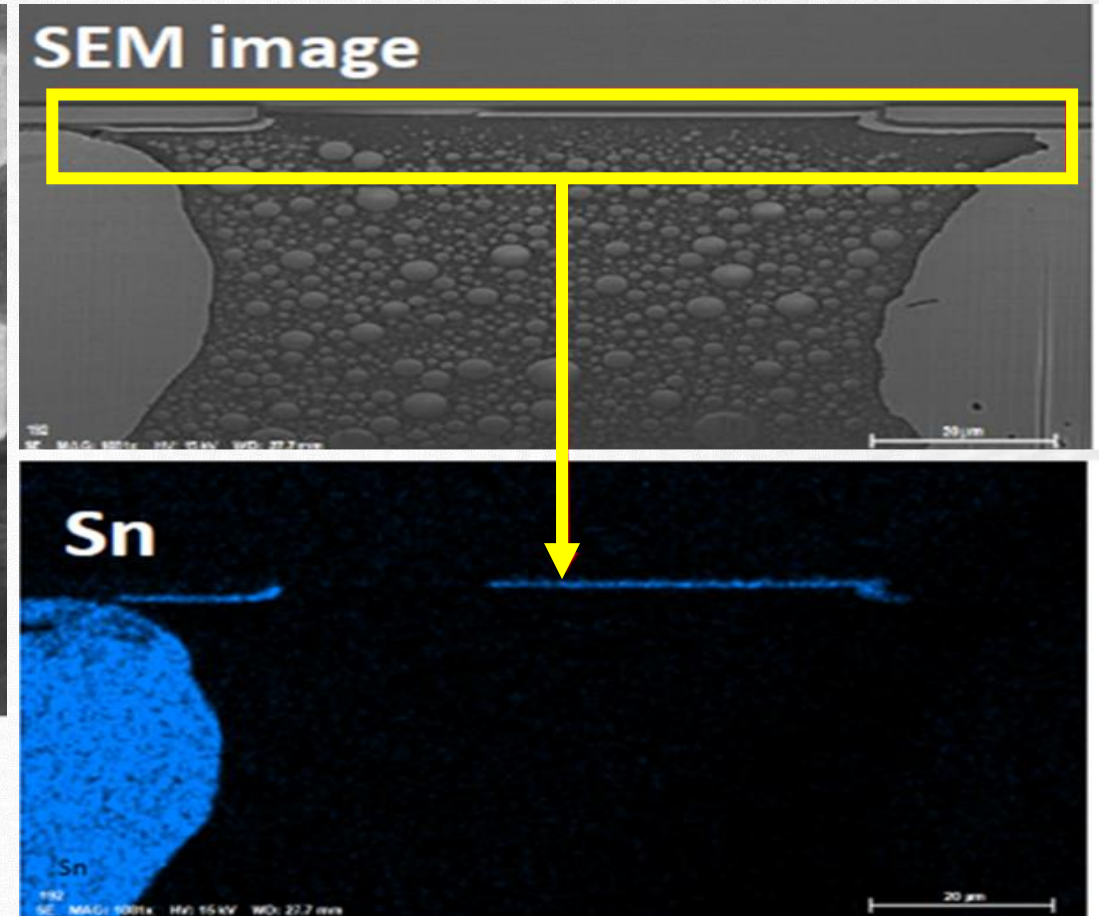
- Possible to do further isolation without having to create a theoretical phase shift model in LIT.
- Do iterative Si thinning at region of interest (ROI) and LIT was done until a more distinct thermal hotspot size was observable.

CASE STUDY 2 – SHORT FAILURE (CSAM/LIT/3D X-RAY)

3D X-ray results:

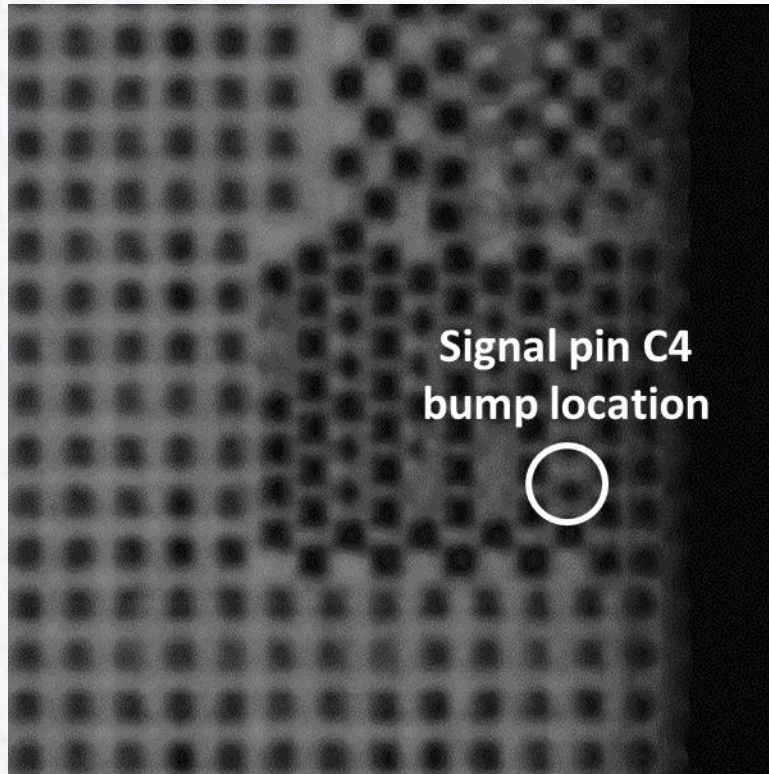


PFA results:

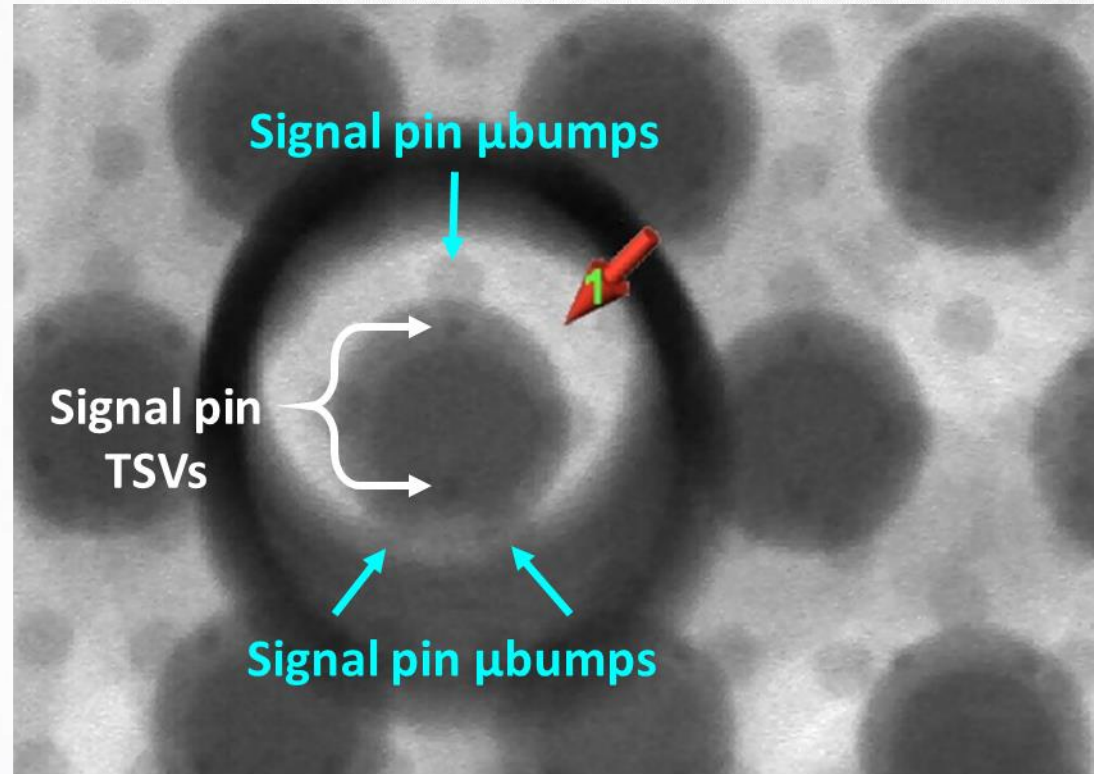


- Root cause: Solder flow into passivation/UF delamination.

CASE STUDY 3 – OPEN FAILURE (CSAM/EOTPR/3D X-RAY)



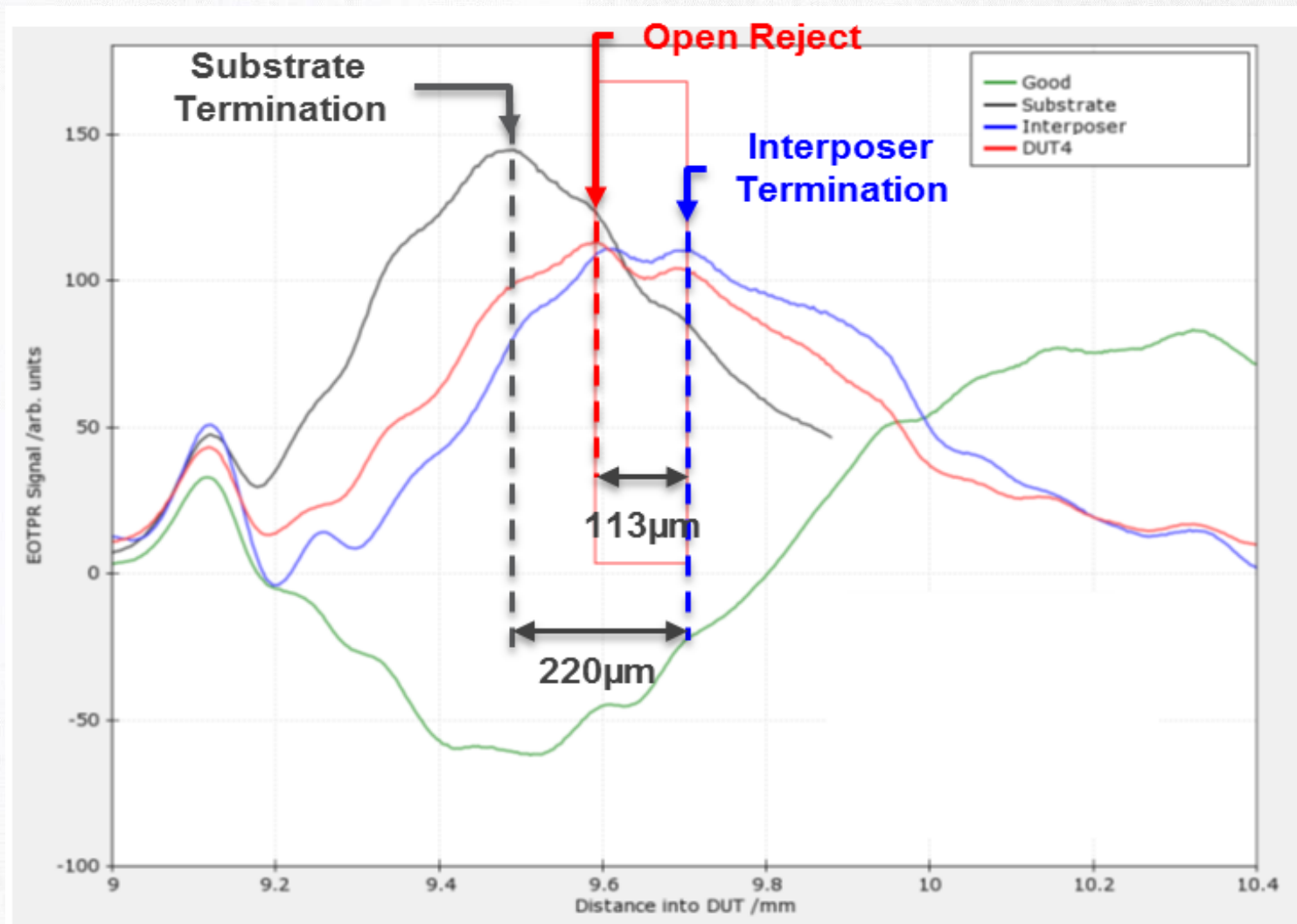
(a)



(b)

- No anomaly observed in CSAM and 2D RTX at associated failure bumps.

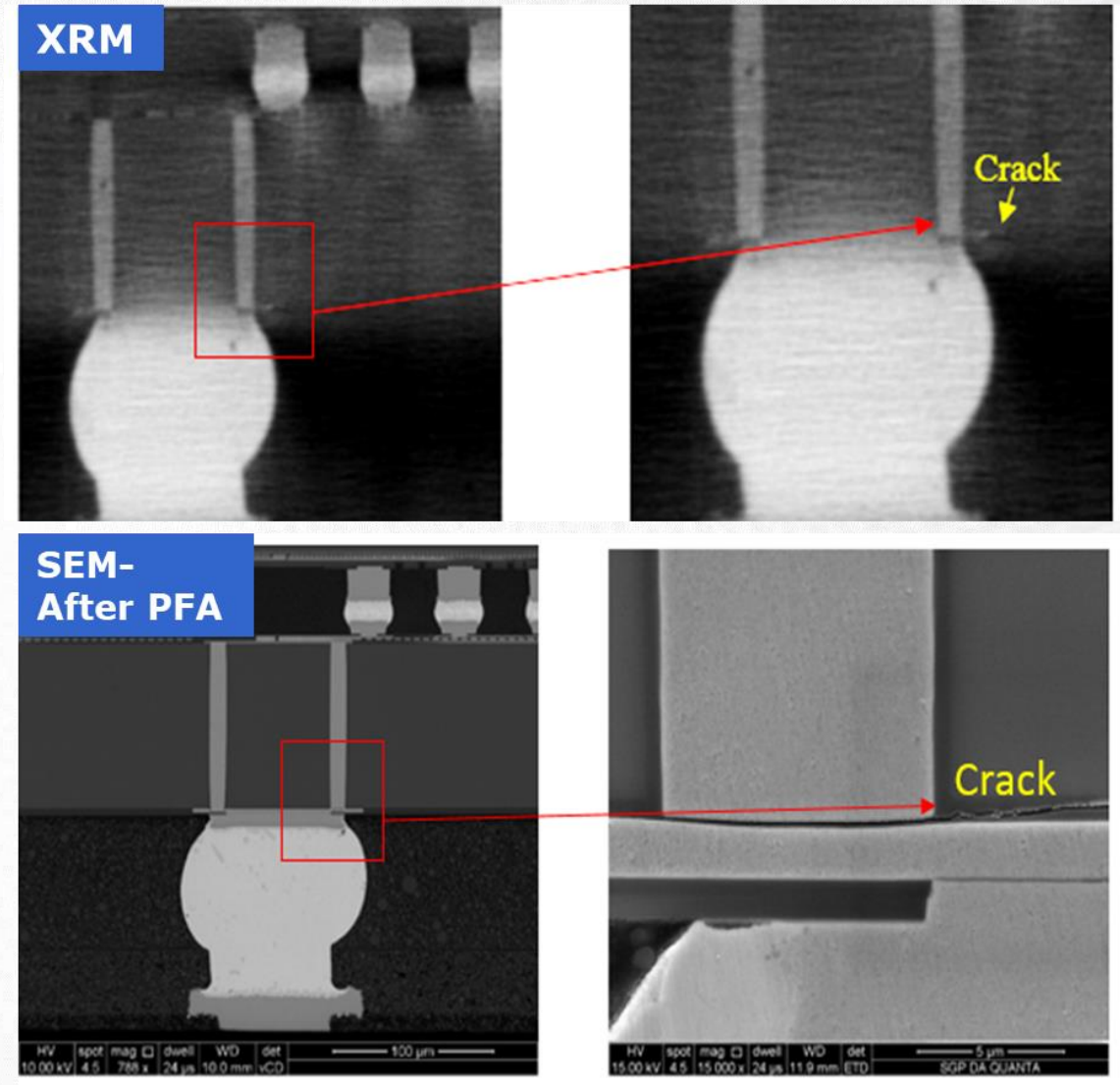
CASE STUDY 3 – OPEN FAILURE (CSAM/EOTPR/3D X-RAY)



- EOTPR found defect to be mid-way between the substrate termination and interposer termination putting it near the bottom of the TSV.

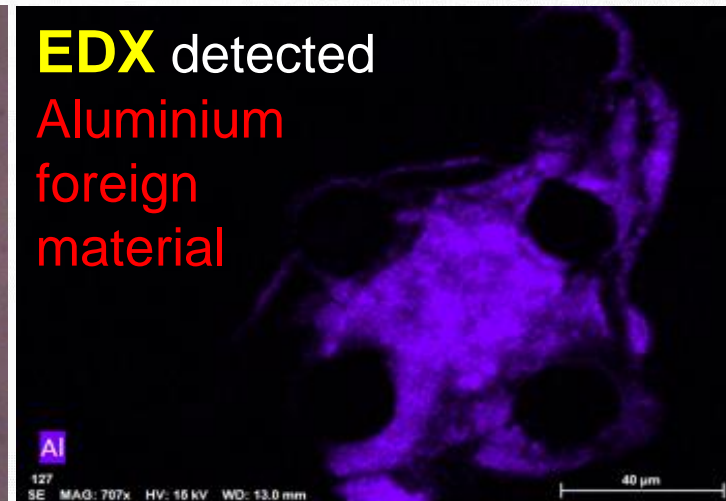
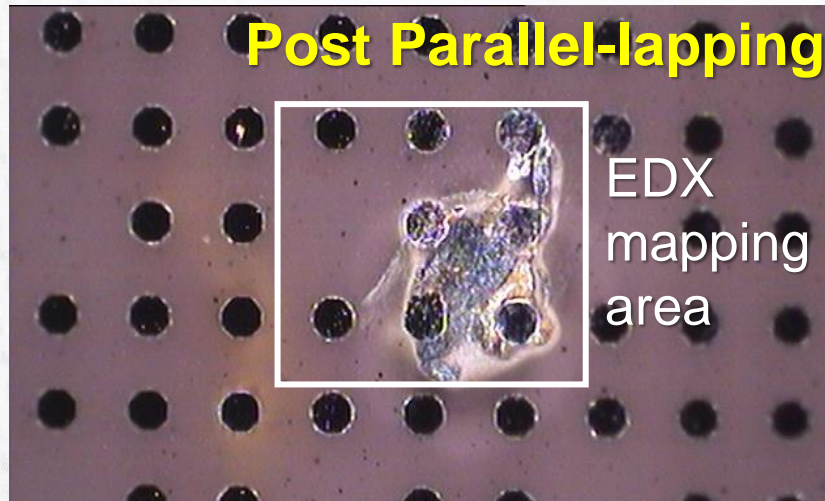
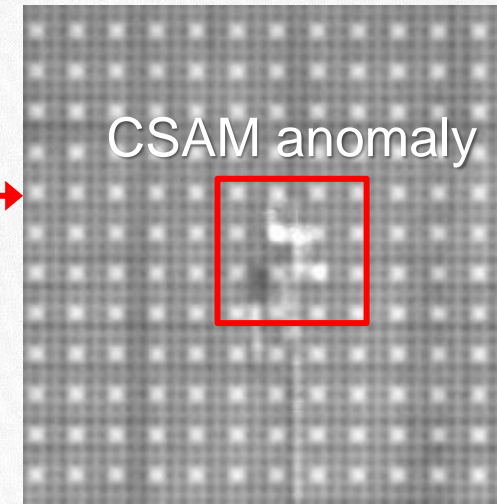
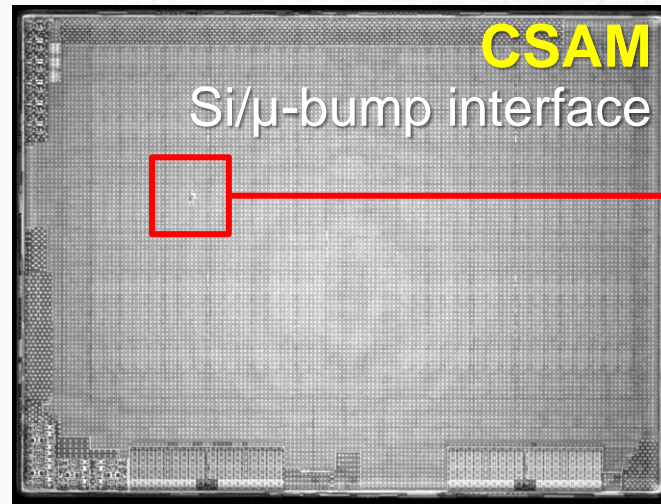
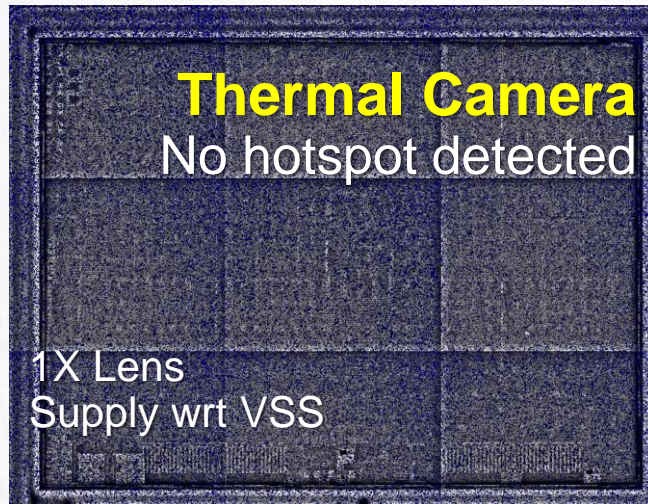
CASE STUDY 3 – OPEN FAILURE (CSAM/EOTPR/3D X-RAY)

- 3D X-ray Microscopy performed to verify NDT – crack was observed.
- XRM provides visual knowledge of the location to focus on and the nature of defect in order to carry out accurate PFA.



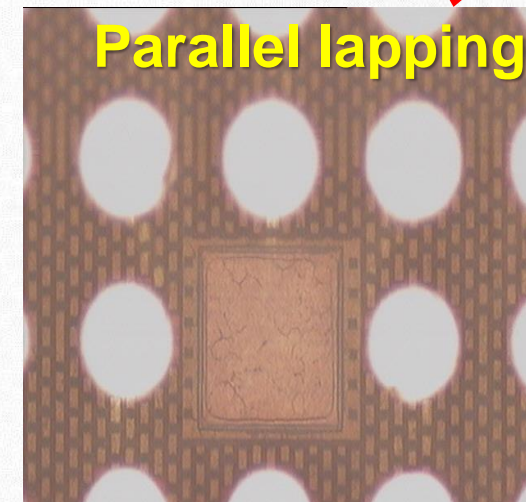
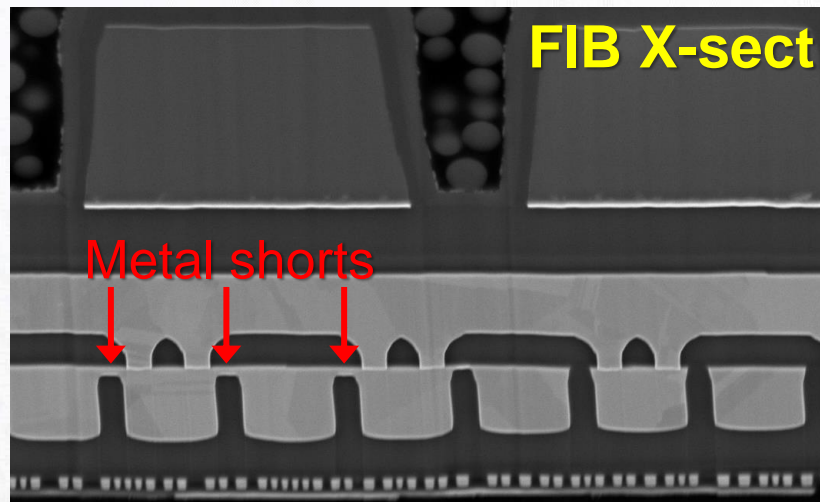
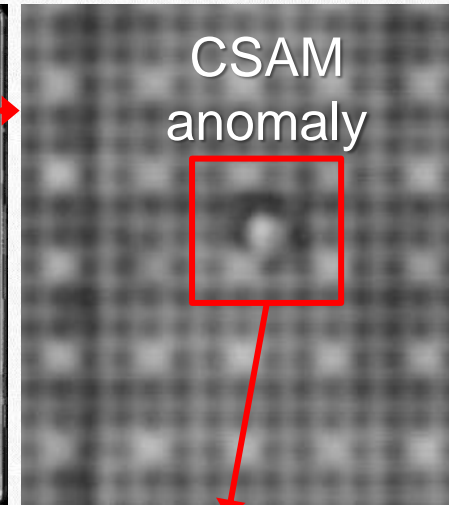
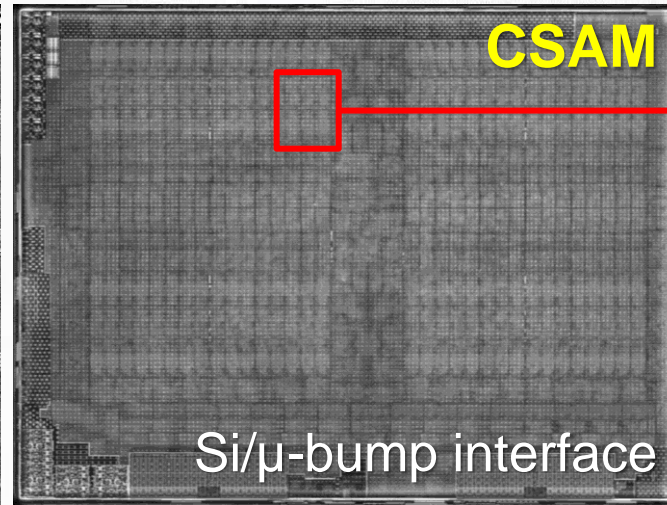
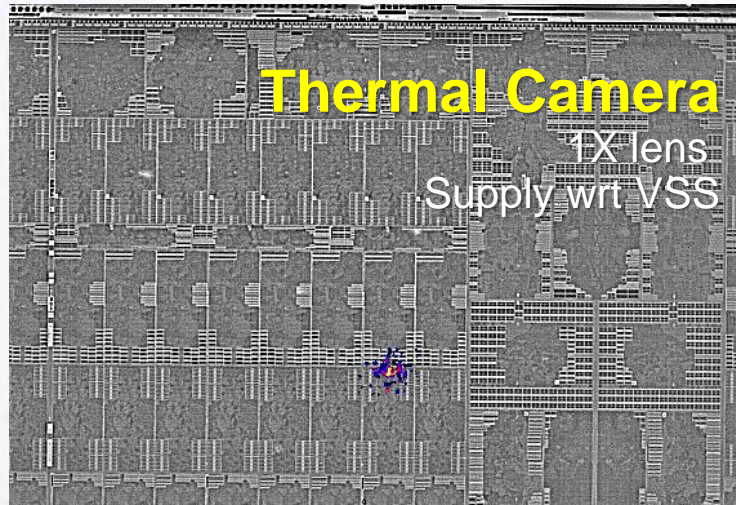
CASE STUDY 4 – POWER SUPPLY SHORT FAILURE (LIT/CSAM)

- Root cause: aluminium FM bridged μ -bumps (defect visible in CSAM).



CASE STUDY 5 – POWER SUPPLY SHORT FAILURE (LIT/CSAM)

- Root cause: metal shorts.



No visible defect in optical inspection

SUMMARY

- Failure analysis field continue to be very challenging with progress of packaging technology.
- Early involvement of FA in the technology/product cycle is KEY.
- Innovations in FA techniques and tools need to occur in tandem with packaging technology advances.

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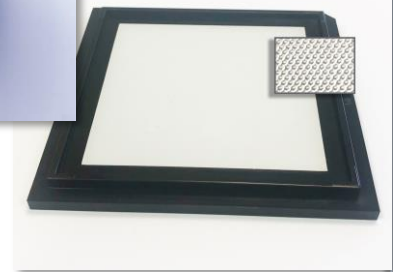
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