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Successful Multi-Die System Design Using Synopsys 3DIC and Ansys Multiphysics Analysis

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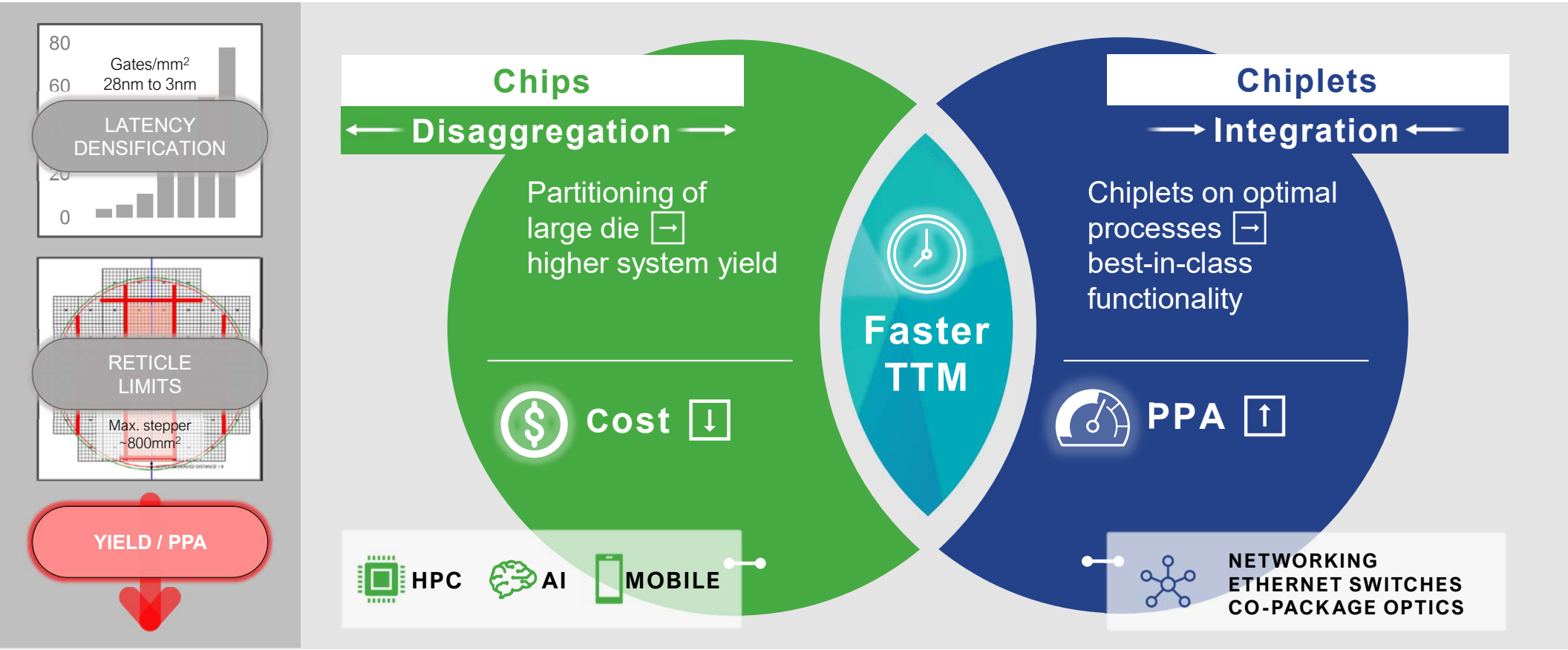
Market Drivers: The Demands for Data and Processing

Silicon Disruption from System-on-chip (SoC) to System-of-Chips…



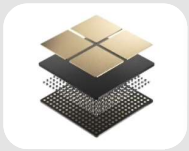
The Rise of Chiplet-Based Solutions

1980s — **Design with Schematics**
Sea of transistors/gates

1990s — **Design with HDL**
Sea of cells/blocks

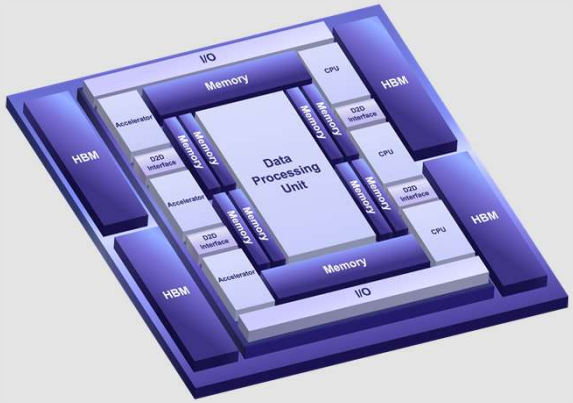
2000s — **Design with IPs**
Sea of functional units/IPs

>2020 — **Design with Chiplets**
Sea of chiplets/IP subsystems



Source: “1000x More Compute for AI by 2025”, Raja Koduri, Intel

System-of-Chiplets

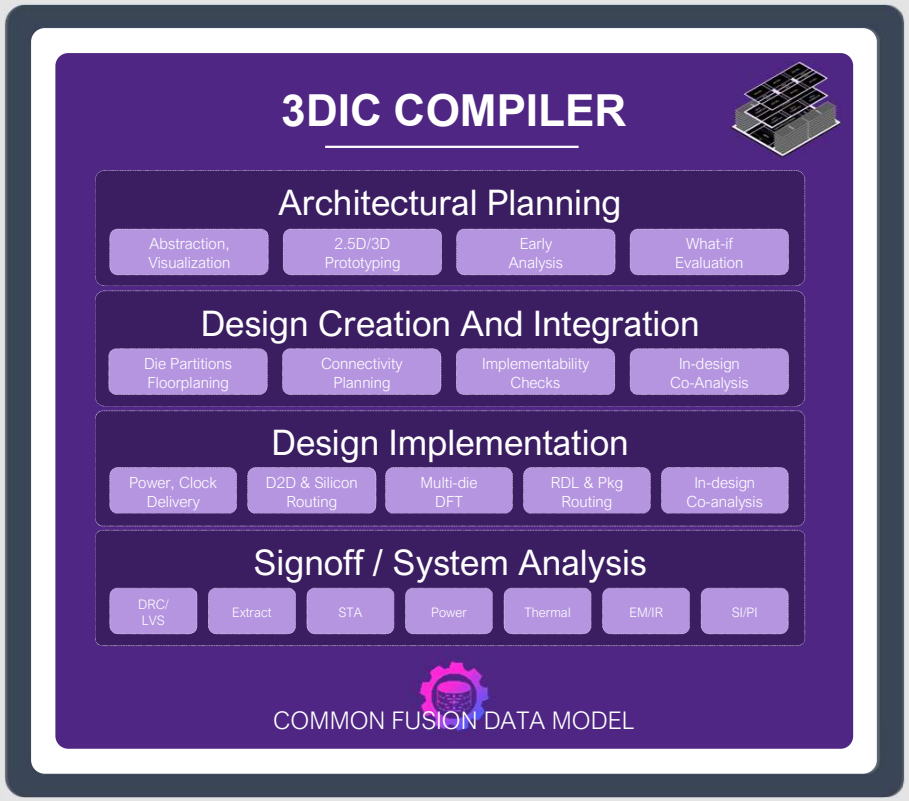


Benefits

- Better yield with smaller dies, exceeding reticle constraints
- Chiplets in its optimal technology, lower cost potential
- Reusability, targeting multiple markets
- Lower system power while increasing throughput

3DIC Compiler: The Unified Exploration-to-Signoff Platform

Extensible solution to accelerate 2.5D Chiplets, 3D Stack and Advanced Packages



Highly Integrated, Scalable Platform

Heterogeneous system-of-chips design and integration over 100s of Billions of transistors

Flexible, Efficient Workflow Environment

Fast exploration and pathfinding to accelerate 3D design creation and D2D planning

Comprehensive Design and Closure

Full breadth of high-throughput engines – D2D/Pkg auto-routing, native DRC, DFT, ECO and more

Trusted, Golden Signoff Analysis

Integrated industry standard technologies (**Synopsys** + **Ansys**) for convergence to optimal PPA/mm^3
(incl. Thermal, EM/IR, SI/PI, STA)

3D Solutions Certified by TSMC for 3DFabric™

SoIC™, CoWoS™, and InFO™

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Synopsys Expands Strategic Technology Collaboration with TSMC to Extend 3D-System Integration Solutions for Next-Generation High-Performance Computing Designs

Synopsys' 3DIC Compiler Delivers Seamless Access to TSMC 3DFabric Technologies

MOUNTAIN VIEW, Calif., Oct. 20, 2021 /PRNewswire/ --

Highlights of this Announcement:

- Expanded strategic collaboration delivers comprehensive 3D-system integration capabilities, enabling the aggregation of hundreds of billions of transistors in a single package
- Synopsys 3DIC Compiler, the unified, multi-die implementation platform, seamlessly integrates TSMC -3DFabric technologies-based design methodologies, to offer a complete exploration-to-signoff design platform
- This joint collaboration combines TSMC's technology advancements with the converged architecture, advanced in-design analysis framework and signoff tools of 3DIC Compiler to deliver the required

Ansys Multiphysics Solutions Certified by TSMC for High-Speed Next-Generation 3D-IC Packaging Technologies

TSMC leverages Ansys' multiphysics platform to analyze power, thermal and signal integrity for its CoWoS® and InFO technologies

Key Highlights

- Ansys achieved certification of its advanced semiconductor design solution for TSMC's high-speed CoWoS® (Chip-on-Wafer-on-Substrate) and InFO (Integrated Fan-Out) 2.5D and 3D advanced packaging technologies
- Ansys' comprehensive suite of power, thermal and signal integrity analysis engines simulate, calculate and alleviate reliability issues, enabling optimal electrical performance

3DIC Compiler Platform Technology Highlights

Fast, Analysis-Driven "What-if" Exploration | Design Realization and Validation | Pathfinding-to-Closure Cockpit

System Creation

Multi-Die Multi-Tech Prototyping / Floor-planning / Integration

Die partitioning

What-if Analysis

Auto Bump/TSV Management

Design Implementation

Fast, Auto / Assisted Routing

Full-Stack Bumps/TSV Creation

Multi-die DRC and LVS

Multi-Die Test Access and DFT Support

System Analysis

Complete Analysis Solution

- Full-spectrum, multi-physics analysis – electrical, thermal, signal and power integrity

Early-Design Analysis Support

- Fast, In-design-level accuracy

3D Data Management Environment

COMMON FUSION 3D DESIGN DATA MODEL

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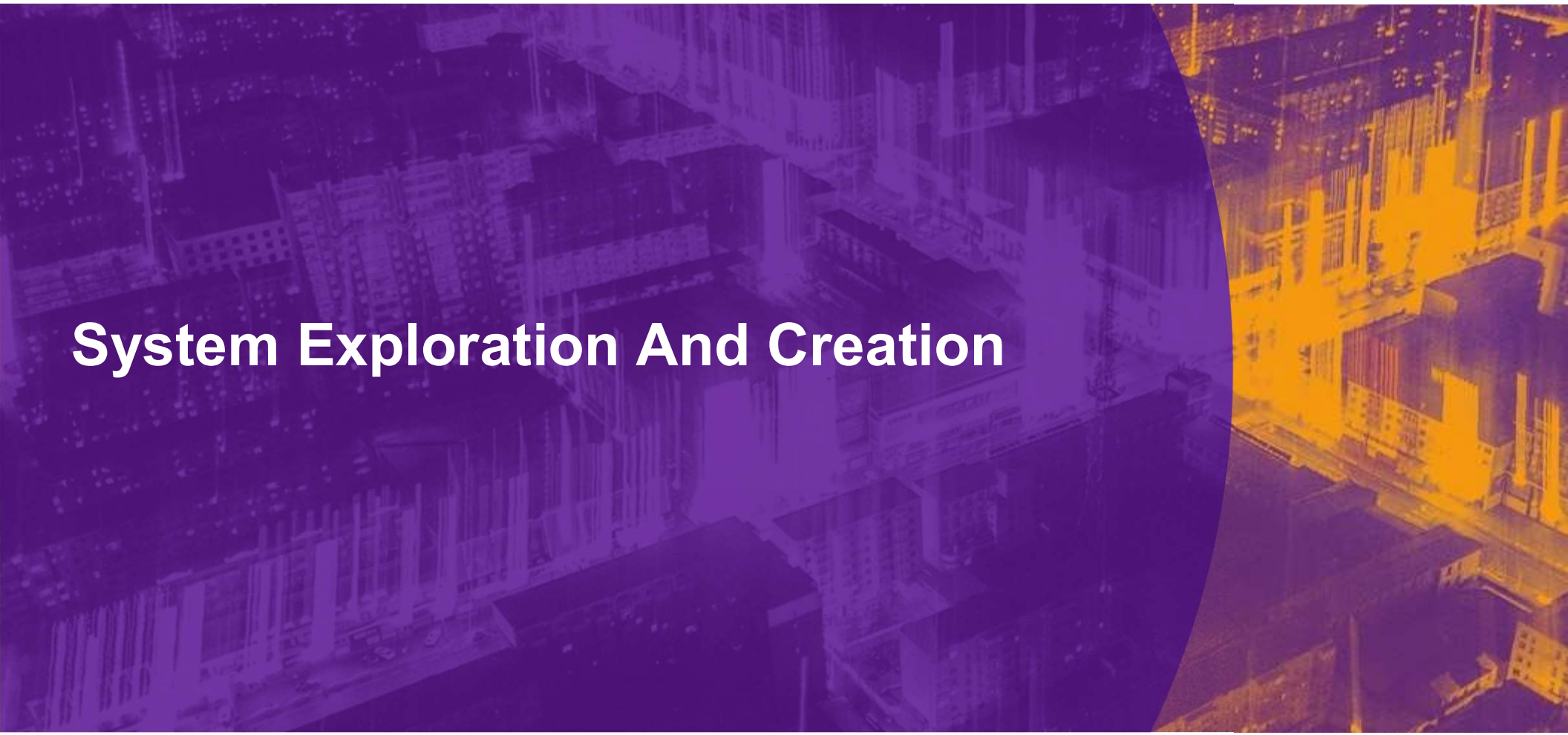


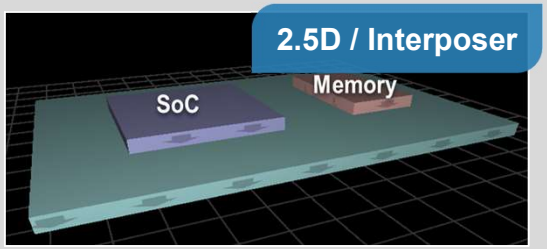
System Exploration And Creation

Iteratively Explore, Create, Optimize in One Place

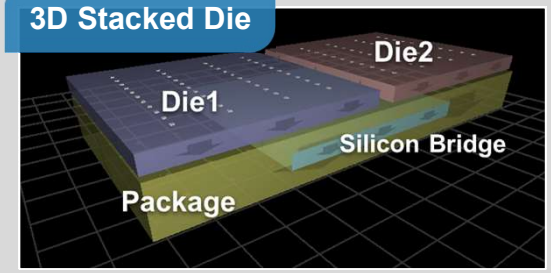
Intuitive UI for Ease-of-Use and Productivity for 2.5D/3D Design

Architecture

2.5D / Interposer

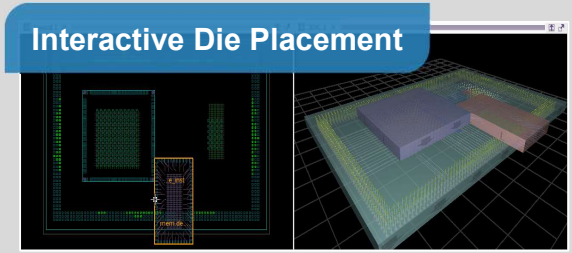


3D Stacked Die

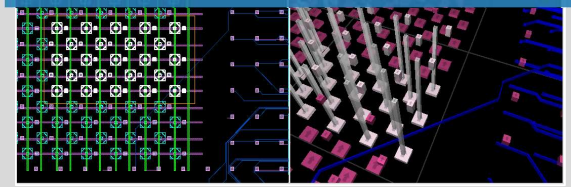


Creation

Interactive Die Placement

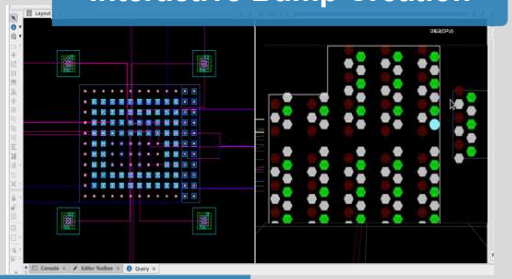


C4 and TSV Selection for Modification

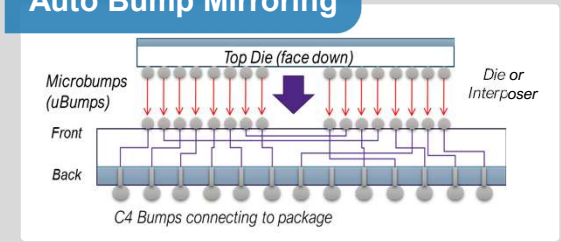


Analysis Driven Optimization

Interactive Bump Creation

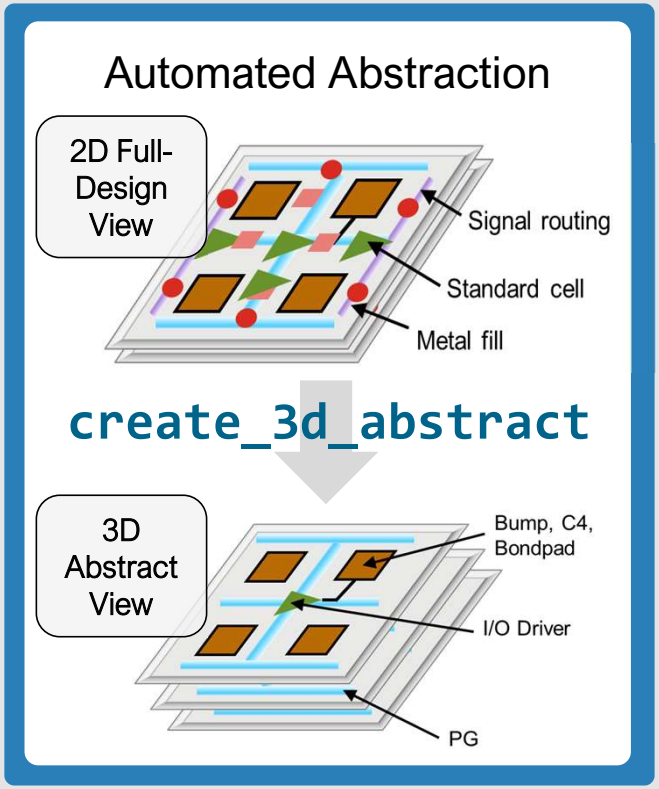


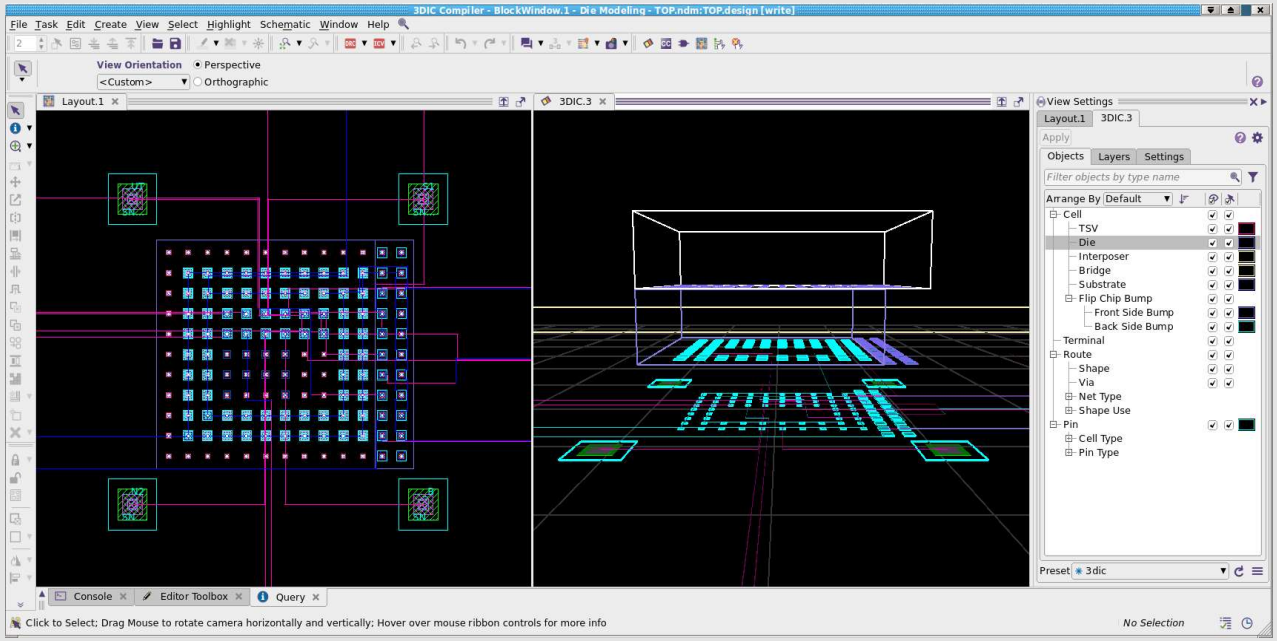
Auto Bump Mirroring



Automated Abstraction Enables Fast Exploration

Single data model delivers fast and seamless data and context management



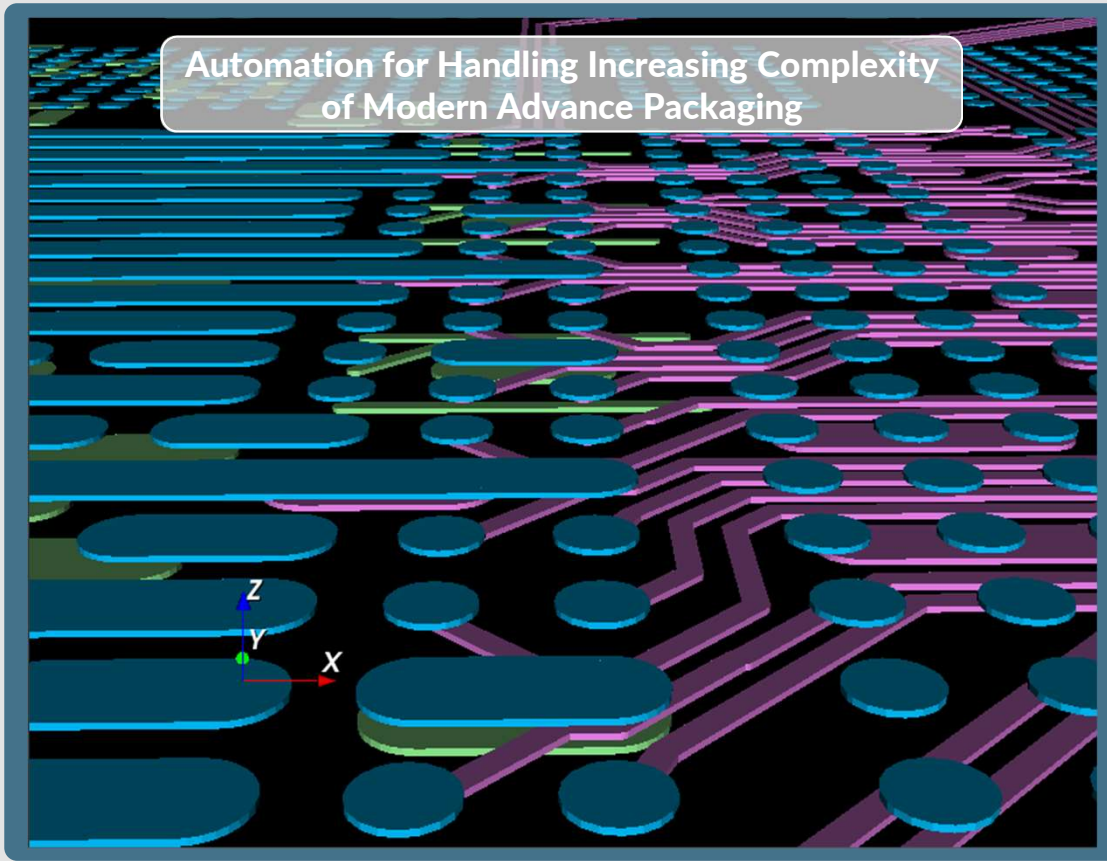


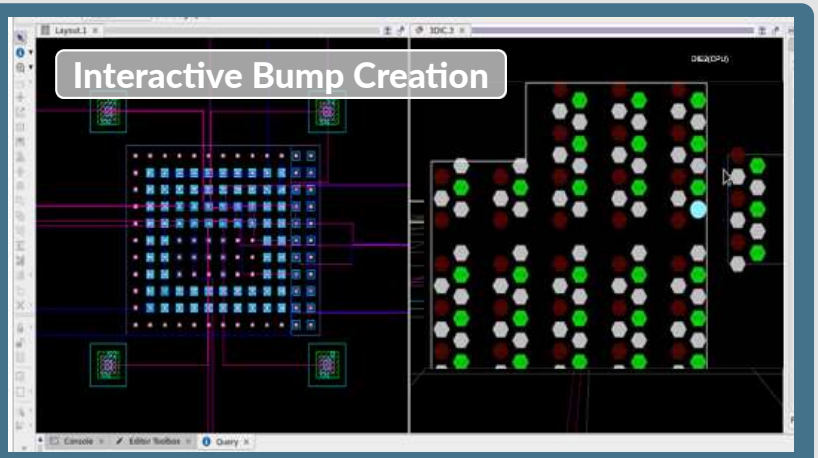
Work with the appropriate level of design details

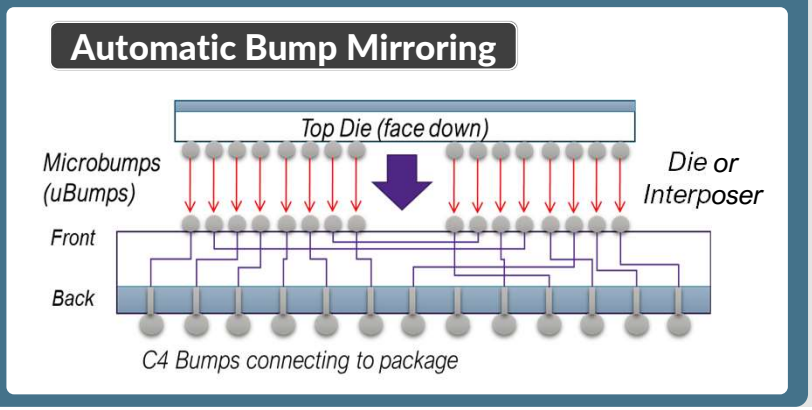
merge_abstract to go back to full-design view

Meeting The Full-stack Scalability Challenge

3DIC Compiler Bump Management



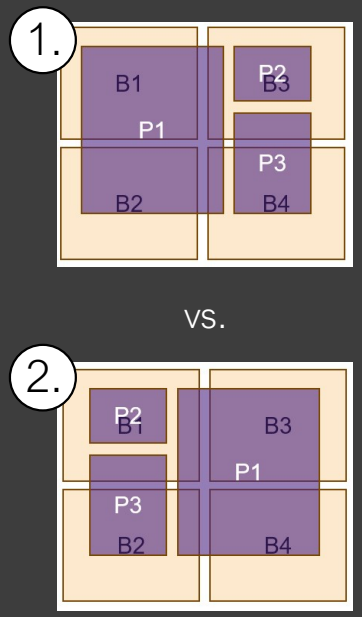




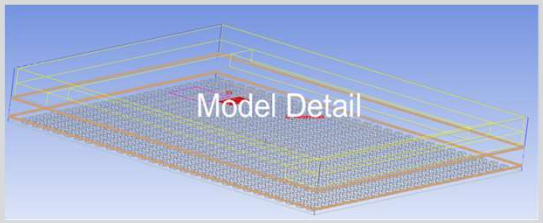
Exploring Alternatives For Power Delivery

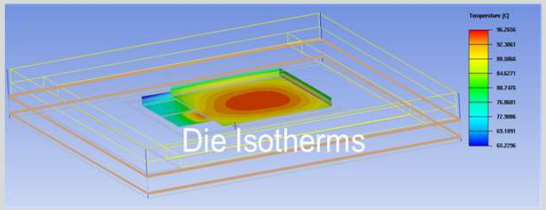
Thermal Analysis Example: Floorplanning Trade-offs

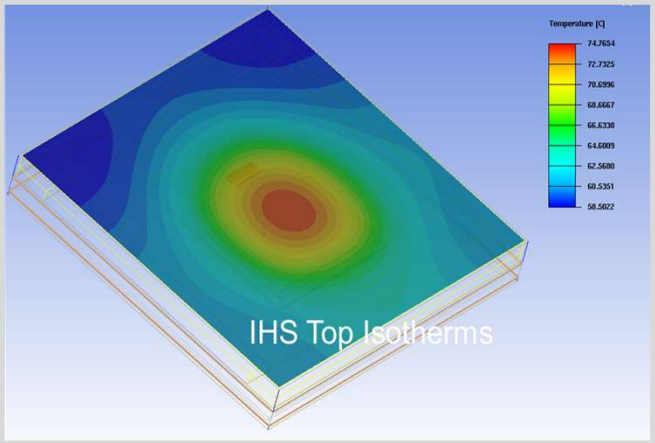
Exploring Floorplan Efficacy



Multi-Die-Package Thermal Maps





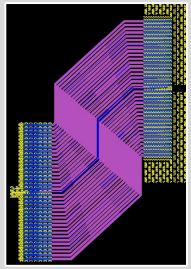


Theta-JC = (96.27-74.77)/36 = 0.597 °C/W


Design Implementation

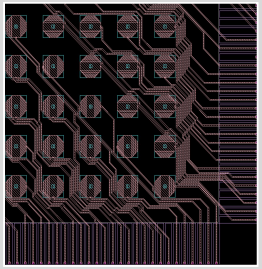
Fast, Automated Routing Technologies for All Architectures

Auto-HBM Routing



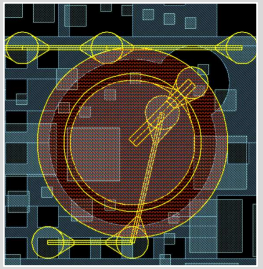
JEDEC HBM bus routing support with optional shielding and differential pairs

RDL Routing



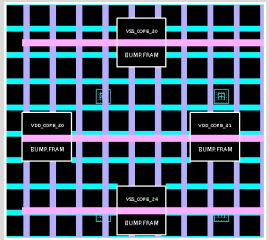
Net-based 45-degree RDL (Redistribution Layer) Routing

Custom Routing



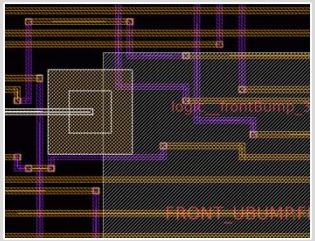
Visually-assisted automated custom layout editing for productivity

PG Routing



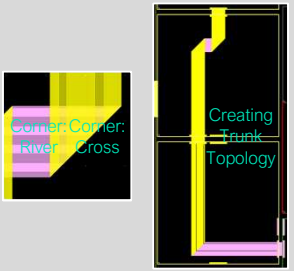
PG grids, rails and straps synthesis with specified pitch

Signal Routing



Net-based 90-degree full-chip signal routing with high-perf DRC, optimization & congestion management

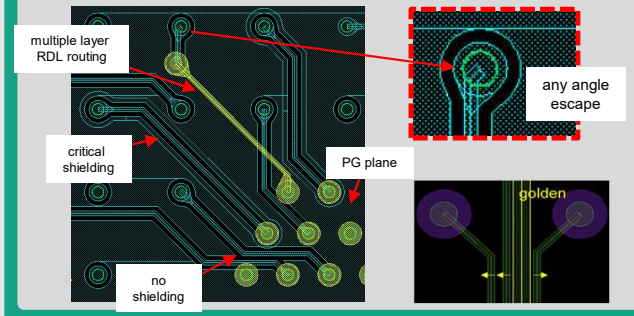
Bus/Trunk Routing



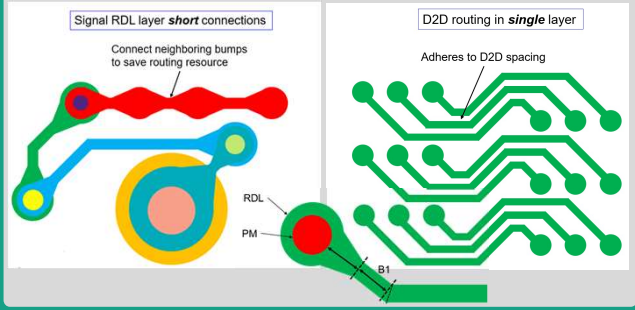
Easy-to-use and fast innovative bus routing

Unique Automated Solution for Advanced Packaging

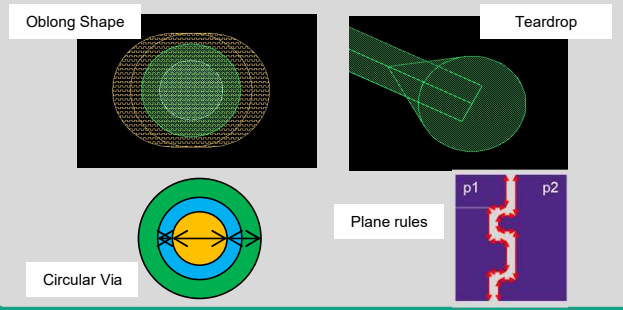
RDL And Push-Aside Routing



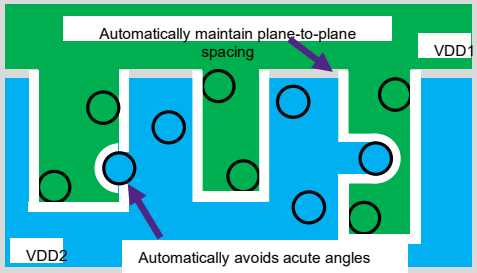
RDL Substrate Auto-Routing



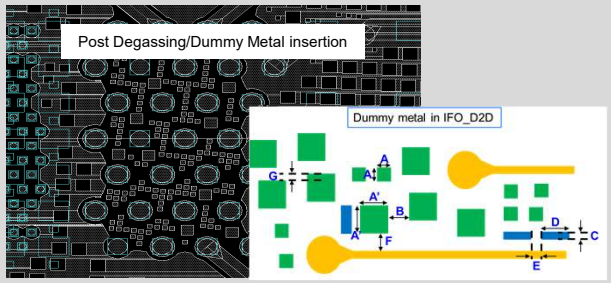
Specific Shapes



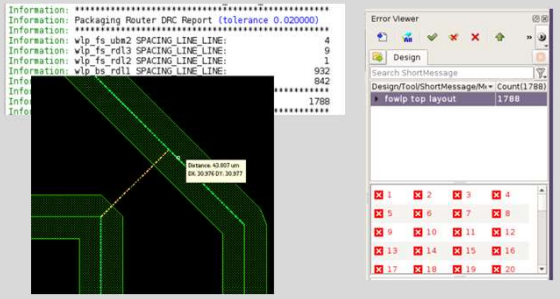
DRC-Aware P/G Realization



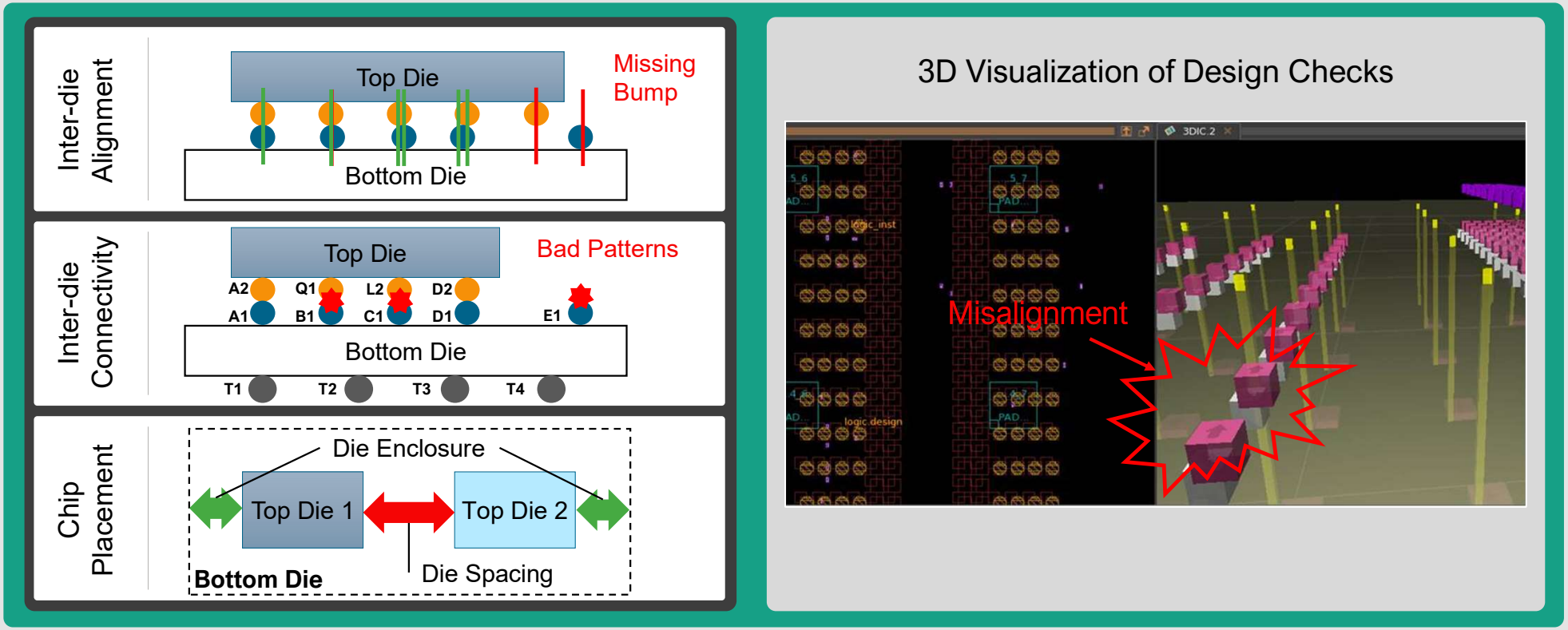
Degassing / Metal fill



Package DRC

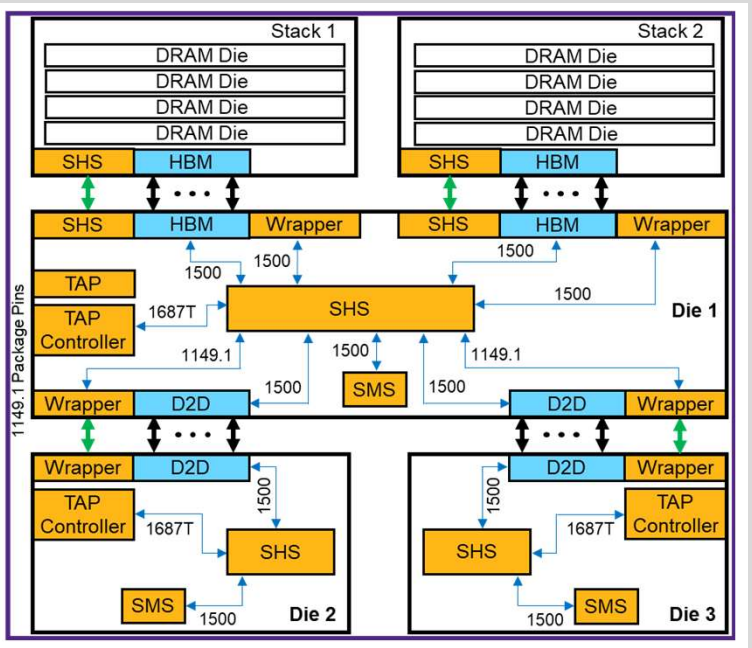


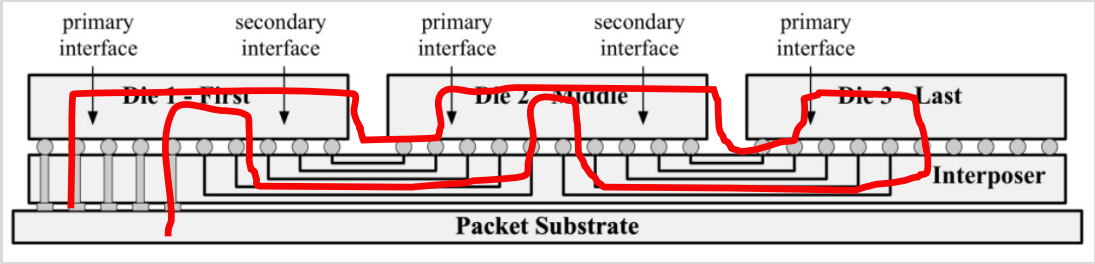
Native 3D Multi-Die And Package DRC

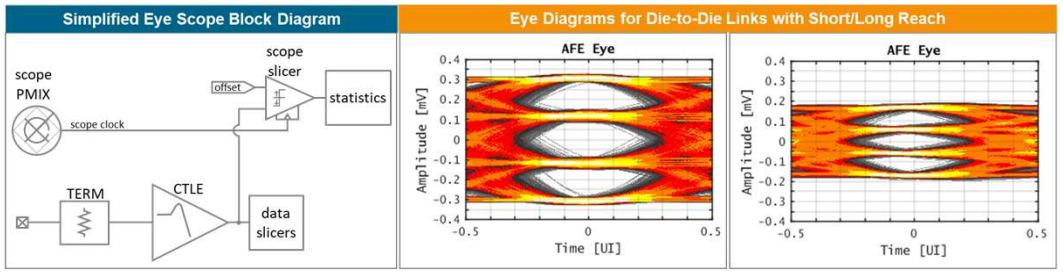


Integrated Test Access and Connectivity Validation

IEEE1838 Test Access Architecture for 3DIC







Internal Eye Scope Enables Validation of Die-to-Die Link Quality

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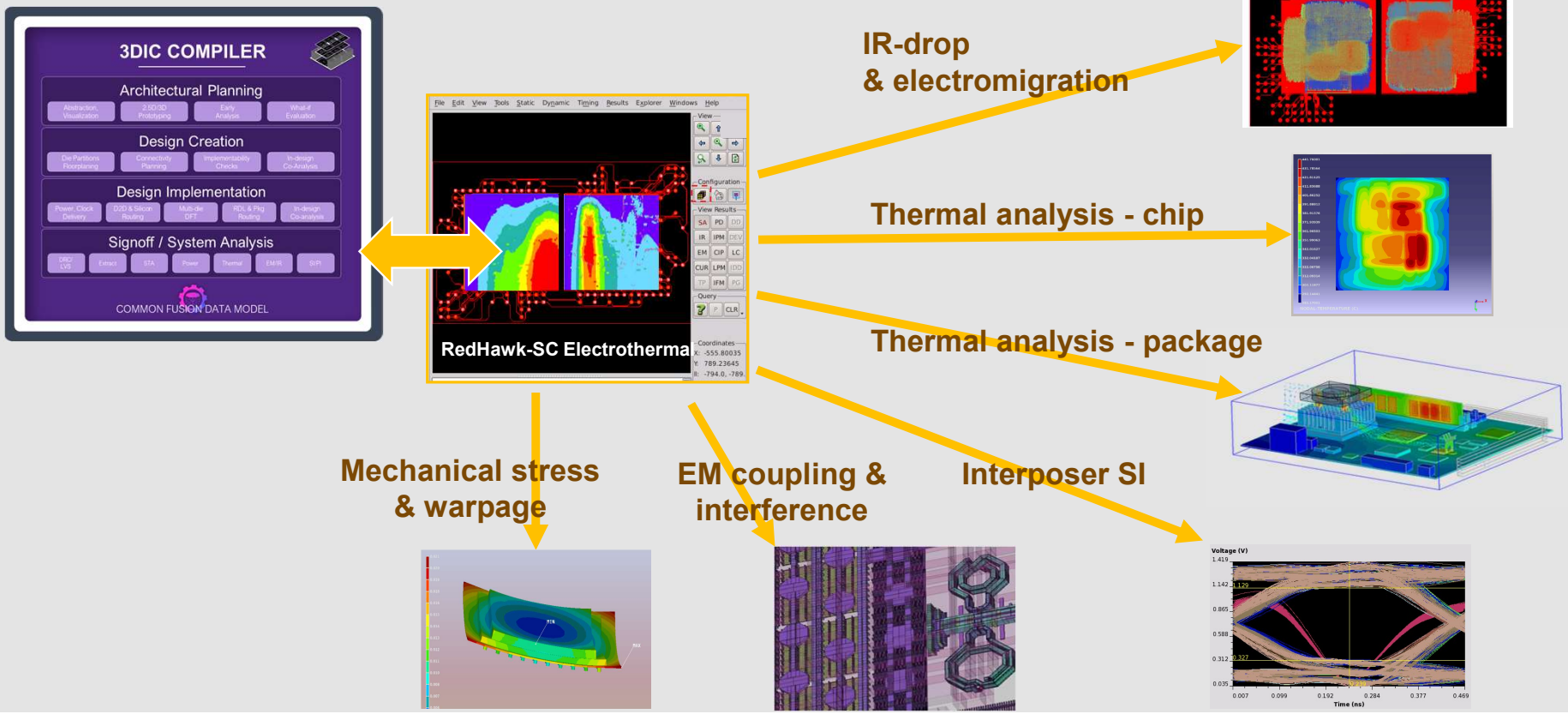
Multiphysics System Analysis

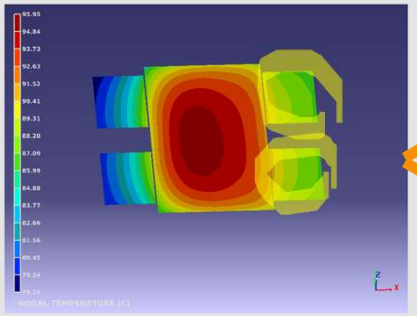
Integrated Chip-Package Multiphysics Co-simulation



RedHawk-SC Electrothermal Thermal Analysis

Full Stack 3DIC Detailed Temperature Profile Maps

3D Package
1 SoC + 4 HBM

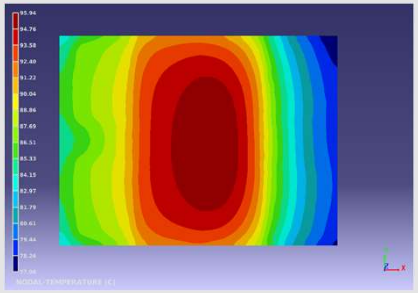


Interposer: >750mm^2

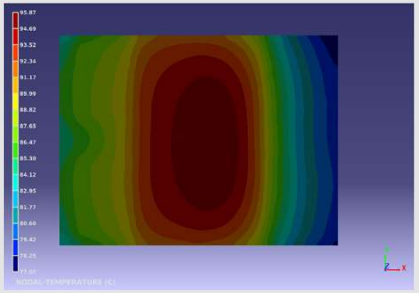
Heat Sink: Yes

Run Time: 1h:20m
(incl. Icepak)

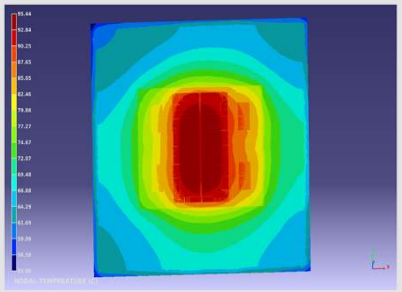
Interposer Microbump Layer



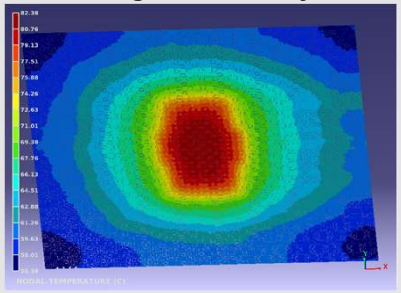
Interposer Substrate Layer



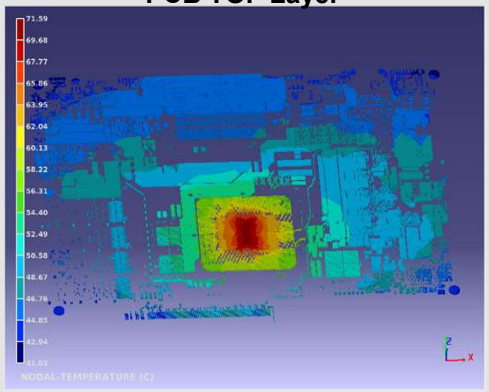
Package TOP Layer



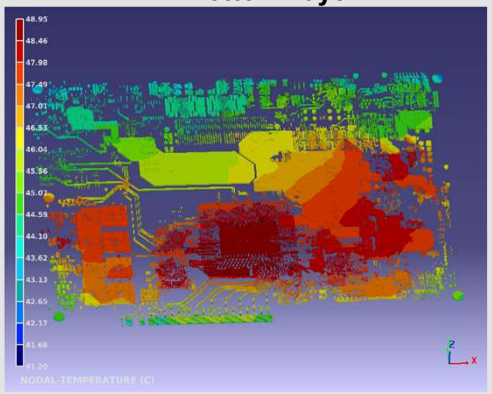
Package Bottom Layer



PCB TOP Layer

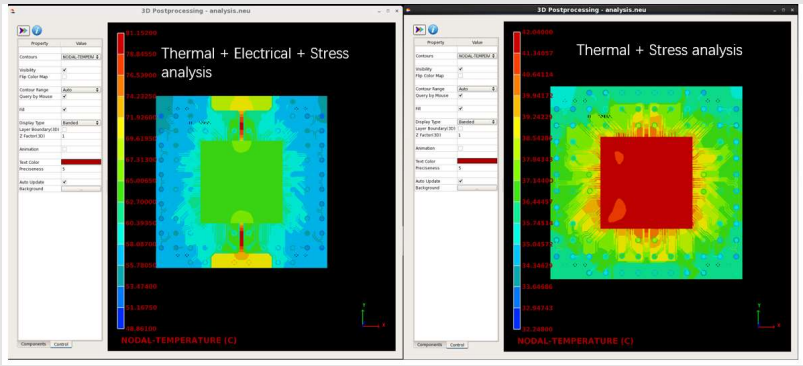


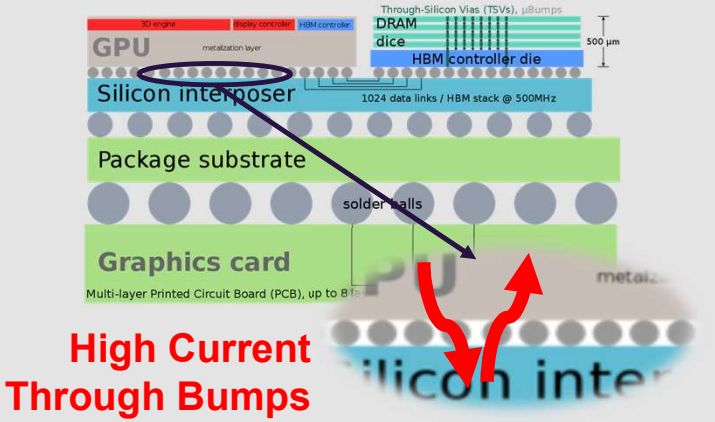
PCB Bottom Layer

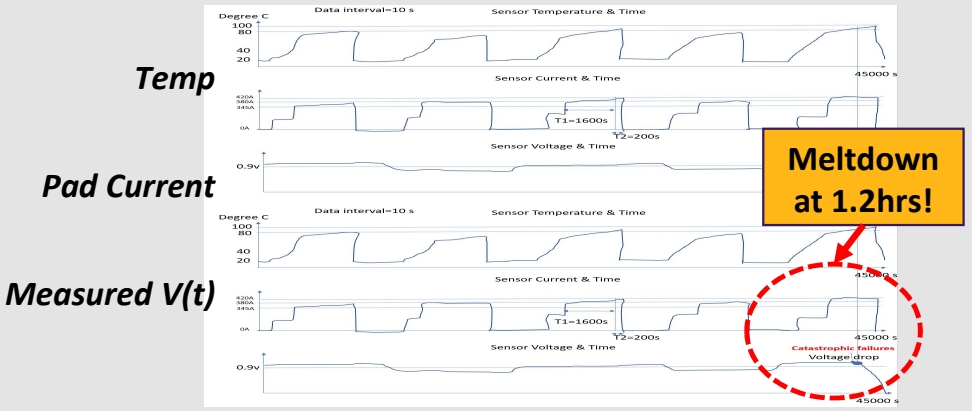


Case Study:
RedHawk-SC Electrothermal Catches Meltdown Issue

- High-power HPC design
- Electro-thermal issue on micro-bumps.
- RedHawk-SC Electrothermal catches this by simulating Joule heating effects and applying pad currents from RedHawk-SC

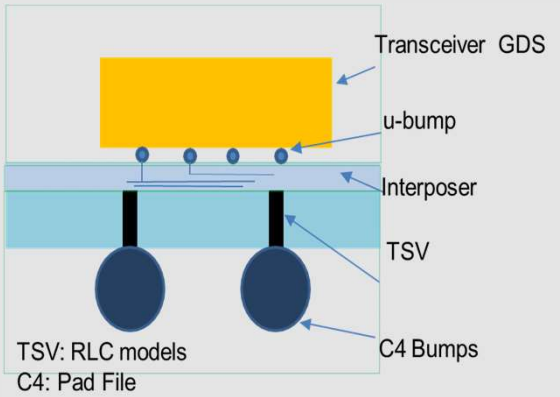






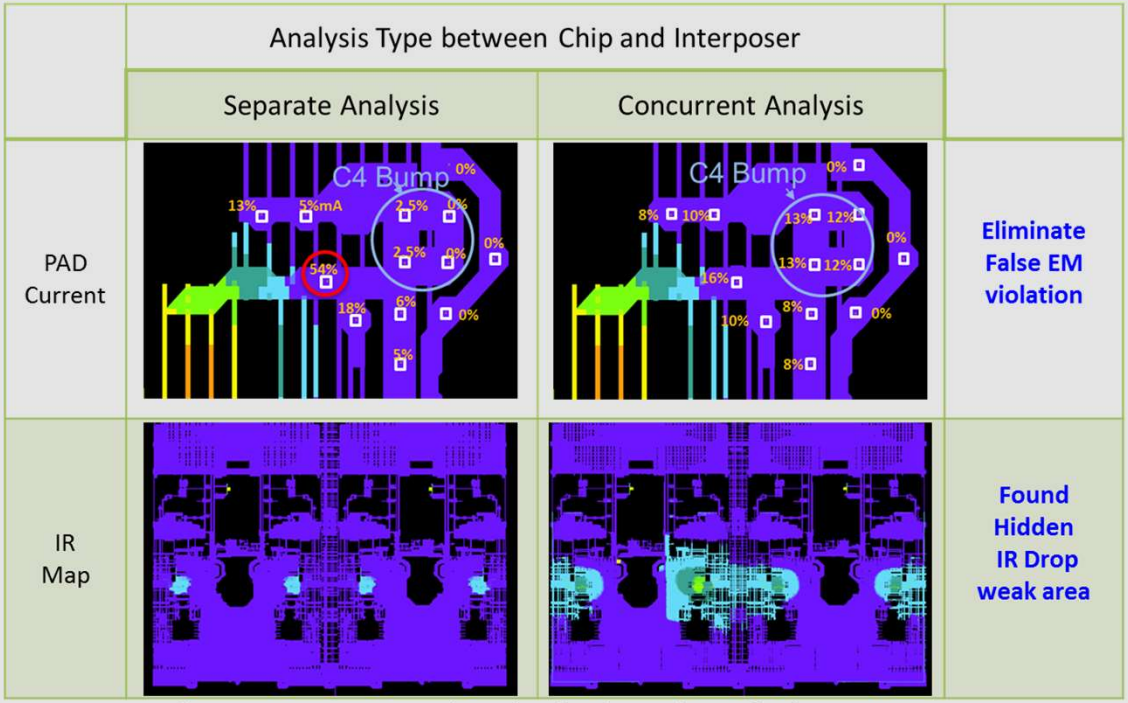
3DIC Chip Level Concurrent EMIR Analysis

Prevent overdesign/underdesign by concurrently analyzing the chip and interposer for accurate current distribution



Design Specification:

. High-speed Transceivers in 16nm FinFET FPGA
. 120x32.75Gb/s SerDes
. 2.58M Programmable Logic Cells w/ DSPs
. 3 fabric slices on CoWoS, 20B Transistors



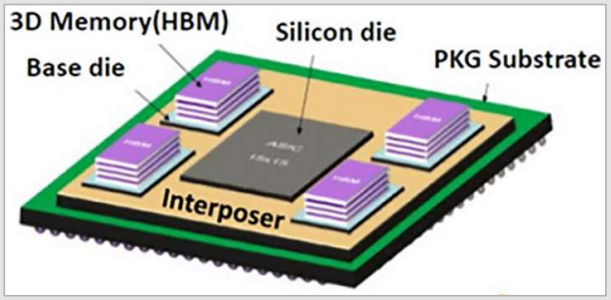
Ling Yang, "Concurrent 3DIC Power Supply Analysis for Xilinx Serdes Interface", DesignCon 2018

SYNOPSYS® // Ansys

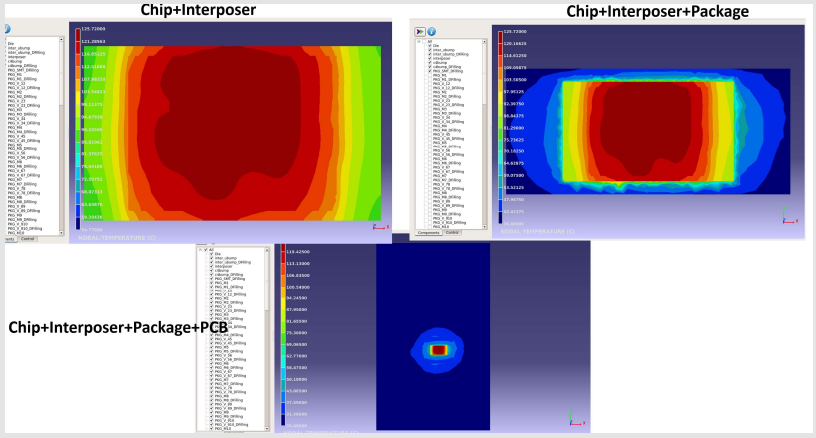
Detailed Temperature Profiles for CoWoS® Down to Each mBump

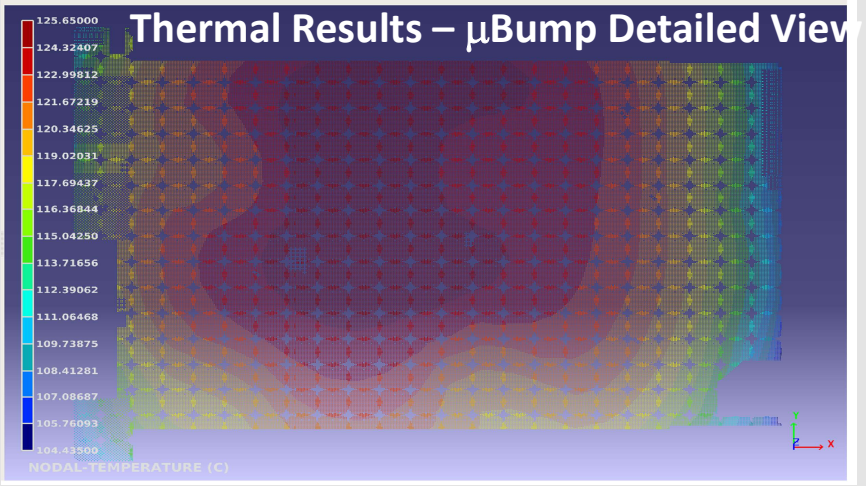
AI/Networking Chip Company

Silicon Die + Interposer + 4 HBMs
Connector Bumps: 100k+
3D-IC Package: 10+ metal layer **CoWoS®**
Board: 20 metal layer, ~70,000mm^2
Peak Memory Usage: 473GB
Full Thermal Analysis Run Time: ~40Hrs



Thermal Results Overview





Summary

- **3DIC Compiler provides industry's only unified platform** for exploration-to-design-and-signoff of 2.5D/3D multi-die/chiplets advanced package systems

- **Integration with Ansys' multi-physics suite of products** delivers golden analysis for entire system – includes EM/IR, thermal, electromagnetic, mechanical

- **Co-design and analysis accelerates** exploration, planning and implementation to achieve fast **design convergence and optimal PPA/mm^3**

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THANK YOU

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