Road to Chiplets: Design Integration

May 10-12, 2022

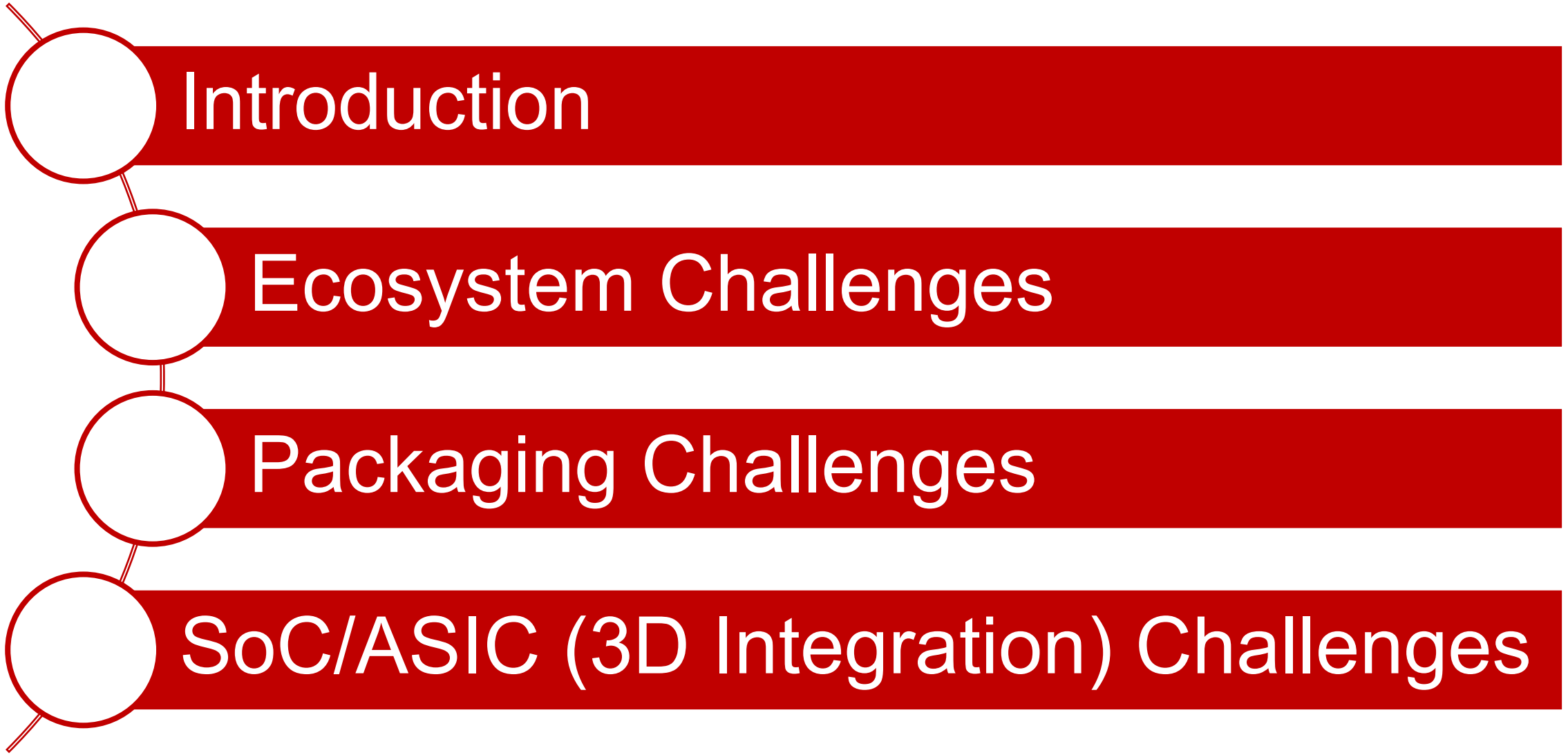
MEPTEC
THE NEXT GENERATION

www.meptec.org

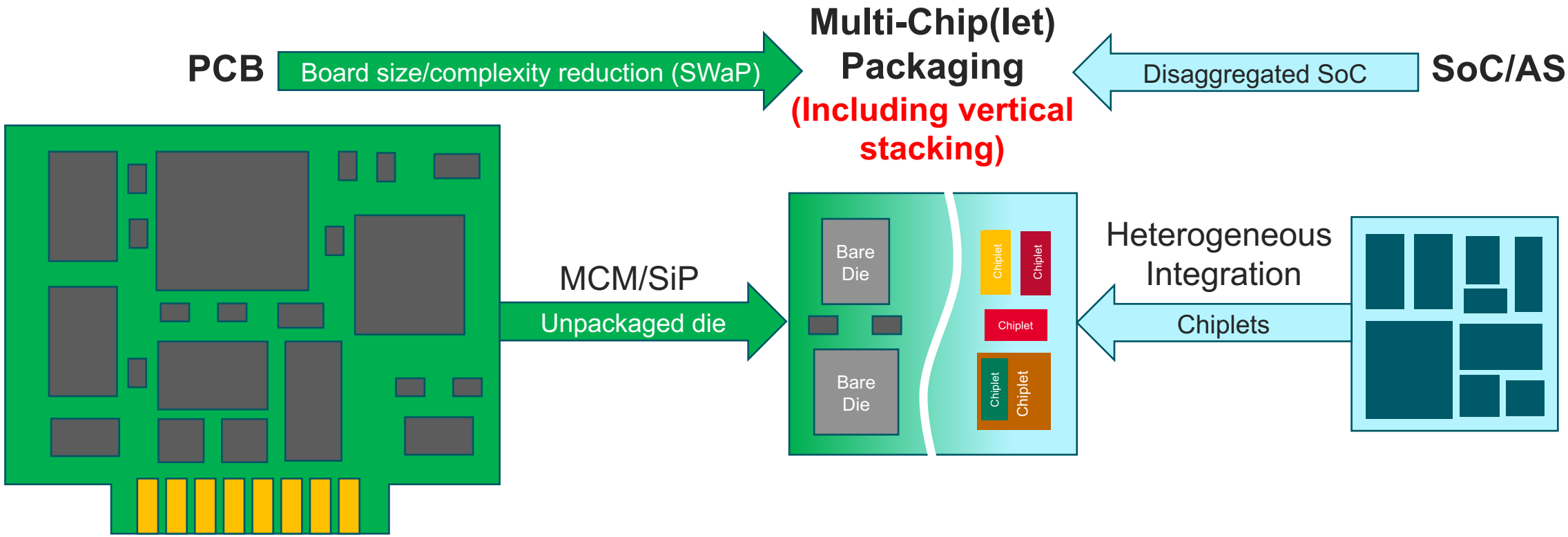
3D-IC (3DHI) Design Challenges

John Park (jpark@cadence.com)
Product Management Group Director

cadence®



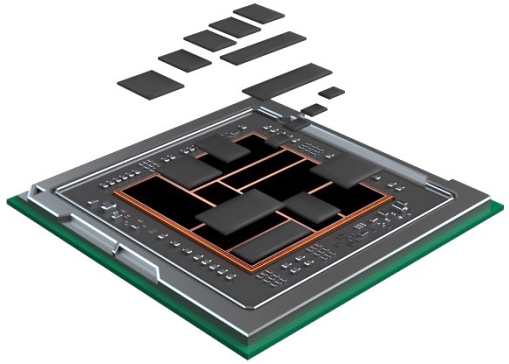
SiP/MCM vs. Chiplet-Based 3DHI Architectures



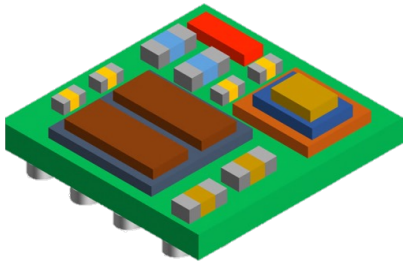
PCB to MCM/SiP Benefits
Smaller footprint
PCB simplification
Higher bandwidth
Lower power

SoC to HI Benefits
Reduced NRE costs
Shorter time to market
Larger than reticle size designs
More flexible IP use-model

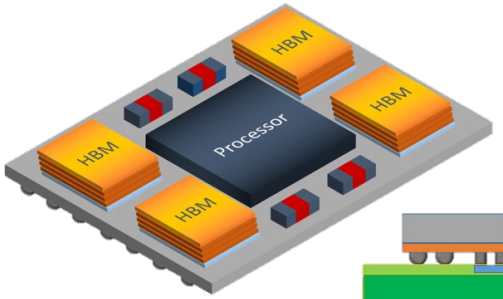
Heterogenous Integration Leverages Multiple Packaging Technologies



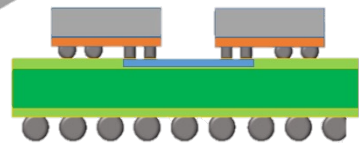
Heterogeneous Integration



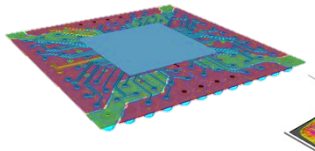
System in Package (SiP/MCM)



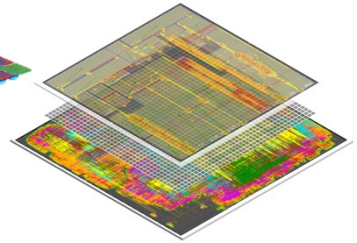
2.5D-IC (Silicon/RDL Interposer)



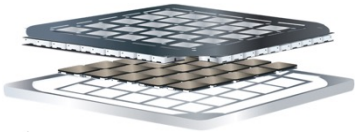
Interconnect Bridges



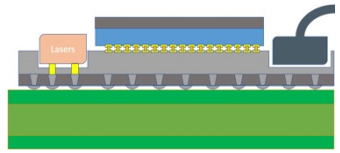
FOWLP (Ultra-High-Density RDL)



Bumpless 3D Integration



3D System-on-a-Wafer

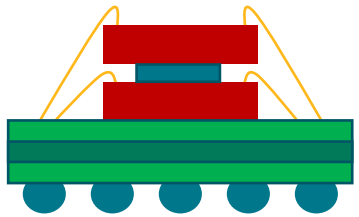


Co-Packaged Optics

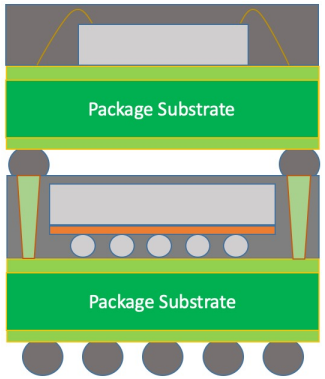
1990 2010 2012 2015 2018 2020 2022

3D Packaging (Back-End 3D) vs. 3D Integration (Front-End 3D)

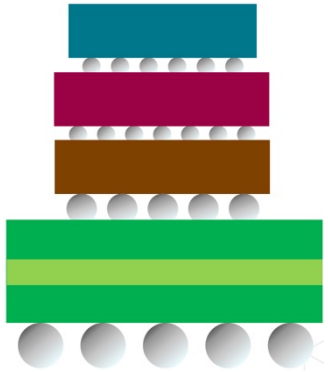
3D Packaging



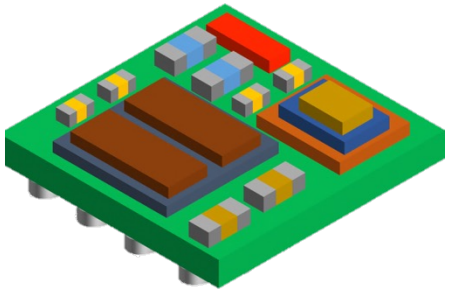
Wire-bonded BGA



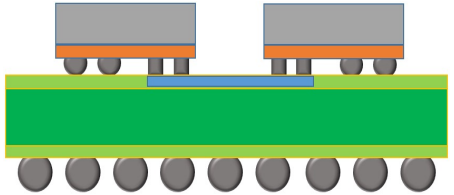
Package on package (PoP)



Micro-bump stacking

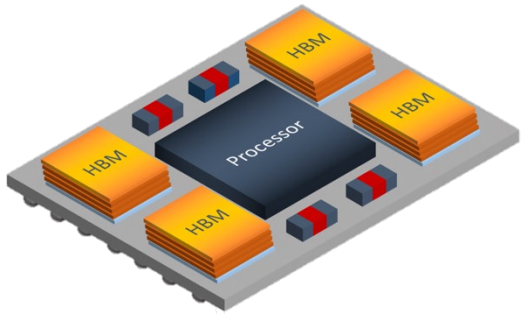


SiP/MCM

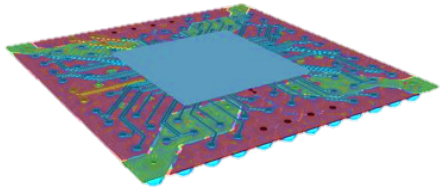


Interconnect bridges

Hybrid

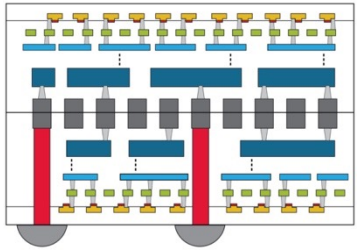


Silicon (TSV) interposer

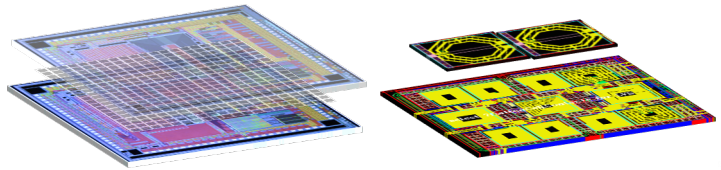


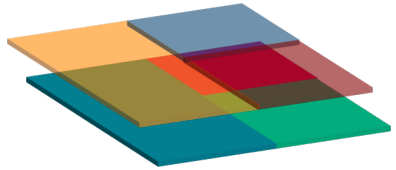
FOWLP
(Ultra-high-density RDL)

3D Integration



Solder-bump-free stacking
Cu-to-Cu bonding, Direct bonding
Hybrid bonding





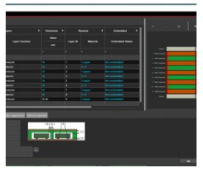
Core Macro and circuit stacking

3DHI Ecosystem Challenges

Assembly Design Kits (ADK)

- PDK equivalent for the entire multi-chiplet assembly
- Historically, OSATs have not provided sufficient data to package designers
  - OSATs have large design centers to off-set this limited formal sharing of design requirements
- Foundries are helping to drive the concept of a PDK into the packaging world

TechFiles

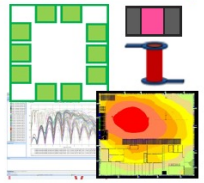


Layer stack-up
- Material
- Properties
- Thickness

Physical/Electrical layout constraints
- Line and space
- Differential signaling

Customized in-design DRCs

Design Libraries



Footprints
- Discrete
- BGA/LGA
- Via structures
- 3D Mechanical

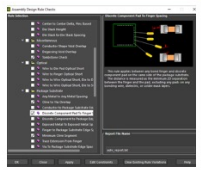
Bond-Wire profiles

Parametrized RF structures

Thermal models

Power models

Assembly Rules



Device placement constraints based on assembly pick & place equipment
- Die to die spacing
- Device to device
- Device to obstacle

Compliance Kits

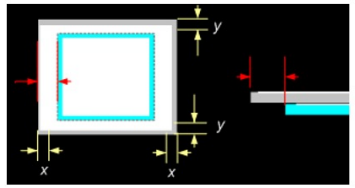
Electrical spec validation of chip(let)-to-chip(let) interfaces
- Interconnect library
- IO libraries
- Eye masks
- Jitter tolerance
- Insertion loss
- Return loss
- Eye mask

Manufacturing Rules

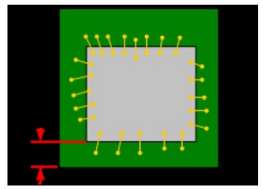
Board/substrate manufacturing process
- Substrate checks
- Soldermask checks
- Soldering issues
- Silkscreen checks

Rule Decks

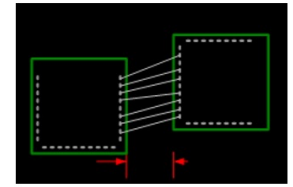
Foundry/ semiconductor manufacturing process
- DRC
- LVS
- Metal fill



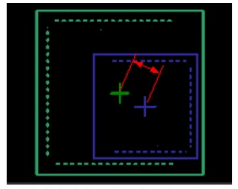
Die/Chiplet Overhang



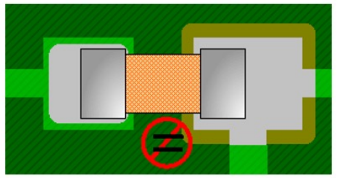
Die/Chiplet Spacing to Substrate Edge



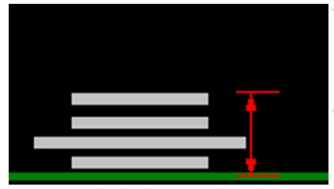
Die/Chiplet to Die/Chiplet Spacing



Die/Chiplet Center to Center Offset



Tombstone Effect (% size diff)

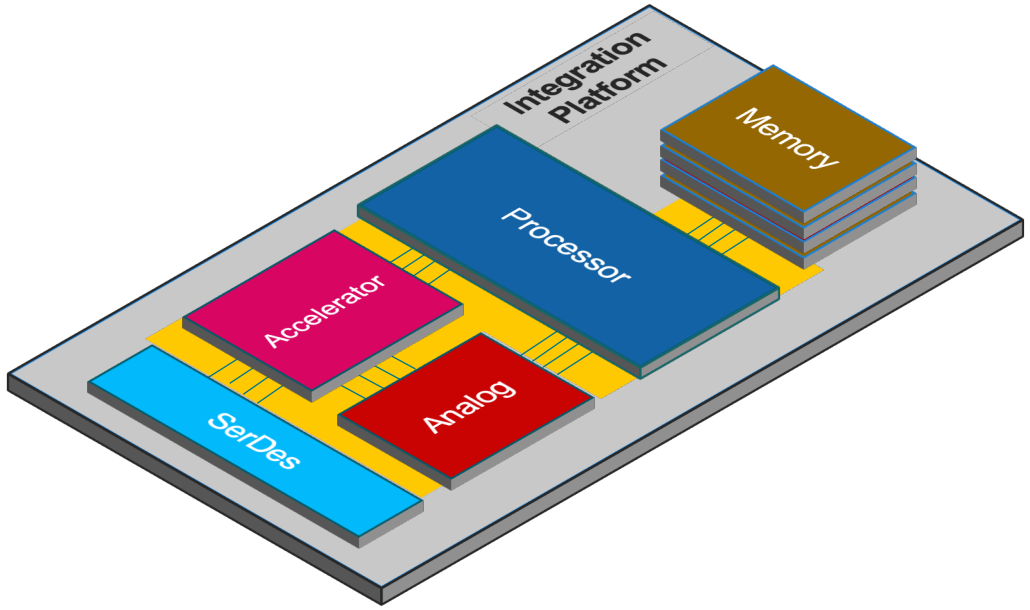


Die/Chiplet Stack Height

3DHI Ecosystem Challenges

Commercialization and Standards for Chiplets

- Most chiplet-based designs are in a closed ecosystem
- Business case for IP companies to provide 3rd type of IP
- Standard exchange formats are lacking
- Common communication interface
  - AIB, UCIe, BoW, OpenHBI, …
  - Too many packaging options to standardize on a single interface



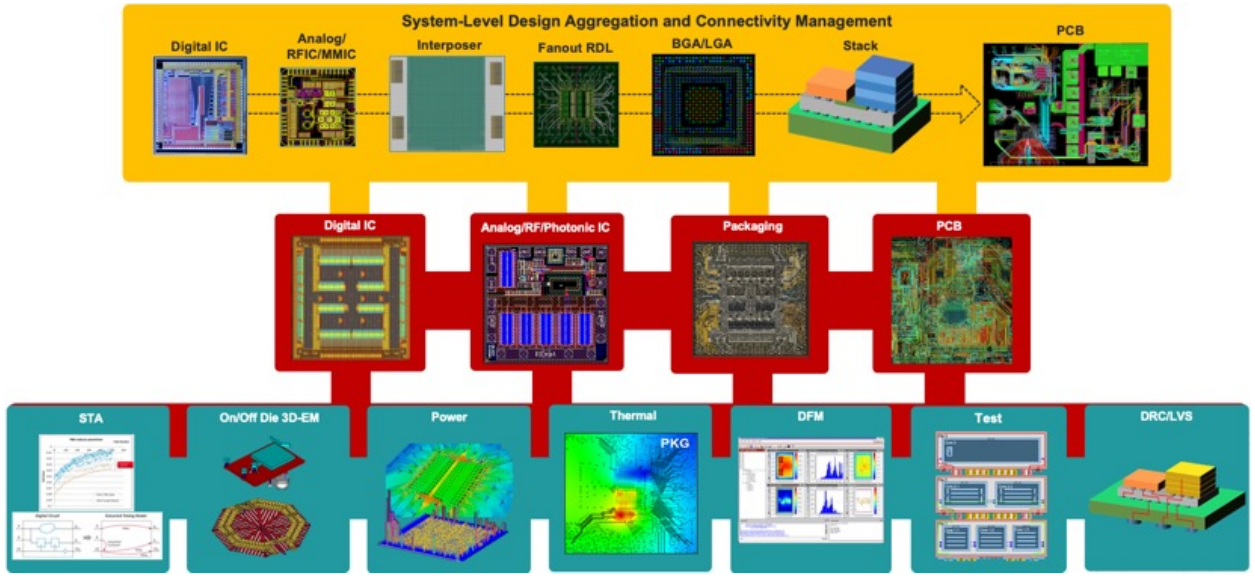
	Monolithic SoC/ASIC	3DHI
Cost	High	
Effort	High	
Risk	High	
Power		2D 3D
Performance		2D 3D
Area		2D 3D

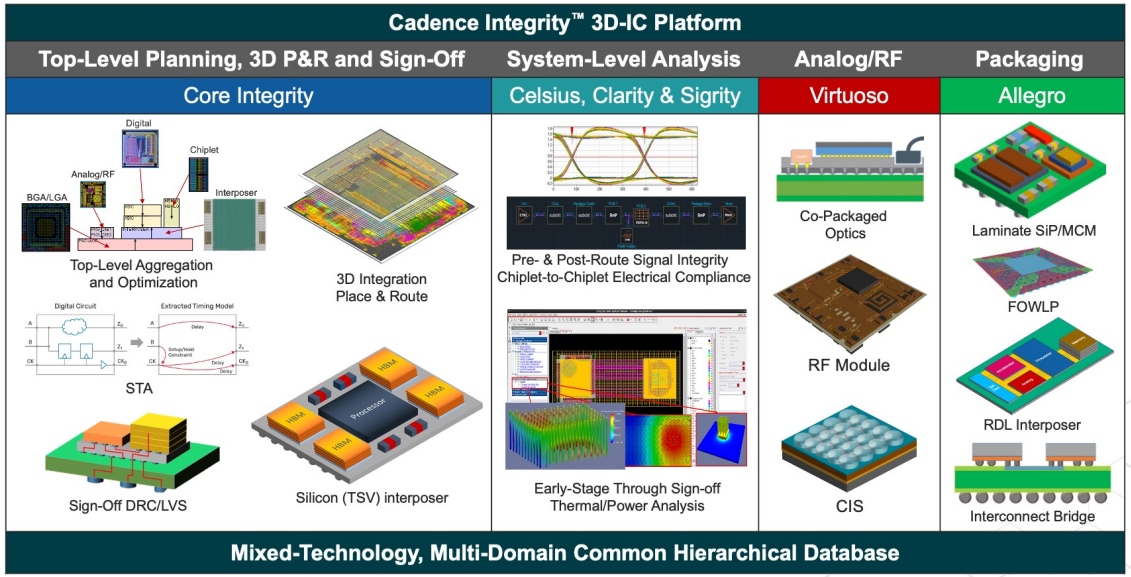
Interface Considerations Serial, Parallel or Proprietary
Package type
Reach (on/off package)
Power (pJ/bit)
Latency
Speed
Bandwidth
Routing complexity
Test, ESD, ???

3DHI Ecosystem Challenges

Complex Design Methodologies

- Explosion in the number of design tools required
- Design tools than support multiple PDKs (Tech LEF) in a single layout canvas
- Collaboration/co-design across multiple tools, design teams (Digital, RF, Systems) and across multiple companies
- Design partition strategies including D2D chiplets, thermal and off-package IO
- Limited capabilities for rapid prototyping with risk mitigation strategies

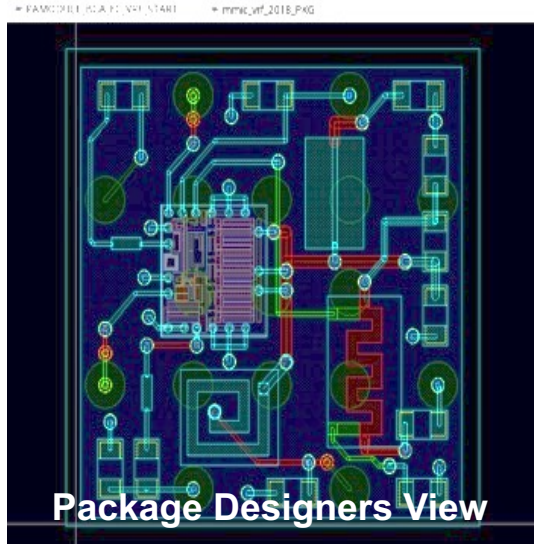


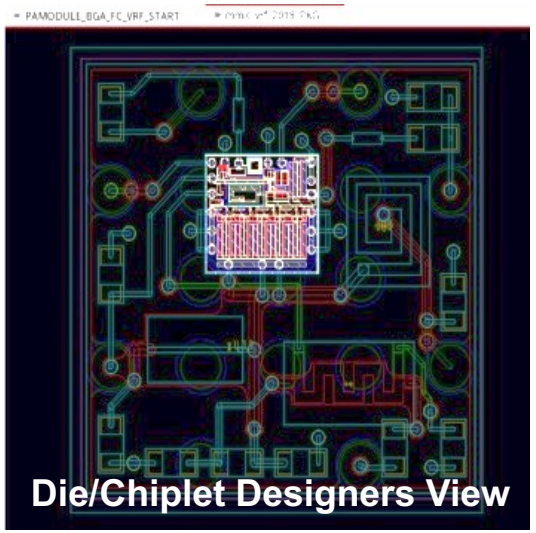


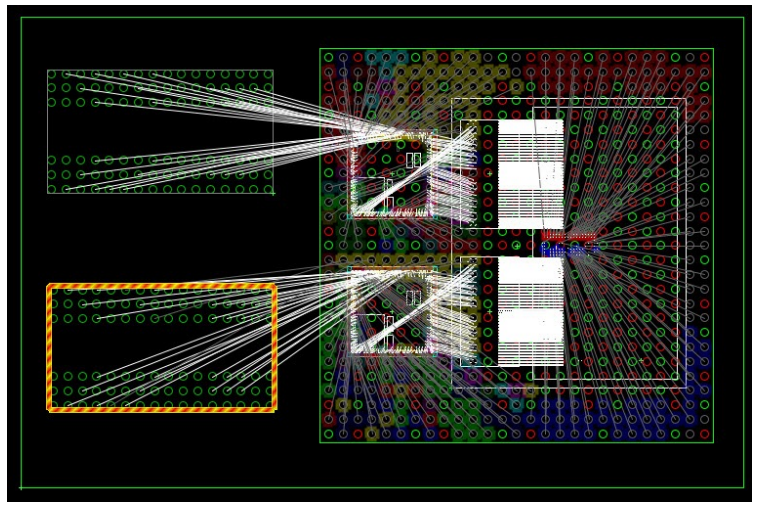
3DHI Challenges for the Package Designer

Cross-Domain Co-Design

- Concurrent planning/editing/optimization environment for IC, package and PCB
  - Abstract-level for early planning
  - Detailed-level for physical co-design
- Tight-loop ECO process between chiplet, package and PCB designs
- System-level LVS with support for rule-deck-free methodology
- Intelligent front-end (schematic/table) connectivity-capture-based flow



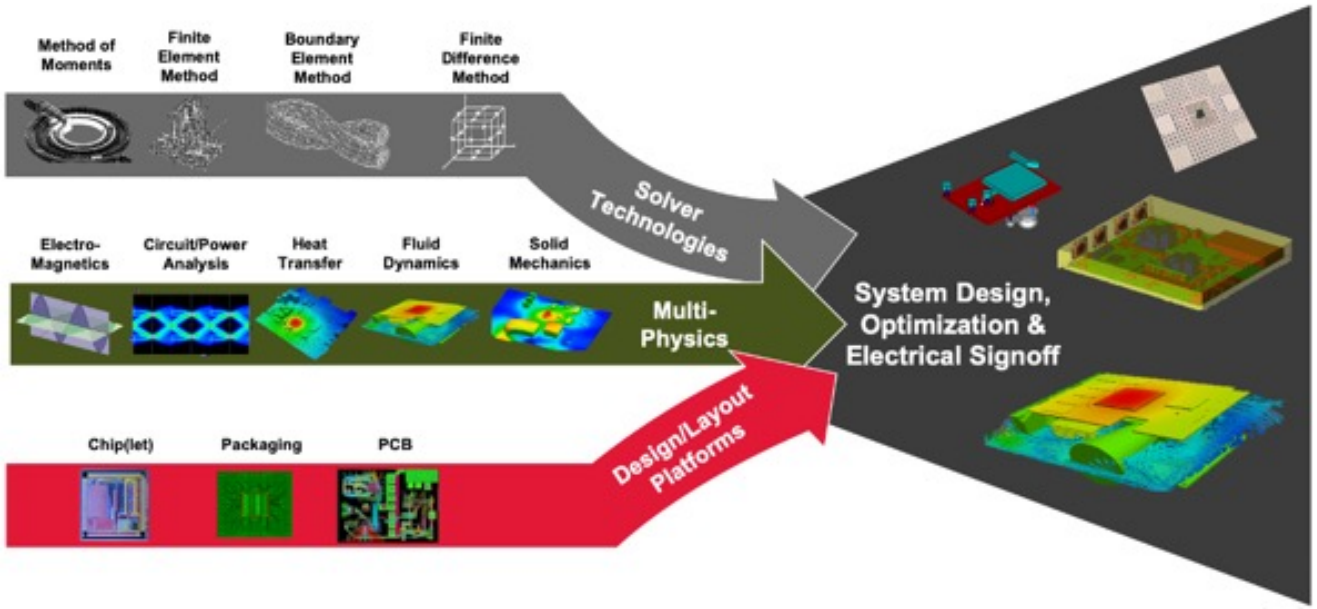


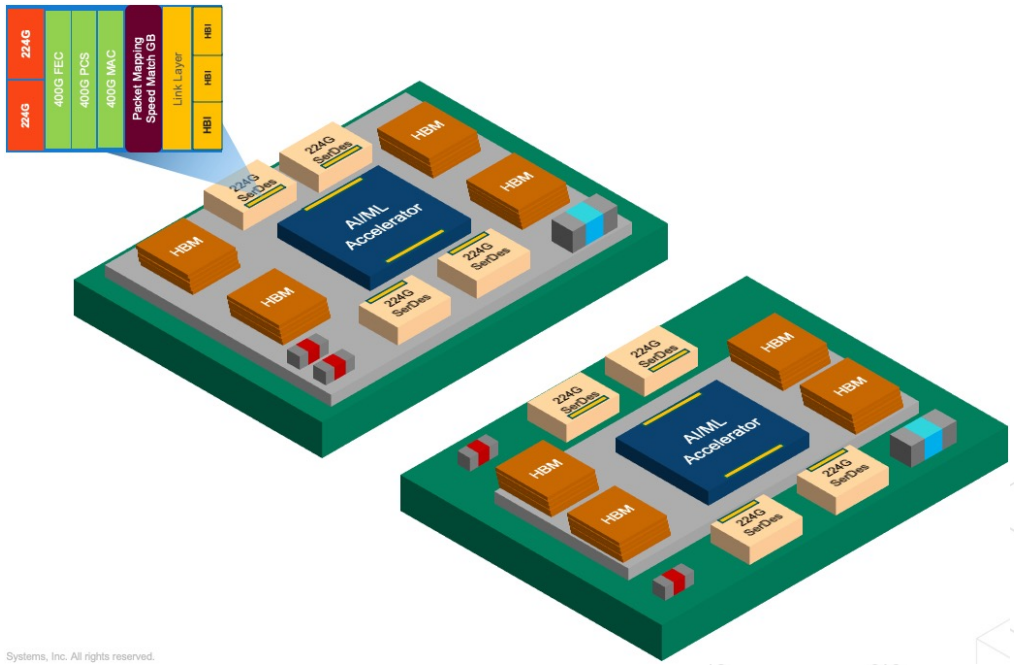


3DHI Challenges for the Package Designer

System-Level Analysis (SI)

- PCB-like analysis capabilities
  - Pre- and post-route chiplet-to-chiplet signal integrity and compliance
  - System-level power analysis
- Multi-physics analysis
- On-die EM/IR coupled with off-die electromagnetics

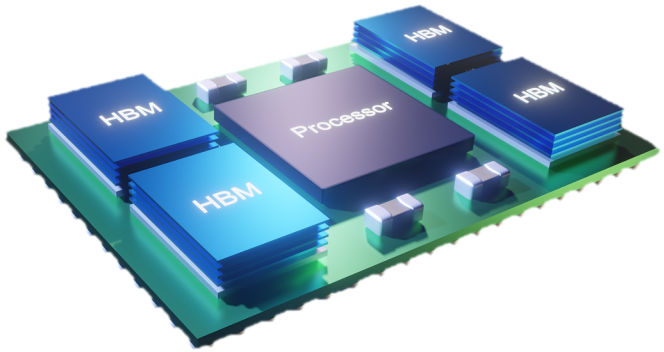


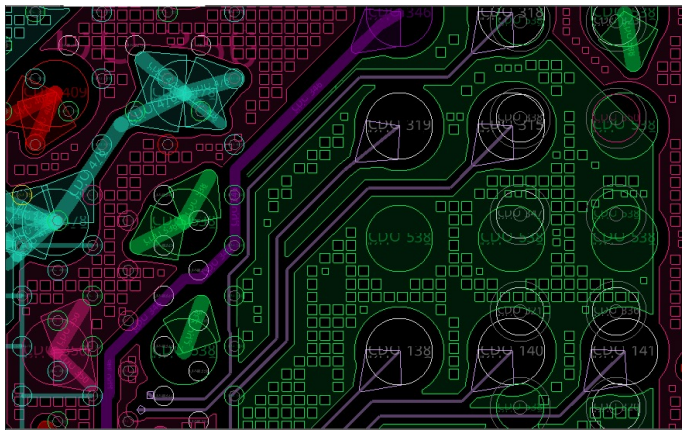


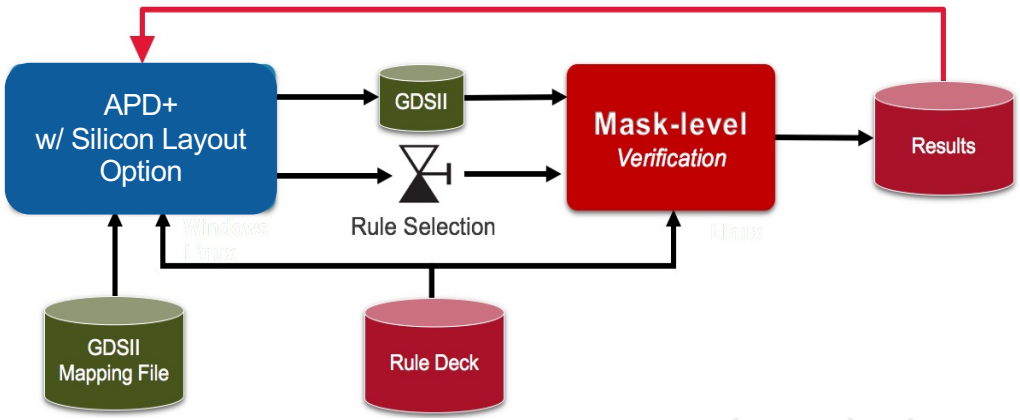
3DHI Challenges for the Package Designer

Silicon-Based Packaging Technologies

- Transitioning from laminate design to silicon design
  - Formal sign-off of DRC and LVS
- Differing power/ground routing styles
  - Stripes/rails and/or copper pour
- Advanced metal balancing
- Design capacity
  - Tens of thousands to hundreds of thousands (or more)



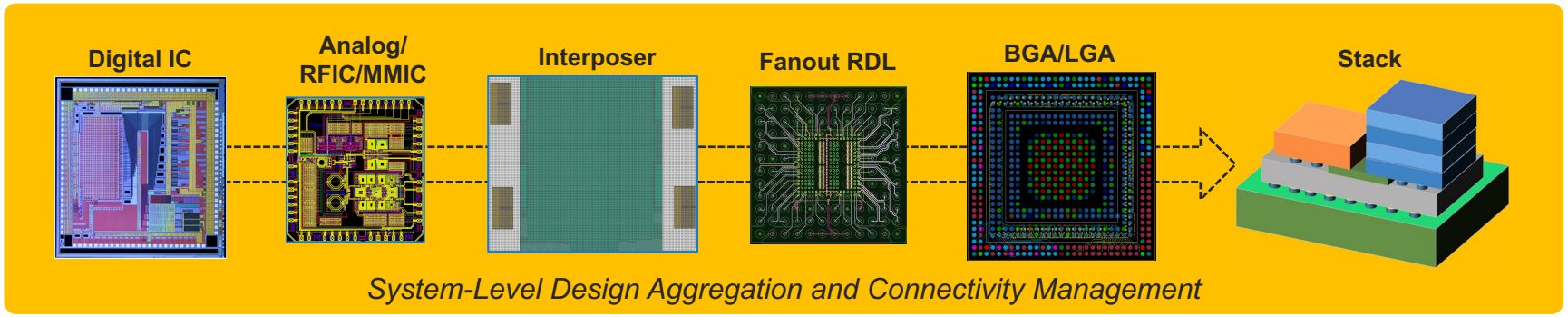




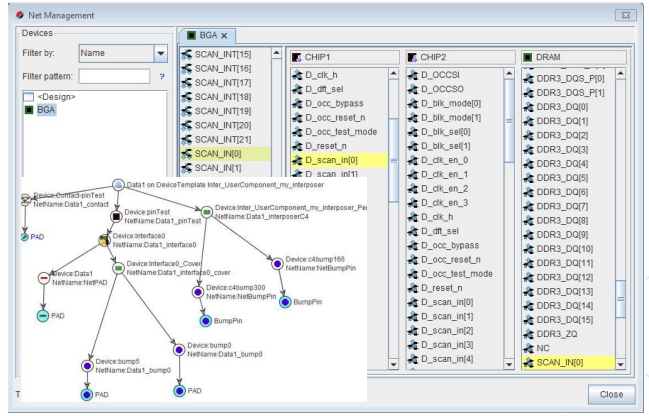
3DHI Challenges for the ASIC/SoC Designer

System-Level Design Aggregation

- Concurrent planning/editing/optimization environment for IC, package and PCB
- Common database for entire 3D-IC system
  - Chips, chiplets, tiles, packaging and PCB
- Early-stage thermal/power analysis
- Hierarchical netlisting
  - Source of golden/sign-off netlist
  - Partitioning by integration level



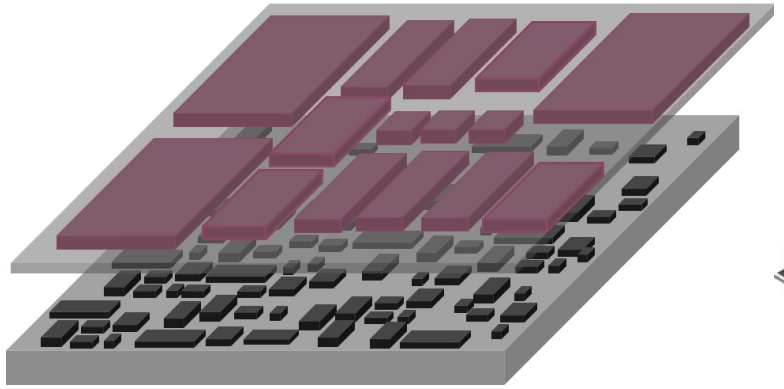
System-Level Design Aggregation and Connectivity Management

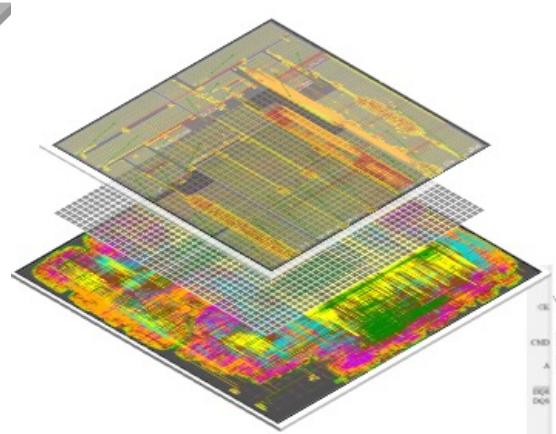


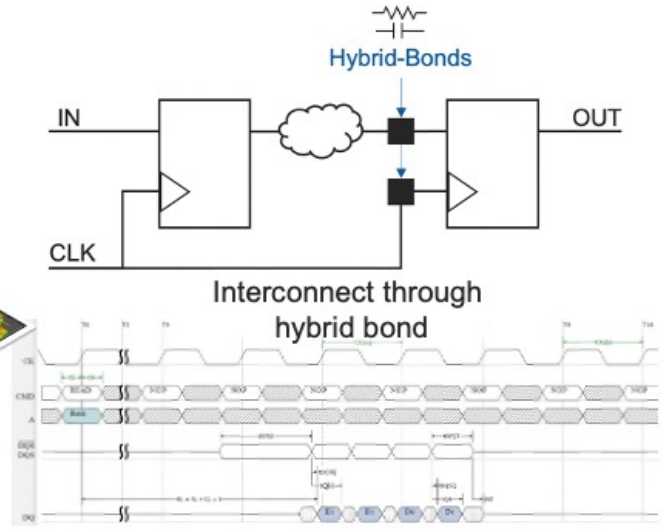
3DHI Challenges for the ASIC/SoC Designer

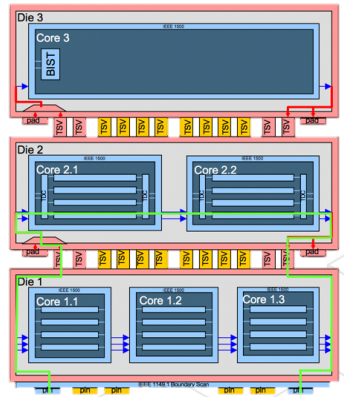
True Multi-Chiplet 3D Implementation

- Design size capacity
- Concurrent editing of multiple devices at full transistor-level detail
  - No abstraction
  - Homogenous and heterogenous
- On-the-fly die splitting and re-partitioning in Z direction
- Timing driven cross-chip(let) routing
- Support for 3D-IC test standards





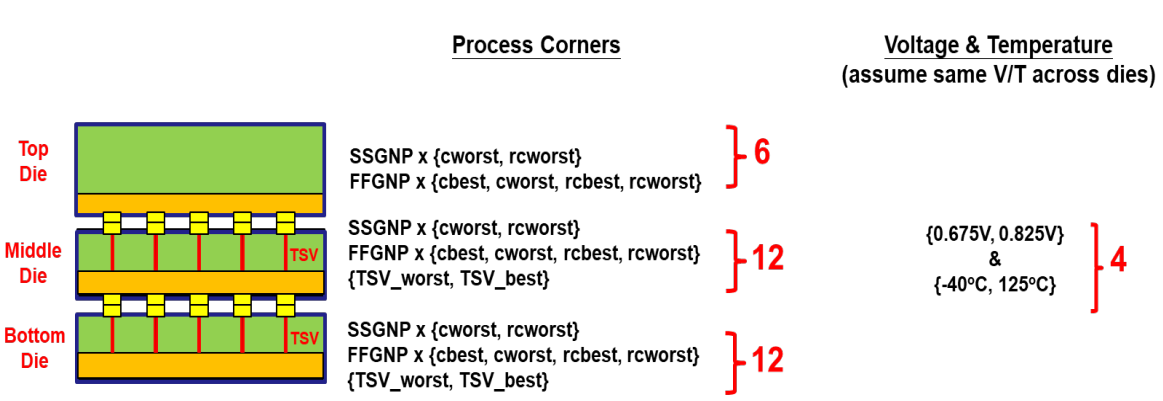


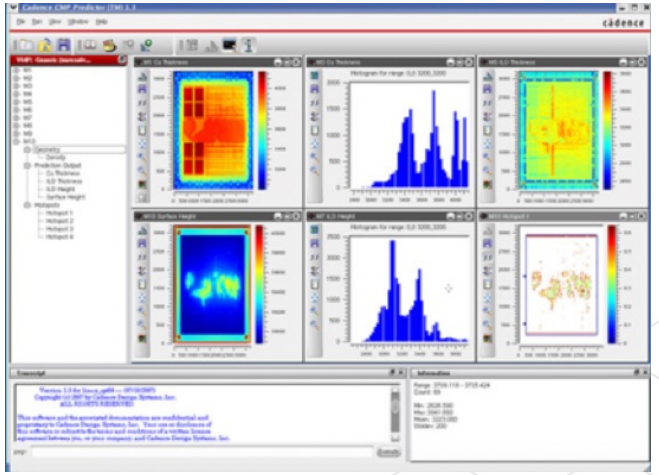


3DHI Challenges for the ASIC/SoC Designer

3D-Enabled Analysis and Sign-Off

- STA with automated corner reduction
- Rule-deck-free system-level LVS
  - Alignment and connectivity checking
- Multi-die EMIR
  - Accounting for dynamic loading across multiple die
- Comprehensive thermal stress and CMP planarity checks

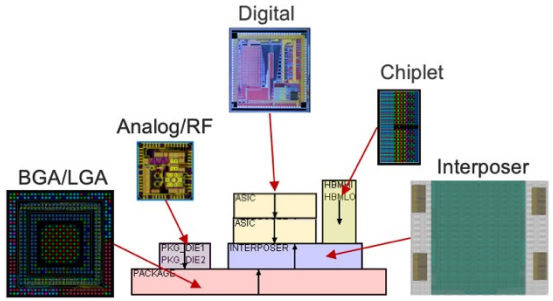




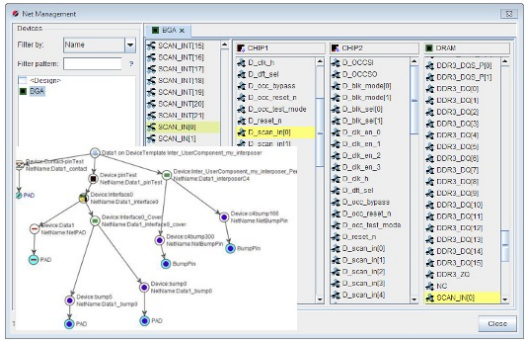
What to Look for in a Next-Generation 3D Integration Platform…

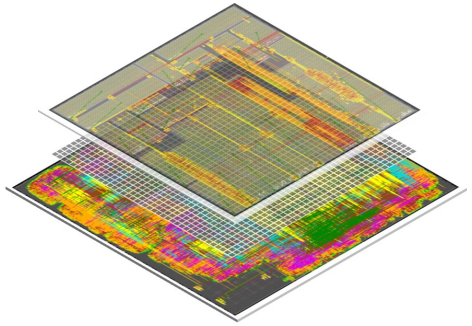
High-Capacity Common 3D-IC Platform

Top-Level Planning, 3D P&R and Sign-Off

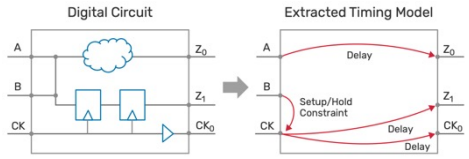


System-Level Aggregation and Optimization

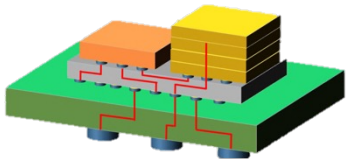




3D Integration Place & Route

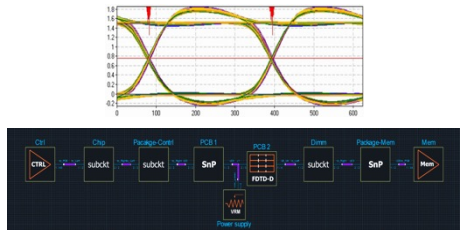


STA

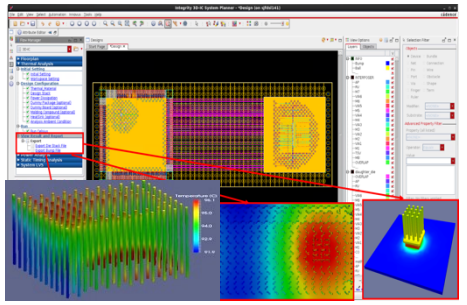


Sign-Off DRC/LVS

System-Level Analysis

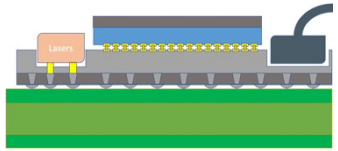


Signal Integrity

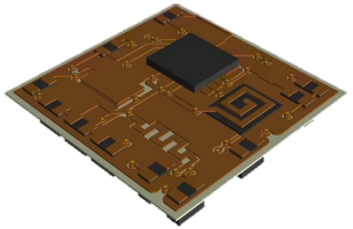


Early-Stage Thermal/Power Analysis

Analog/RF

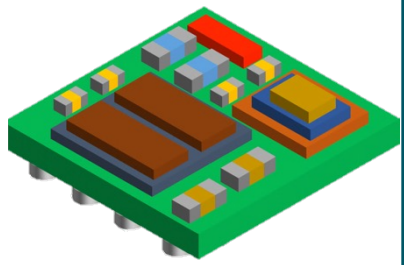


Co-Packaged Optics

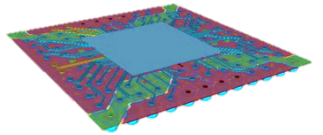


RF Module

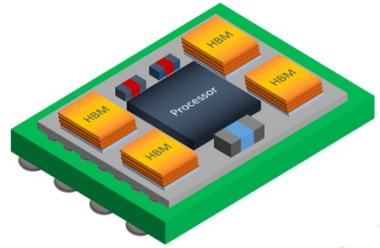
Packaging



BGA/SiP/MCM



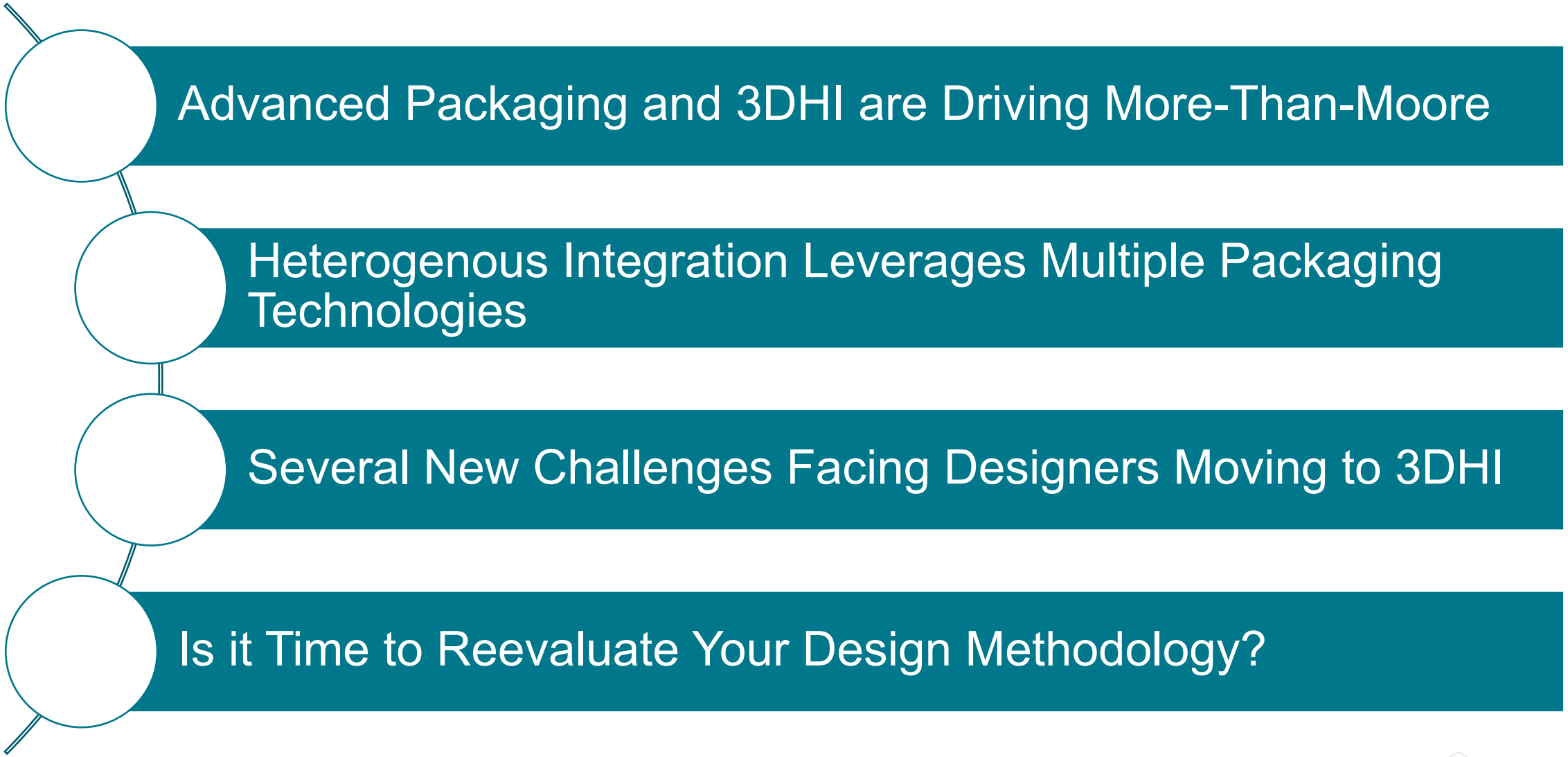
FOWLP



Silicon (TSV) Interposer

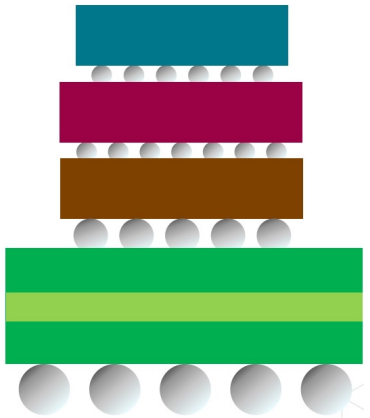
Mixed Technology, Multi-Domain Common Database

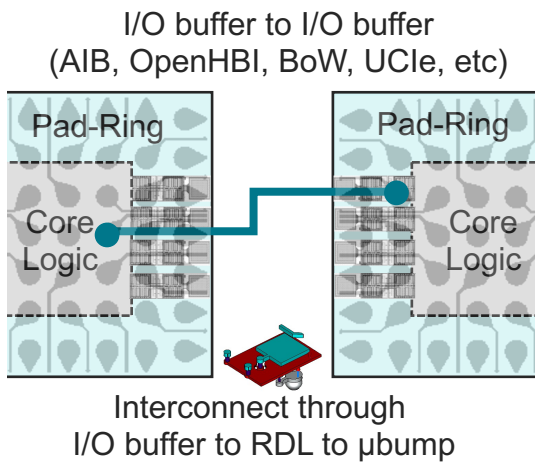
Summary



3D Packaging Versus 3D Integration

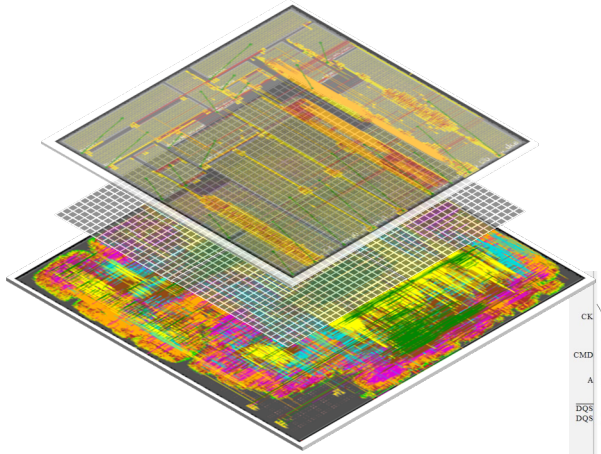
3D Packaging

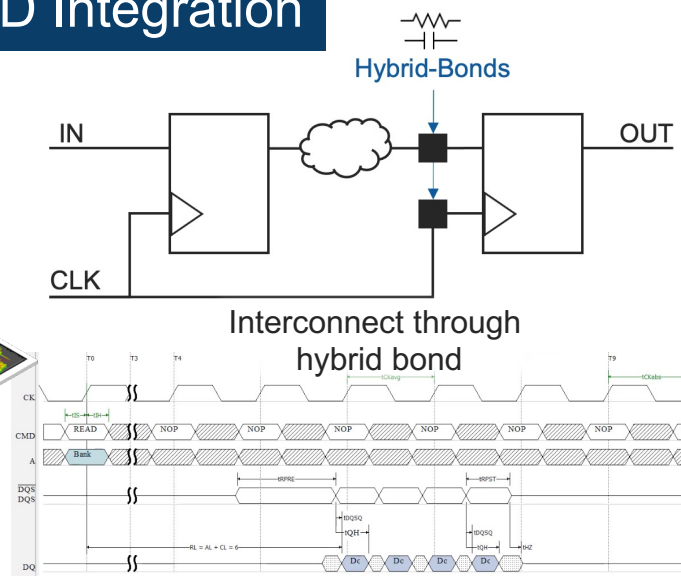




- (Micro)Bumped
  - Timing closed/signoff each die separately
  - Typically, no concurrent design of the dies
  - Common approach for Memory and CIS for over 5 years

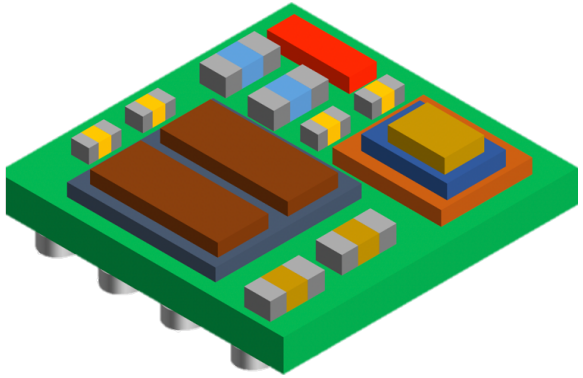
3D Integration

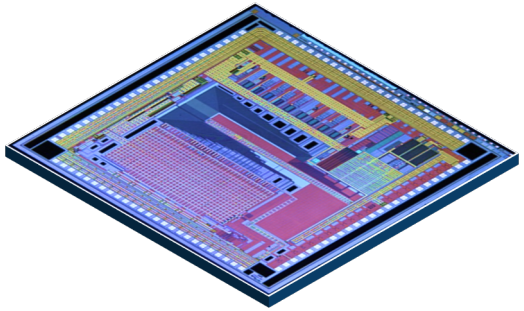




- Bump-less (Hybrid-bond/Cu-to-Cu bond, Direct bond)
  - No I/O buffers between die/macros
    - Concurrent design/analysis mandatory
    - Timing-driven routing and STA required for digital designs
    - Cross-die/chiplet route resource sharing
    - Z-dimension placement

Why Can’t We Have One Tool Than Can Design Everything?





	Package/PCB	IC
Use-Model	GUI-centric interactive place & route	Batch/script driven fully automated design
Placement	Tens of devices, mechanical structures/restrictions, 3D assembly rules **Abstract representation of die(s)/chiplet(s)**	Hundreds-of-thousands of instances, standard-cells (all the same height) and macros, partitioned into multiple blocks
Routing	Constraint-driven, push/shove 45-degree/all-angle routing, vias larger than traces, metal fill power planes. Passive interconnect substrates	Timing-driven routing, 90-degree, Vias smaller than metal routing, gridded power routing. Active (device + metal layers) substrate
Capacity/Performance	100,000s	1,000,000,000s
Extraction/Analysis	3D-EM, System-Level SI/PI, IO-to-IO timing	RC extraction, Flop-to-flop timing
Manufacturing Outputs	Board/Substrate (informal sign-off)	Foundry (formal sign-off DRC/LVS)
OS	Windows	Linux

COPYRIGHT NOTICE

The content of this presentation is the work and opinion of the author(s) and is reproduced here as presented at the **Road to Chiplets: Design Integration** (May 10-12, 2022).

www.meptec.org

MEPTEC
THE NEXT GENERATION