Road to Chiplets: Heterogeneous Integration Testability

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Die and Probe Layout Strategies to Enable Probing Best Practices for Heterogeneous Integrated Products

Will Thompson, March 16

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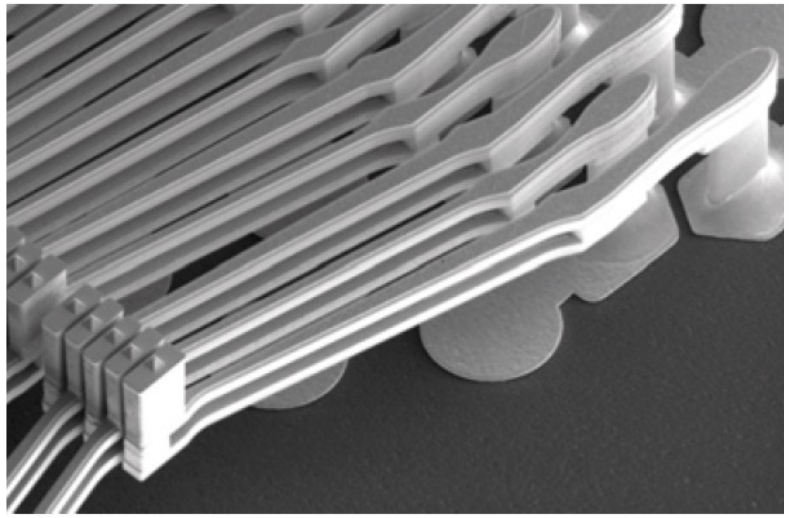
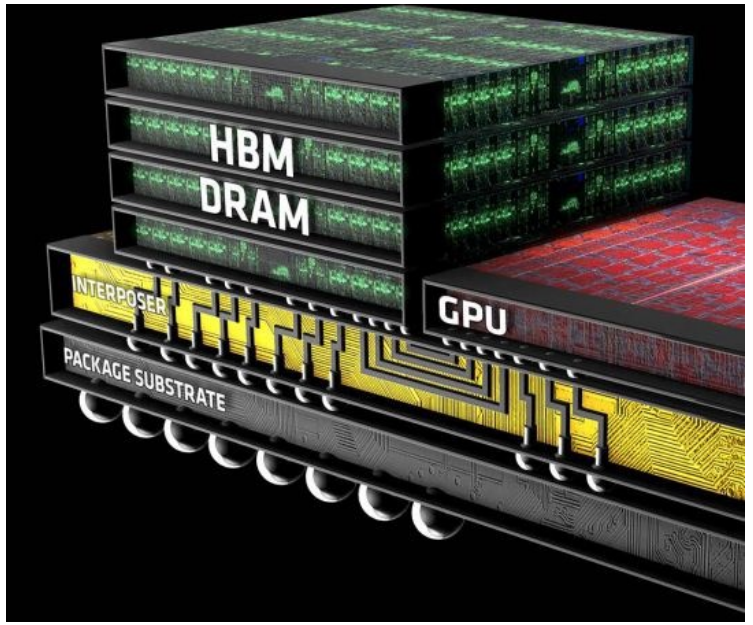


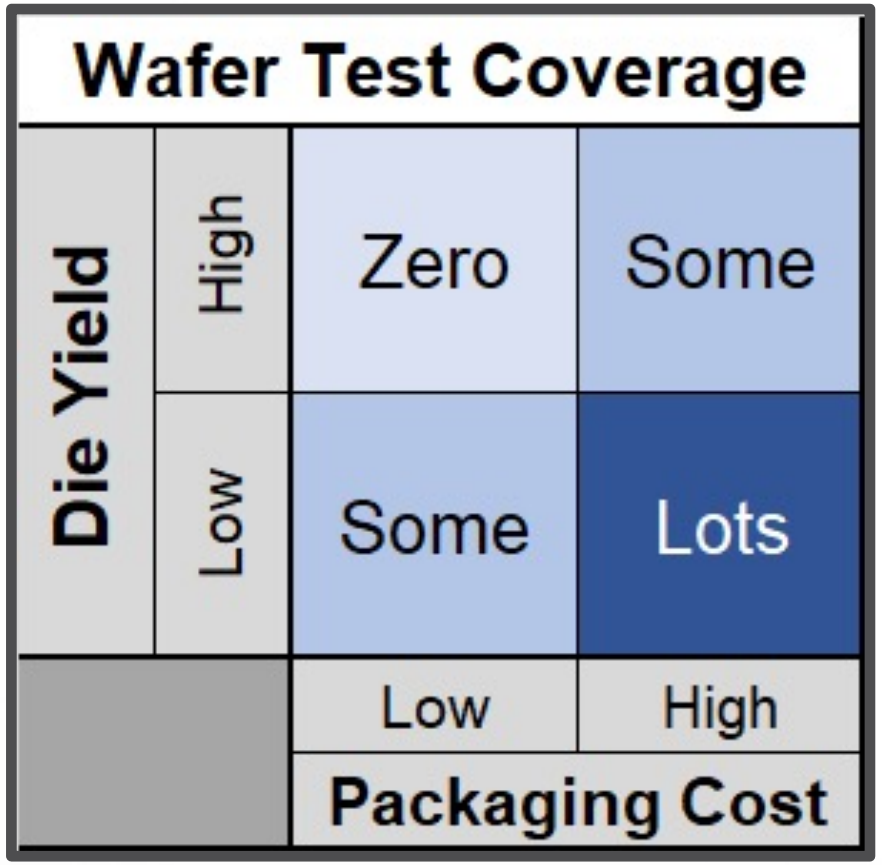
Industry's Call for KGD

- Each Heterogeneous Integrated (HI) product contains multiple chiplets that each likely require probe test
- The exponential arithmetic of composite yield loss has led to calls for Known Good Die, or KGD, coming out of probe.
- Even for classical monolithic die, KGD gets expensive for two reasons
  - To test a leading-edge chip at speed while physically contacting each I/O and power pin on the die requires a very complex and costly tester and probe card
  - To verify a 100%-fault-free results in long test times → throughput of tester and probe card is low



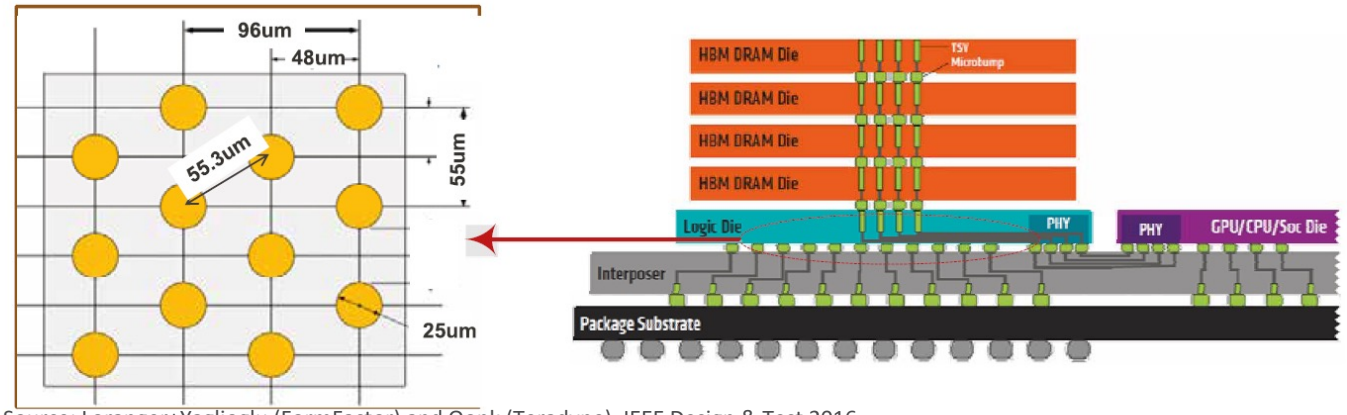
Source: https://www.anandtech.com/show/9390/the-amd-radeon-r9-fury-x-review/3

Why do Customers Pay for Wafer Test?



- Probe is inherently a cost-saving product
  - Optimal utilization sacrifices KGD to keep the cost of probe low while preventing downstream scrap
- To maintain the ROI of probe, it is important to find ways to decouple probe pitch demands from rapidly tightening microbump pitches

Microbumps and Probe Cards



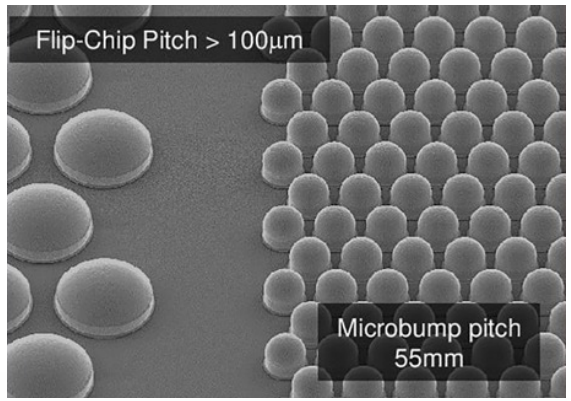
Source: Loranger+Yaglioglu (FormFactor) and Oonk (Teradyne), IEEE Design & Test 2016

- Microbumps are a high-density (40-50 µm pitch) method to connect chiplets
  - Microbumps formed during wafer fab via electroplating instead of post-fab deposition

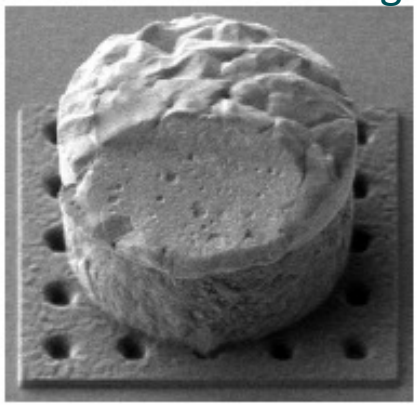
Challenges

- 50,000+ contacts in a one-centimeter square footprint: two to four times denser contacting patterns than an equivalent monolithic device.
- Microbumps have stringent probe-induced damage criteria to prevent downstream yield loss.
- Though the newest MEMs-type vertical probe arrays can accurately touch down on fine-pitch microbumps, it is often economically unfeasible

SEM After Probing



IEEE Spectrum, April 2019



Marinessen, *Direct Probing on Large Array…* ITC 2014

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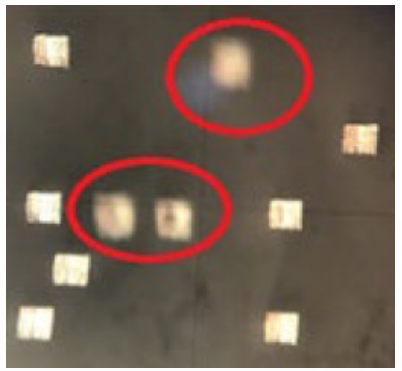
Hybrid Bump and Probe Layouts

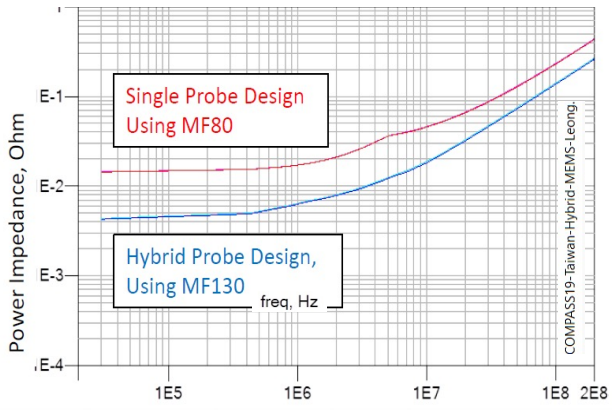
- Hybrid Bump Layout = allowing space for a bigger probe where large currents or high-power densities are required AND allocating fine-pitch, high-speed I/Os separately
  - Requires flexibility from wafer designer
  - Partitioning the real-estate on the die this way makes the job of probe a little easier which keeps the cost of the probe card down

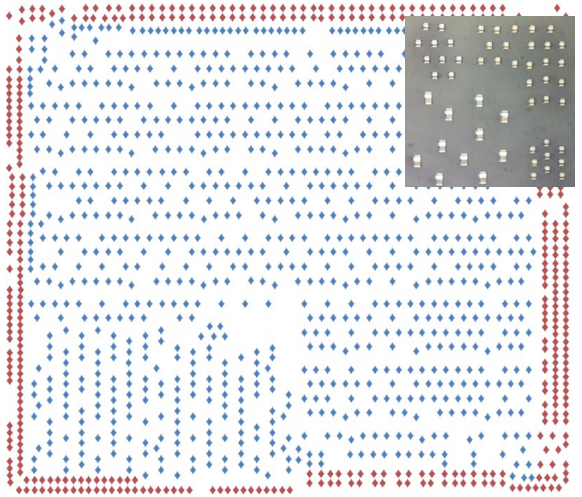
- Enabling the use of lower-pitch probes enables higher current probes which are less likely to burn out during high-current testing
  - Probes that have exceeded their MAC exhibit planarity differences (right)



Example

A probe array with two different probe types. The powers and grounds are in the center of the array with more spacing to allow for a larger probe with 60% higher Maximum Allowable Current (MAC) and better Power Impedance (PI)





Source: Leong, Amy. "Hybrid MEMS Probe Technology…" *Compass*, FormFactor, 2019, compass.formfactor.com/wp-content/uploads/COMPASS19-Taiwan-Hybrid-MEMS-Leong.pdf

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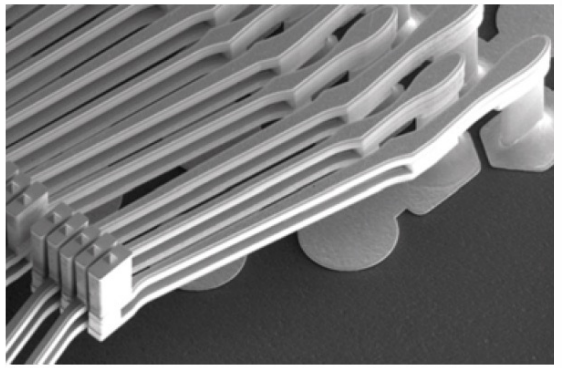
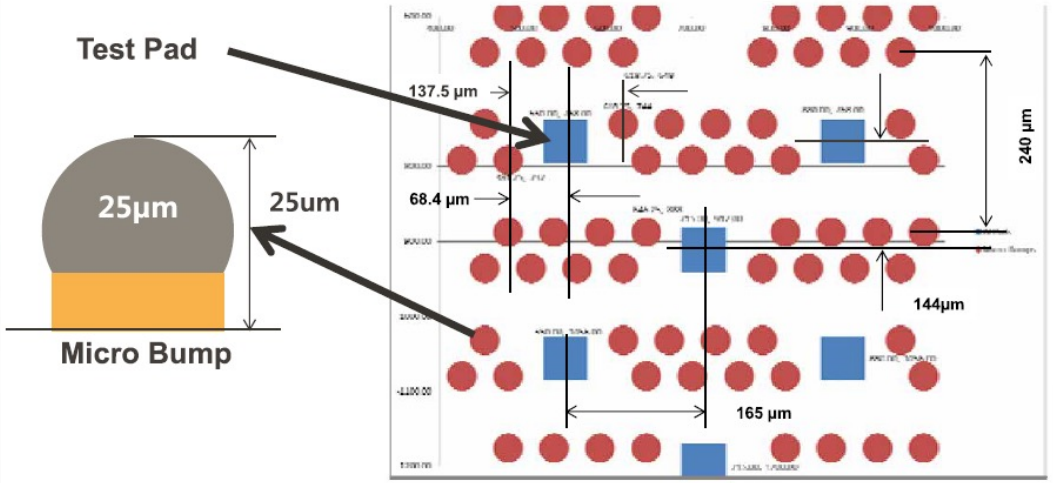
Employing Test Pads Among Microbump Arrays

- Designers can integrate dedicated probe pads within the component die design to enable use of traditional DRAM cantilever probe technology
  - Enables full-wafer contact → Higher parallelism → Lower cost test
  - Avoids directly probing the TSVs that will form the die-to-die connections in the multi-die stack
  - These “dummy” pads won’t be used for wire-bonding, so the size and pad damage constraints can be relaxed.





- Requires effort and flexibility from wafer design
- Costs space on the die

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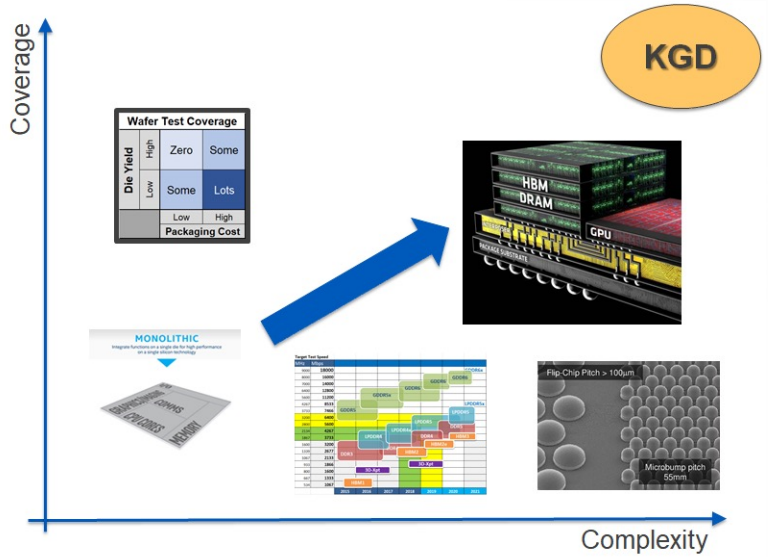
Conclusion

- Increasing test complexity and coverage is unyielding
  - KGD is economically impractical to achieve – continuously moving goalposts



- Creative methods to save cost on probe are not limited to the ones mentioned previously
  - Ex: Touching multiple microbumps with a single probe
  - Ex: Skipping some bumps while using BIST and DFT to make up for the loss in resolution
  - Ex: Reduce the compliance for overtravel requirements
  - …and?

- Wafer and probe designers should communicate to find ways to loosen the demands of probe to achieve cost-effective testing

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