



Road to Chiplets: Heterogeneous Integration Testability

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Test Economics in a Disaggregated-Die world

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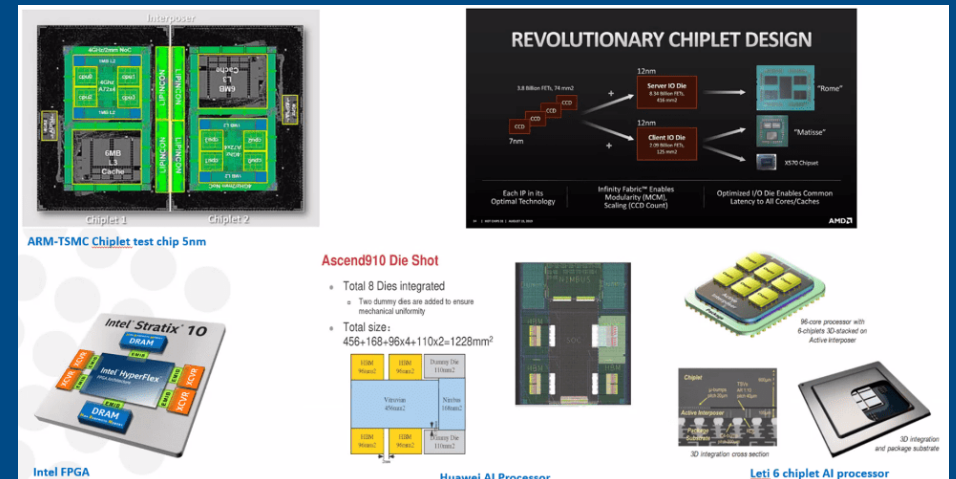
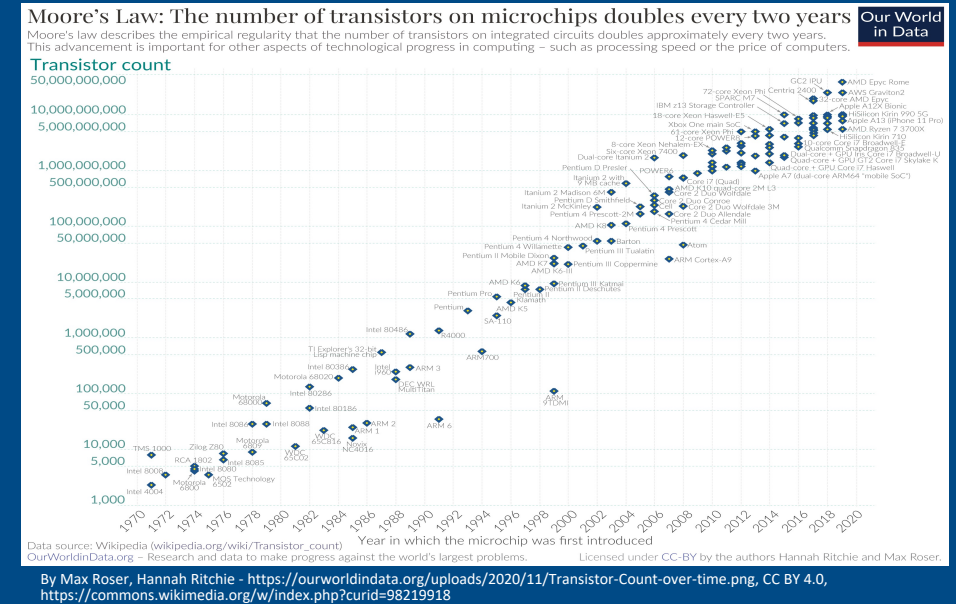
Co-Authors: Pooya Tadayon, Greg Iovino

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Die Disaggregation is the future

- Industry is moving rapidly towards heterogenous integration and die-disaggregation
- Driven by the continuous need to extend Moore's Law as transistor sizes approach atomic scales
- Performance IPs on cutting edges nodes
- Other IP blocks on older, higher yielding (and cheaper) process nodes
- Smaller chiplets result in higher yields



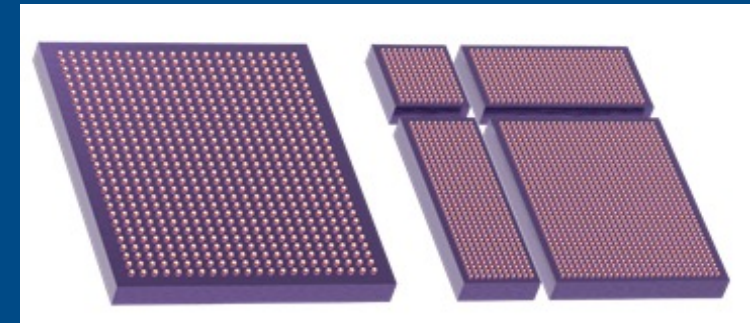
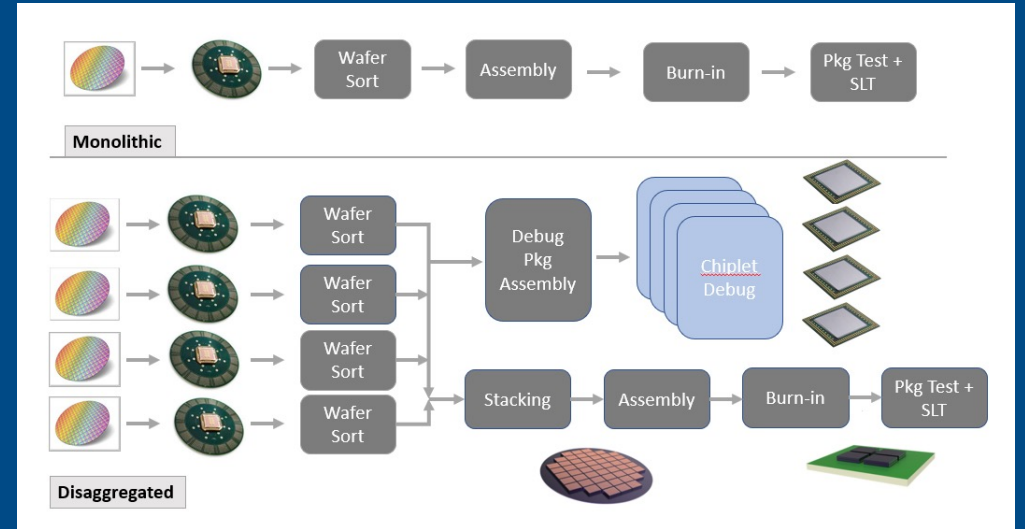
Ack: <https://semiengineering.com/waiting-for-chiplet-standards/>

Die-Disaggregation – Impact on Test Ecosystem

- Disaggregation is driving major impact to test eco-system
- High test complexity, test cost and HW / capital costs
 - Need to rely on a KGD strategy to minimize package yield loss
 - Added complexity / test-time in Sort test for "characterized KGD"
 - Individual Probe Cards for each chiplet – added cost
 - Tight pitch micro-bumps pose signal integrity challenges – leading to complex IO test methods and differences between Wafer Sort & Pkg test
 - Testing of D2D interconnect introduces additional cost/complexity

Test HW Impact

- Individual Chip-lets drive up Probe Card count
 - A 4 die disagg product needs 4 probe-cards – typically at the same time – added stress on the supply chain
 - Increased cost for multiple die HW collaterals
- Individual die may be packaged into standalone ‘debug’ packages for easier pkg debug/FA
 - Additional pkg costs; additional HW costs
- Disagg drives the need for dense D2D interconnect because of connectivity requirements between IP blocks
 - This drives up probe count, aggressive pitch reduction and high-density micro-bumps
 - More complexity and cost adders to probe card



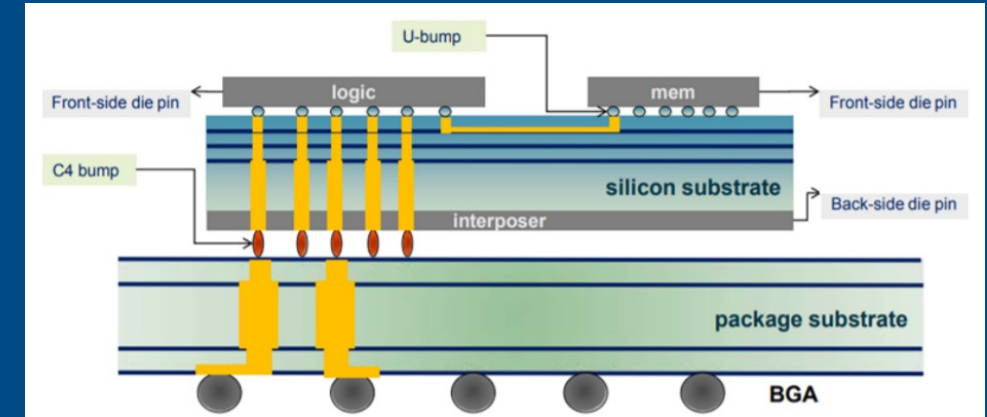
Dense pitch micro-bumps on disaggregated die

Test overhead and test complexity

- Basic Test Overhead needs to be repeated for each chiplet wafer sort
 - Connectivity, CRES, Shorts / Opens -- Added test-time per chiplet
- Traditional wafer test parallelism techniques conflict with increased testability requirements
 - Test parallelism requires reducing probe counts per die (or higher tester channel count)
 - Reducing probes drive limitations at wafer-test and divergence with pkg test
 - Disagg die with tight pitch micro-bumps pose signal integrity challenges for high-speed IOs
 - Can be mitigated with DFT / loopback schemes but diverges with pkg test and can potentially cause higher yield loss downstream
 - All these trade-offs for cost v/s complexity need to be carefully considered

Si Interposer / Base Die Test

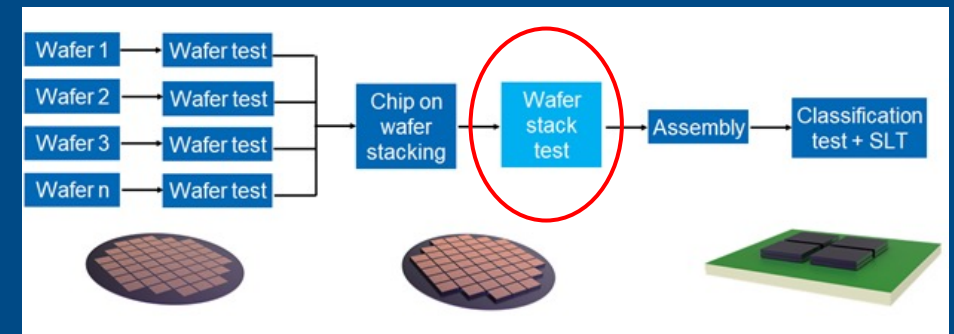
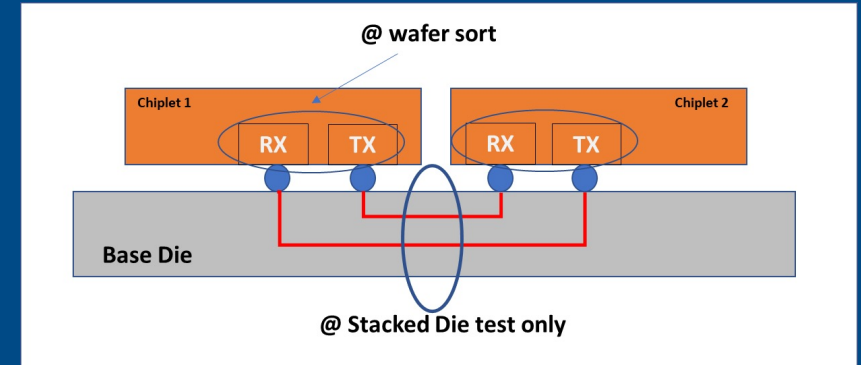
- Disagg drives usage of a passive interposer or Si bridge for D2D interconnect
- Base-Die test strategies need to be considered
 - Blind-build and rely on low DD
 - Incorporate test and redundancy techniques
 - design / DFX complexity / higher test-times
 - Incorporate sampling strategies



**Si-Interposer / Base-Die test
driving new test-cost /
complexity in a die-disagg
future**

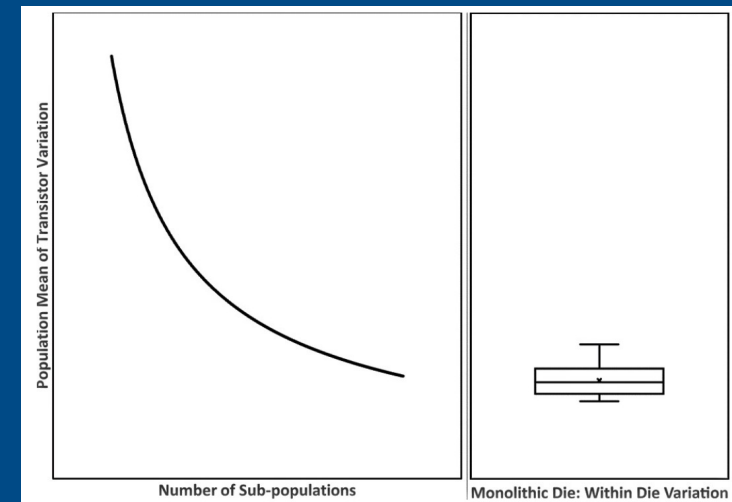
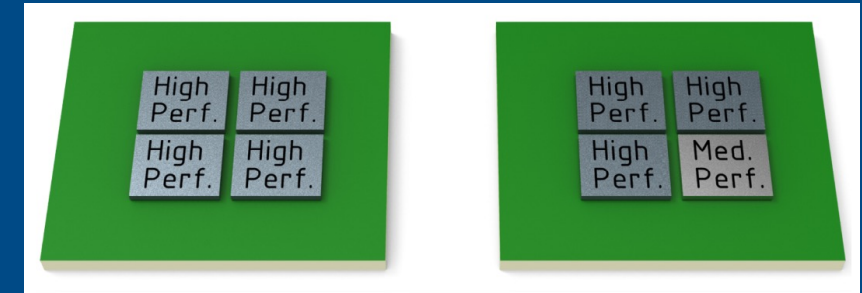
KGD and Stacked Die Test

- As number of chiplets in a die stack grows, the overall yield reduces
- This drives a higher need for KGD at wafer-sort
- D2D interfaces cannot be fully tested at Sort
 - Full interconnect cannot be tested at Sort (only one side of Tx/Rx buffers is accessible)
 - D2D connections not exposed to package can only be accessed once the stack is assembled
- Drives a need for a new stacked-die test socket
 - Additionally, redundancy / repair of interconnect need to be built in – additional dfx, die-area and test complexity



Die Disagg and “Characterized KGD”

- Die Disagg places additional demand on chiplet characterization prior to stacking
- Die of similar performance characteristics should be paired together for optimal power/frequency performance
- Characterization at wafer level is not trivial
 - Drives additional test content / test-time
 - Need to account for power delivery differences between package and wafer-sort
 - Chiplets from different suppliers with different technologies drive complexity and cost higher.



Intelligent segregation of chiplets into several discrete sub-populations reduces chiplet to chiplet variation

Summary / Call to Action

- Die disaggregation causing test-cost per transistor to rapidly approach/cross per transistor cost
- Disagg causes greater test complexity / test cost
 - Added complexity / test-time in Sort test for "characterized KGD"
 - Denser probe cards with large number of micro-bumps at tight pitch and overall increase of probe cards drive up capital costs
 - Base-Die / Silicon interposer testing required – yet another test cost adder
 - Stacked-Die test socket insertion needed to fully test D2D interconnect – added TPT and test-cost
- As interconnect density increases, technologies such as hybrid bonding will further exacerbate test complexity and test cost challenges

Stronger collaboration needed between Design, Packaging and Test to ensure manufacturing solutions are optimized for test cost

References

- Moore's Law and the future of test (Pooya Tadayon, Greg Iovino, Sameer Ruiwale) – Chipscale Review May/Jun 2021
- 'More Than Moore' Reality Check (Anna Steffora Mutschler)
- Data and Test - Sreejit Chakaravarty: Chip-lets Interconnect Test Challenges

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