Road to Chiplets: Heterogeneous Integration Testability

March 15 & 16, 2022

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Test Impacts of Multi-Die Packages

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March 2022

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Agenda

1. Integration End Markets
2. Assembly Package Integration Technologies
   - Amkor Examples
3. Opportunities & Impacts to Test; Call for Action

Amkor Integration Market Applications

Automotive, Health, Industrial

ADAS, SiP/IVI
MEMS, sensors
Performance, safety

Communications

5G, RF & mixed signal
Handheld devices
Mobile/Smartphones
Tablets, IoT, satellite

Artificial Intelligence, Networking, Computing

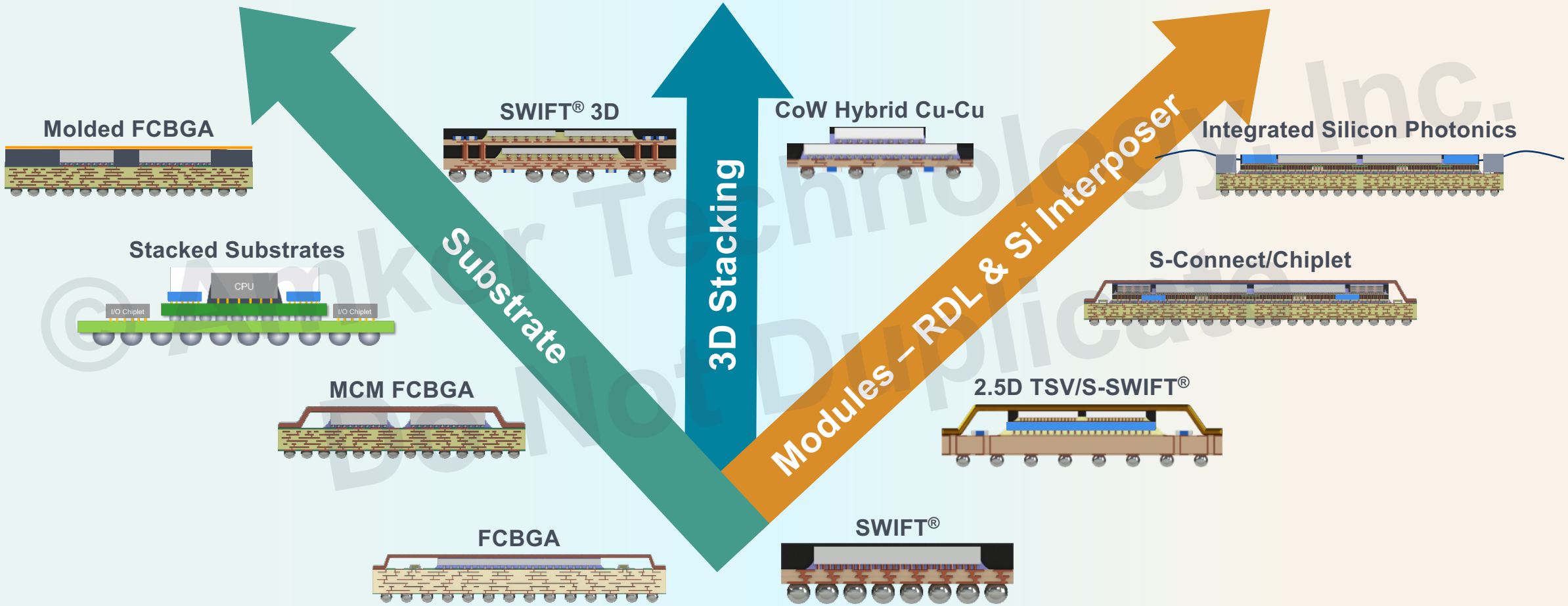
Networking
Data center, infrastructure
PC/Laptop, storage

Consumer

Connected home
Set-top box, televisions
Visual imaging, wearables

Multi-die packages are ubiquitous!

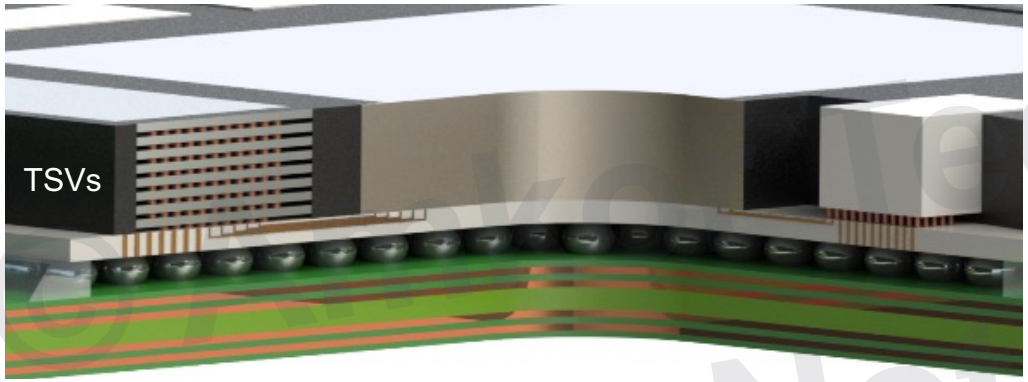
Amkor Multi-Die Package Technologies

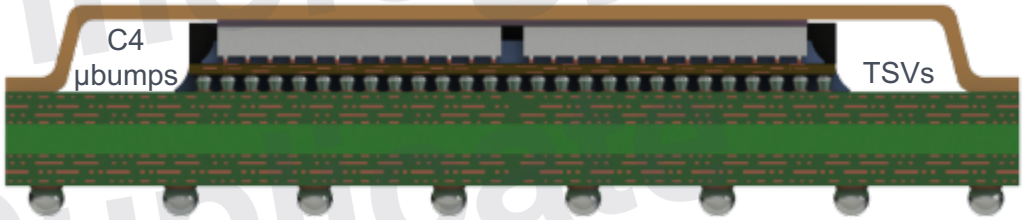


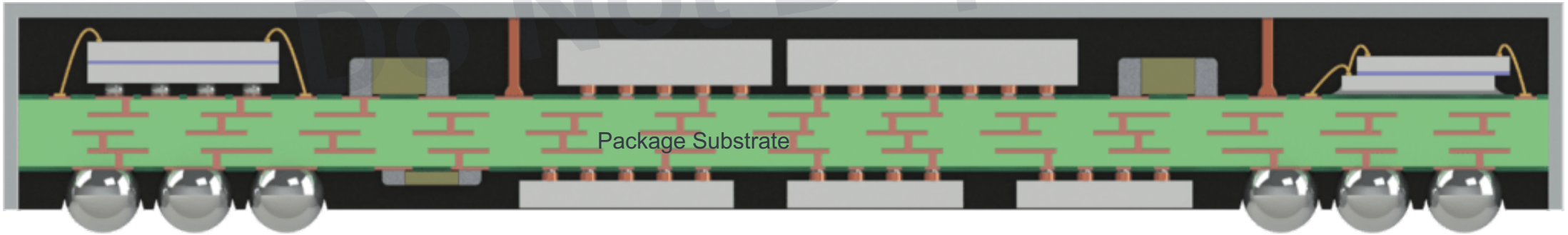
Die disaggregation, to allow higher levels of integration!

Amkor Package Assembly Topologies

ASIC/CPU/GPU/FPGA, high bandwidth memory

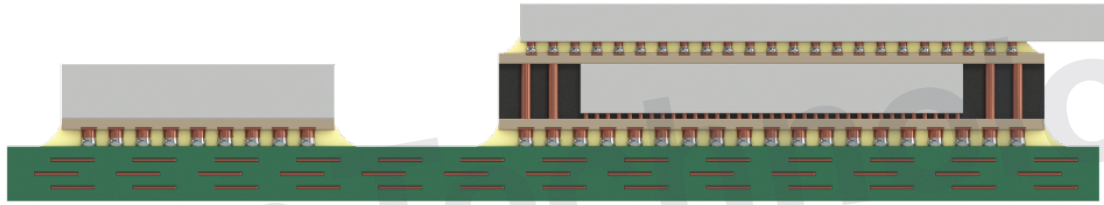


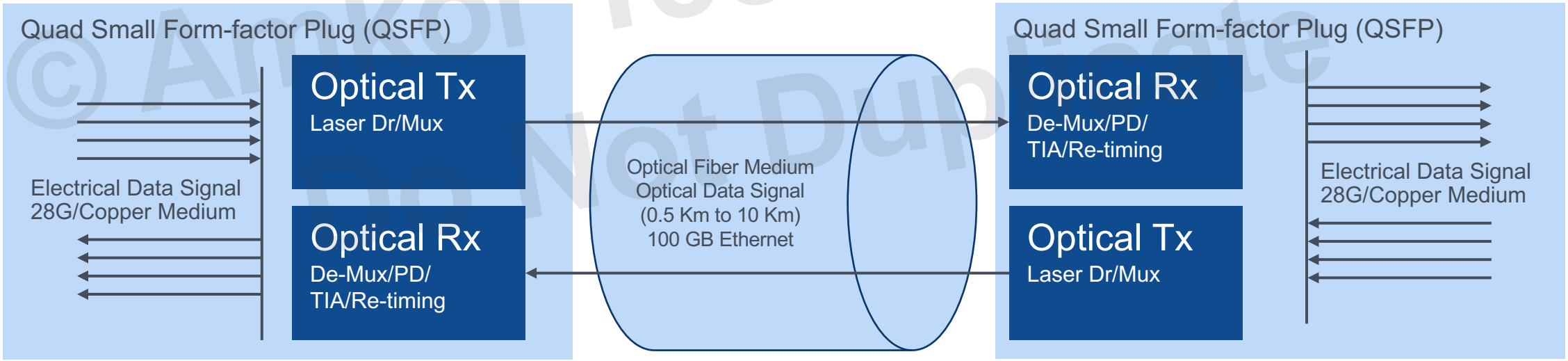




Amkor Package Assembly for Si Photonics

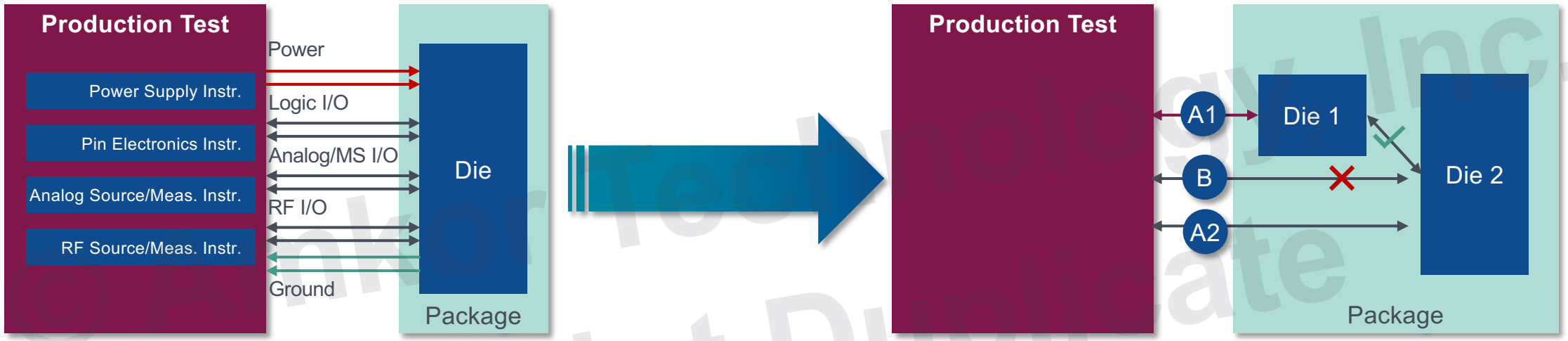
Enabling 100 to >400 Gbps data rates





As packaging complexities increase, new matching test methodologies must be architected

Production Test Challenges



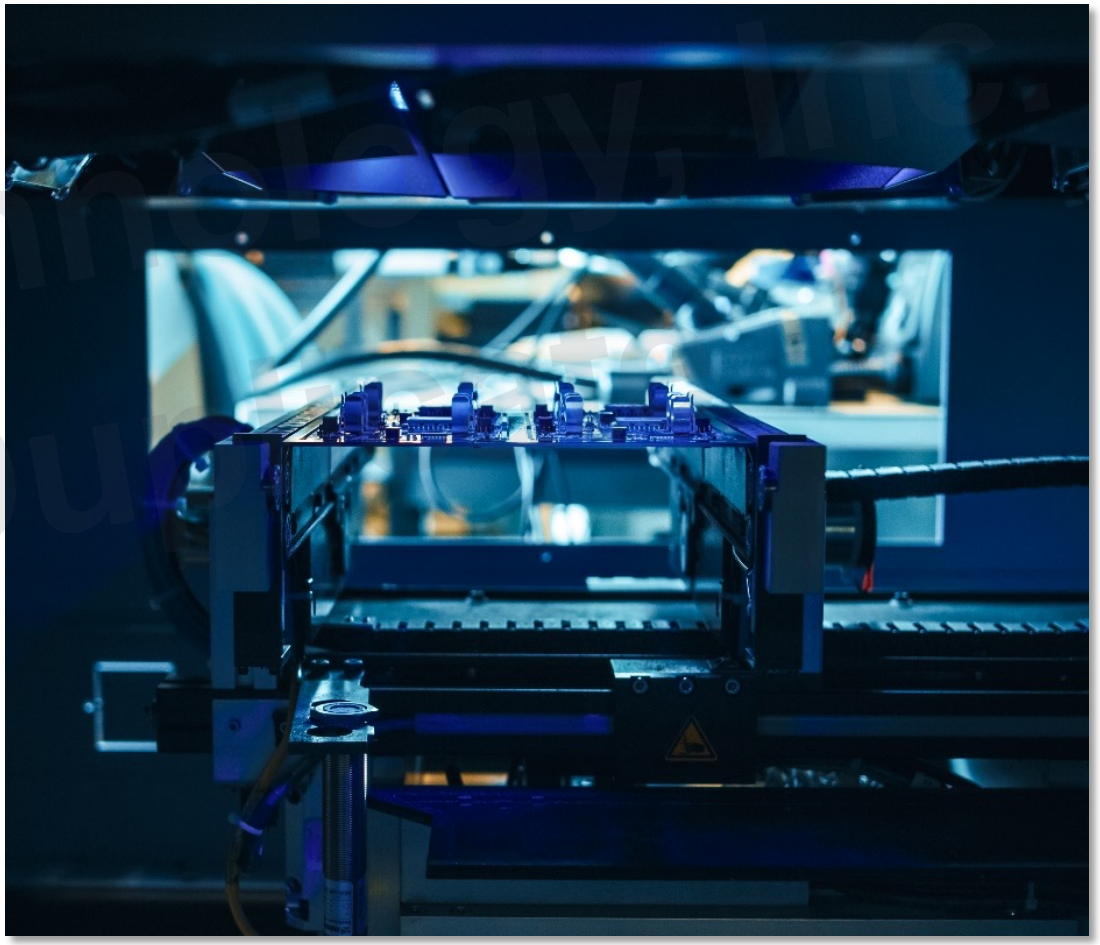
- No direct access
- Radiative access
- Digital system bus protocol

Die 2 interface physically

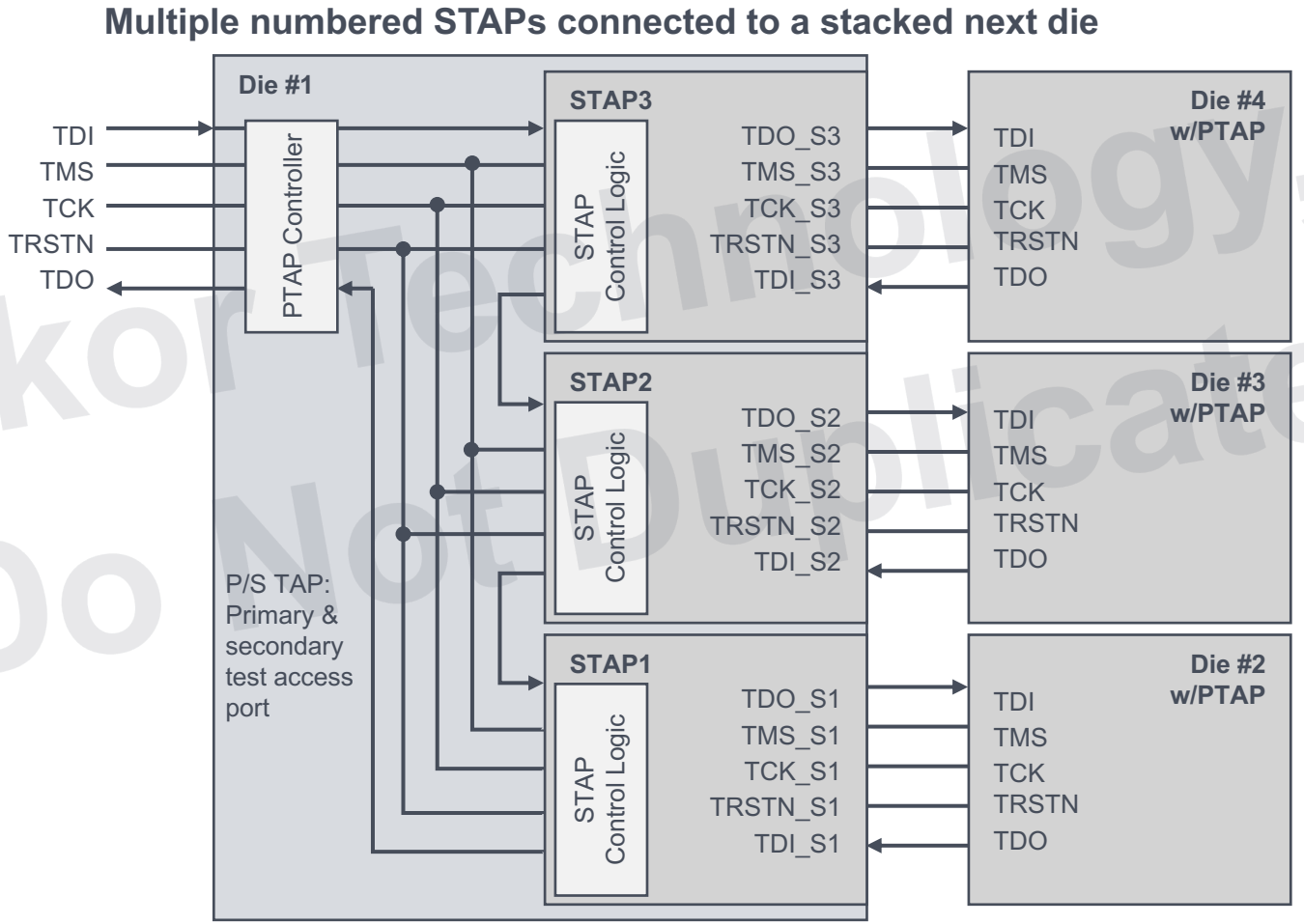
- A Pinned out
- B Not pinned out

Production Test Methodology – DFT

- Functional & structural test content
  - BIST, SBFT, scan – IEEE 1149.x, 1500, 1687, 1838
- Digital test instrumentation features
- Concurrent testing



High Density Digital Packages – TAPs

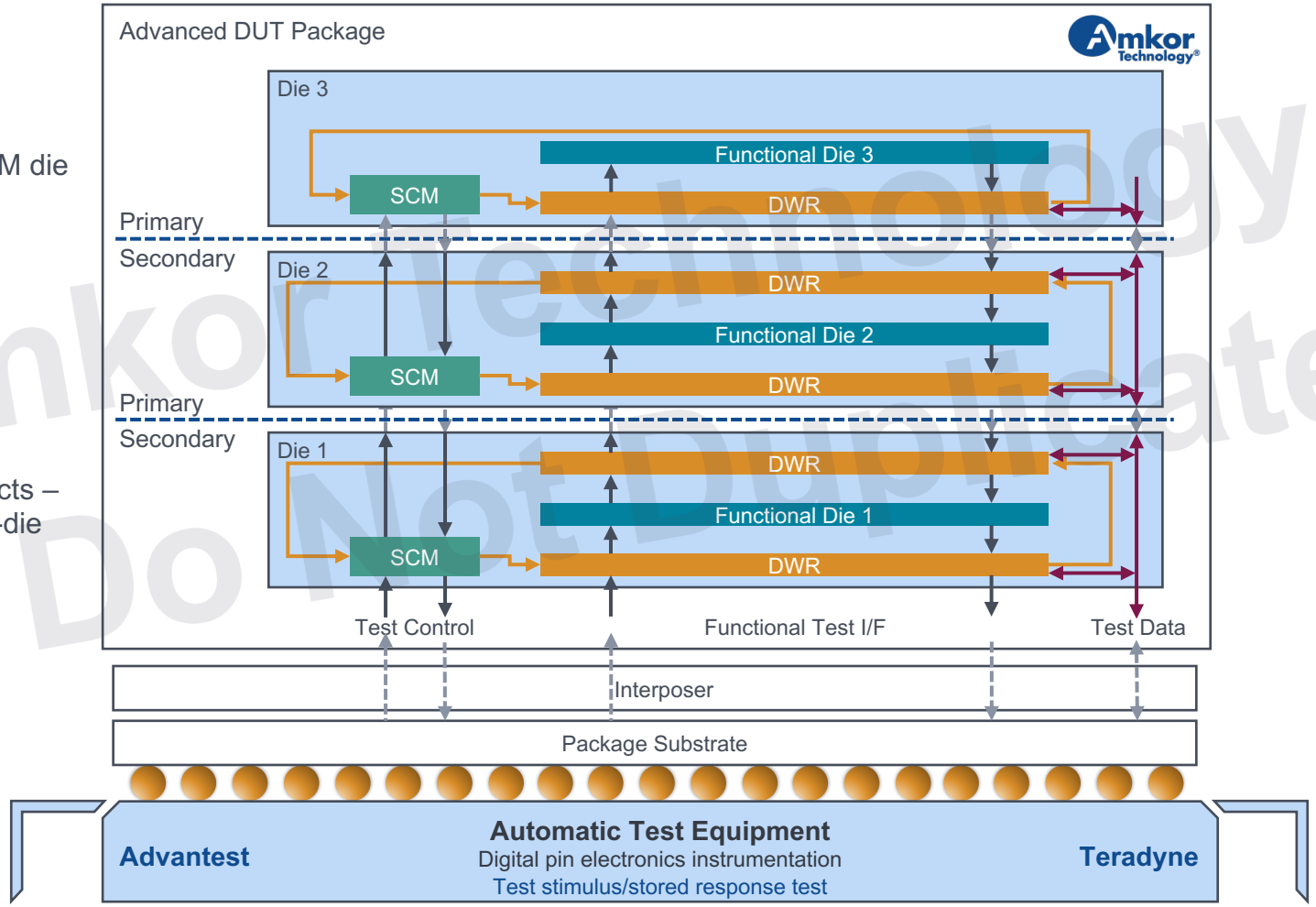


Source: "IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits," IEEE Std 1838-2019 , vol., no., pp.1-73, 13 March 2020, DOI: 10.1109/IEEESTD.2020.9036129.

3D IC Test View

CPU (logic), GPU, DDR/HBM die

Test challenge: Interconnects – substrate, interposer, die-to-die

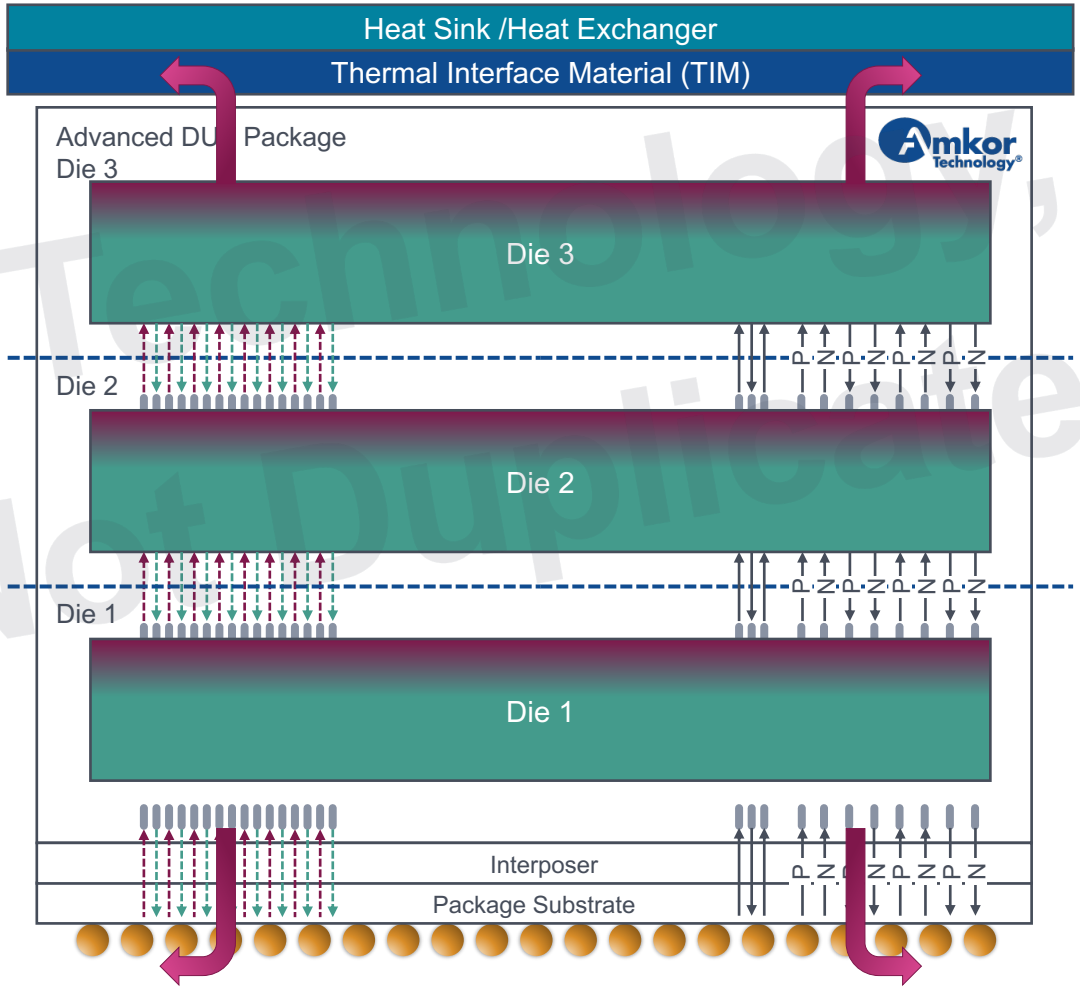


DWR: Die Wrapper Register
SCM: Serial Control Mechanism
FPP: Flexible Parallel Port

Source: IEEE1838-2019

3D IC Test Challenge

- Power
  - Cu pillar & µbump – contact resistance
- Signal
  - Capacitive loading for signal & ground
  - Crosstalk & increased noise in Si substrate
  - Insertion loss & return loss – via/bump interface
- Thermal
  - Interconnect/underfill layers
  - End-of-the-line layers
  - Bulk silicon
  - µbump
  - Heat sink



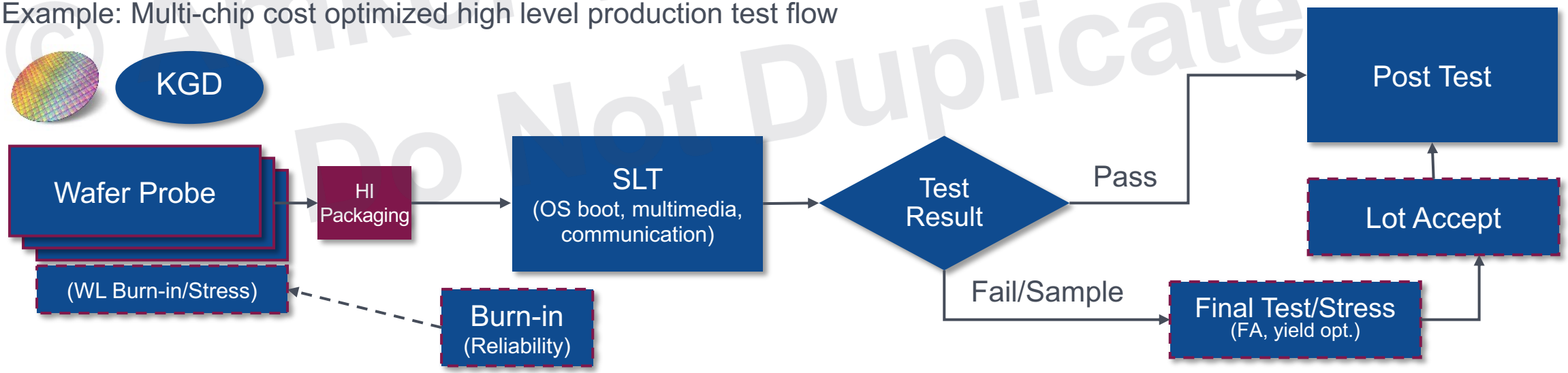
Call for Action

- Production test simplification
- Standardization
- Enable re-use

Production Test – Impact to Test Flow

Example: Single chip production test flow

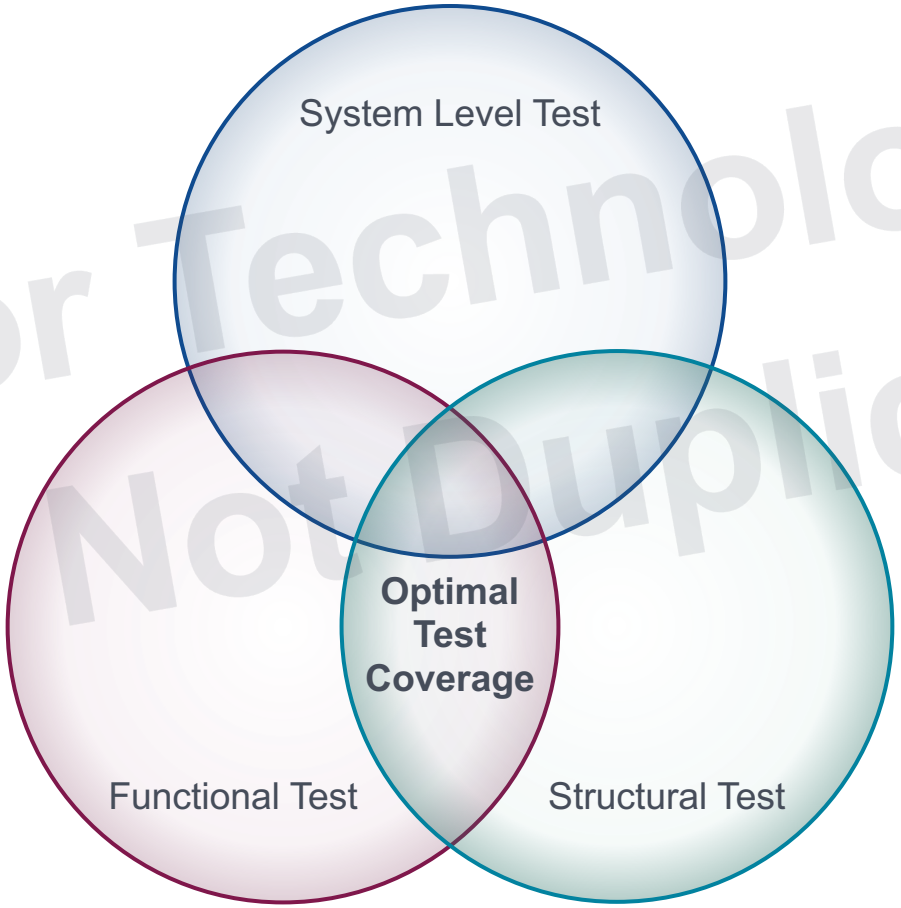
Example: Multi-chip cost optimized high level production test flow



Altered Test Flow **Test Content Re-distributed** **Platform Level Test Quality**

System Level Test

- High-speed serial interface, e.g., USB, PCIe, MIPI, UFS, Ethernet
- Test access port, serial, e.g., IEEE 1149.x, 1500, 1687, SPI/I²C…
- Contactless interface e.g., Wi-Fi, 5G NR RF, Zigbee…



DFx

- Manufacturing: Yield optimization, fault isolation
- Quality & reliability – burn-in, stress
- Thermal design
- Test: High-speed serial, 5G RF, analog, digital content generation

System Level Test Equipment

Tester

- Power, signal, clock, protocol
- SLT Requirements – eased by FPGA based instrumentation & popularity

Handler

- Package size range
- Massively parallel
- High UPH

Test Hardware

- Mimic end application
- Increased complexity
- Increased test coverage

TechWing

Hontech

Chroma

Advantest

Teradyne

Summary

- Multi die packages allow for denser integration
- Business continues to have economic and performance challenges
- Call to action – advanced test methods
- Amkor is the industry leader in advanced packaging and production test solutions

Amkor Test Services

24/7

Operation of fully networked test floors

>2300 TESTERS in 7 LOCATIONS

2000+ Amkor, 300+ consigned

TESTED ANNUALLY

>9 Billion units

>1.8 Million wafers

Test Development

Software & hardware for probe, strip, final and system level test

Testing For Commercial, Industrial & Automotive Devices

Discrete, power, mixed-signal, memory, RF, MEMS and SiP devices

ACCURATE AND THOROUGH TEST SERVICES

Wafer probe, final test, strip test, film frame test, system level test, opens/shorts test, burn-in and complete end-of-line

Full End-of-Line Processing

Bake, scan, pack, ship and finished good services

Thank You

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