

Road to Chiplets: Heterogeneous Integration Testability



March 15 & 16, 2022



The HI Product Testability BKM: A Practitioner's Guide to Testing Chiplets

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Agenda

- The Rise of Chiplets!
- Chiplet Testability Gaps
- What is the purpose of the BKM?
- What's inside the BKM?
- Key Findings
- Summary and Call to Action

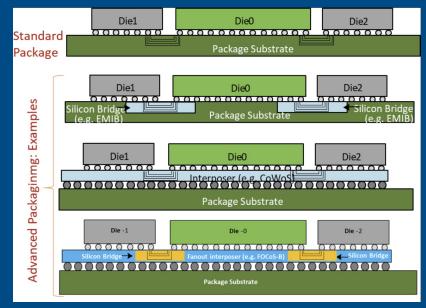


The Meteoric Rise of Chiplets!

 Industry adoption of Chiplets has accelerated much faster than anyone has anticipated, highlighting many critical testability gaps

Definition: a chiplet is a tiny IC that contains a well-defined subset of functionality. It is designed to be combined with other chiplets on an interposer in a single package. A set of chiplets can be implemented in a mix-andmatch "LEGO-like" assembly.

Ack: https://en.wikipedia.org/wiki/Chiplet

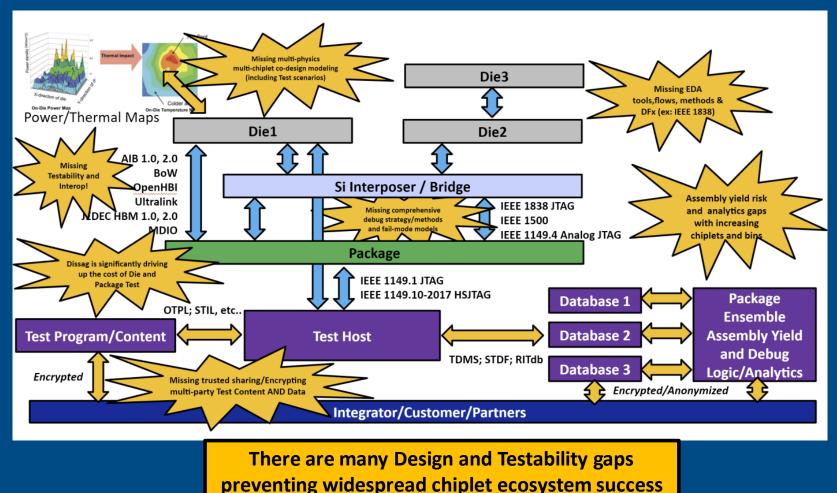


https://images.anandtech.com/doci/1728 8/UCle_Packaging.png



Chiplet Design and Testability Gaps

 Existing Standards and efforts have been significantly lacking from the product integrator perspective







Example Existing Chiplet Interface Standards

- Advanced Interface Bus (AIB) 1.0/2.0
 - https://chipsalliance.org/announcement/2020/07/16/aib-2-0-draft-specification/
- Bunch of Wires (BoW)
 - https://www.opencompute.org/wiki/Server/ODSA
- Universal Chiplet Interconnect Express (UCIe)
 - https://www.uciexpress.org/
- JEDEC HBM
 - https://www.jedec.org/standards-documents/docs/jesd235a

Lots of standards, but all fall far short on defining the minimum requirements for manufacturing and debug interoperable Testability



What is the HI Testability Best Known Methods (BKM)?

- Purpose is to consolidate the best techniques needed for successful Test deployment of 2.5D and 3D integrated products of today.
- This complements the IEEE EPS Heterogeneous Integrated Roadmap (HIR) content which is our longterm (5yr+) vision
- Authored and ratified by the IEEE EPS Test Technical Committee at the end of 2021.
 - Freely downloadable by anyone. Get your copy today!
- TC home: https://cmte.ieee.org/eps-test/
- BKM Document download: https://cmte.ieee.org/eps-test/wp-content/uploads/sites/132/2022/01/IEEE_EPS_Test_Het_Int_Product_Testability_BKM_Final_v1_0-1-14-22-1.pdf



Heterogeneous Integrated Product Testability Best-Known Methods (BKM)

Revision 1.0

Sponso

Test Technical Committee
of the
IEEE Electronics Packaging Society (EPS)

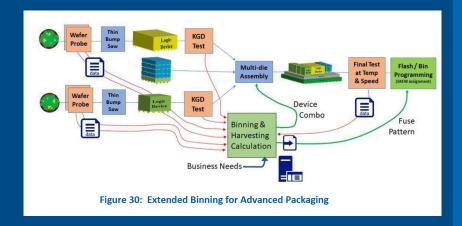
Approved 10 December 2021
IEEE EPS Test Technology Committee (TTC)

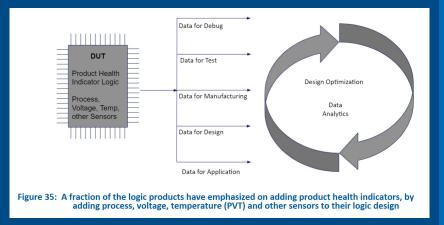




What's inside the HI Testability BKM?

- 76 pages; Chapters designed to be read out-of-order
- Themes and sections
 - Ecosystem and Test Economics Best Practices
 - Sameer Ruiwale to present later in this workshop
 - Die Probe strategies and Best Practices
 - Will Thompson to present later in this workshop
 - Interconnect BIST best practices, Redundancy, Repair and Rework
 - Sreejit presented on this in last year's Road To Chiplets Workshop: https://www.youtube.com/watch?v=6BiTiibfw1E
 - Debug and Fault Isolation Best Practices
 - Terrence Tan presented in last year's Road to Chiplets Workshop: https://www.youtube.com/watch?v=VfEmAlegJjQ
 - The changing nature of ATE and Content Delivery Best Practices
 - Database and Data Sharing Best Practices
 - HI Product Deployment Checklist
 - Chiplet Integration Case Studies from the Industry
 - What's worked well, but also cautionary tales!











Key Finding: There is a Fundamental Need for Multisupplier chiplet Test *Interoperability*

- Harmonized EDA Tools, methods and flows
- Harmonized minimum-viable DFt, Test and full-assembly Debug strategies
- Advanced probe technologies for KGD Testing of die and die-stack testing
- Portable test content and secure supply chain data sharing and package assembly analytics



Summary and Call to Action

- The HI Testability BKM is a tool to help the chiplet ecosystem navigate a fragmented design and integration space so that they will be successful at manufacturing a product with chiplets at-scale
 - But our Testability BKM alone is insufficient!

- As an industry, we must decide now where and how we must cooperate so we can all successfully compete in a rapidly-growing chiplet marketplace
 - Please participate in tomorrow's MEPTEC Workshop Panel Discussion on this exciting topic and make your voice heard!

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