Road to Chiplets: Heterogeneous Integration Testability

March 15 & 16, 2022

MEPTEC
THE NEXT GENERATION

www.meptec.org

ADVANTEST

The Changing Nature of Protocol based Testing

Bob Bartlett, Advantest

Agenda

- Introduction
- Test Data Volume
- Protocols
- Protocols used in Semiconductor Test
- JTAG/1149.1
- Evolution of Multi-Chip Integration Technology
- Heterogeneous Integration
- Paradigm Shifts in ATE
- New Test Requirements Drive New Methodologies
- AI/PSV
- Summary

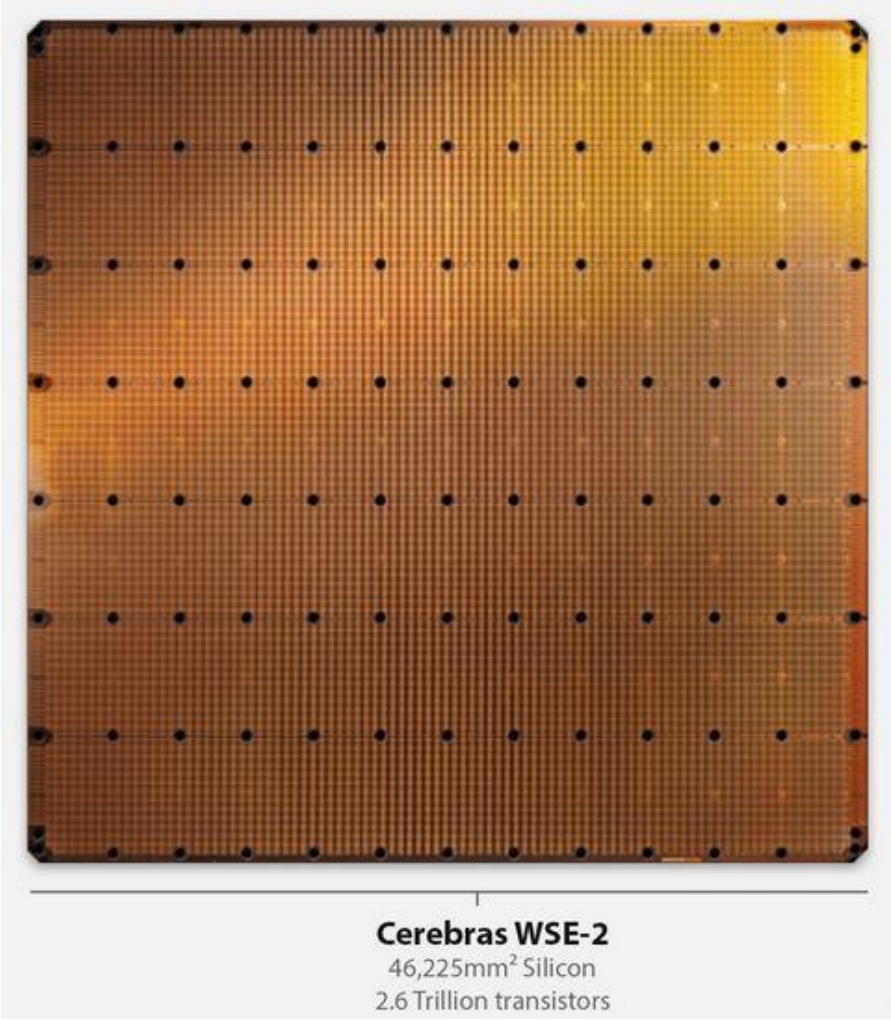
Test Data Volume

Semiconductor production facilities made 250 billion billion (250 x 10^{18}) transistors in 2015 – Dan Hutcheson, CEO, VLSI Research, April 2015
For the CY2021 approximately 1.6x10^{21} transistors were produced.

How much data does test generate?

Assuming only 80% of the transistors are tested and each transistor results in just one bit of data, that is >40 Tb per second in 2021..

Largest GPU
826mm² Silicon
54.2 Billion transistors



Cerebras WSE-2
46,225mm² Silicon
2.6 Trillion transistors

Protocols

Definition

- **Protocol:** Set of conventions governing the treatment and especially the formatting of data in an electronic communications system - “Protocol.” *Merriam-Webster.com Dictionary*, Merriam-Webster
- **Communication Protocol:** A set of rules and regulations that allow two electronic devices to connect to exchange the data with one and another
- **JTAG:** a serial communication protocol and a state machine accessible via a Test Access Port(TAP)

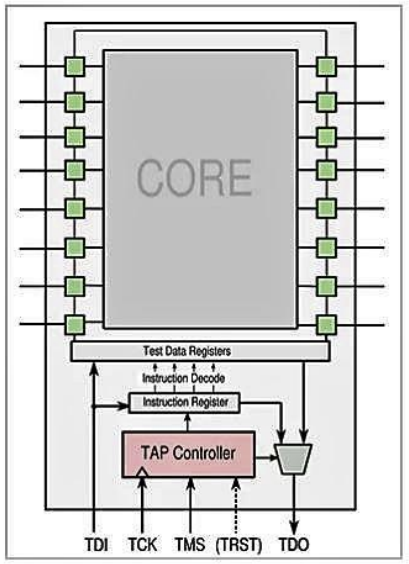
Protocols used in Semiconductor Test

• UART	1971	2-wire	9,600-1.492Kbps
• SPI	1980	4-wire	1-10Mbps
• I2C	1982	2-wire	100K-3.4Mbps
• CAN	1986	2-wire	125K-5Mbps
• JTAG	1990	5-wire	1-25Mbps
• SMB	1995	2-wire	10-100Kbps
• MDIO	1999	2-wire	100K-2.5Mbps
• SWD	2003	2-wire	1K-32Mbps
• USB3.1	2013	2-wire	10Gbps
• PCIe4	2017	4-wire	16Gbps

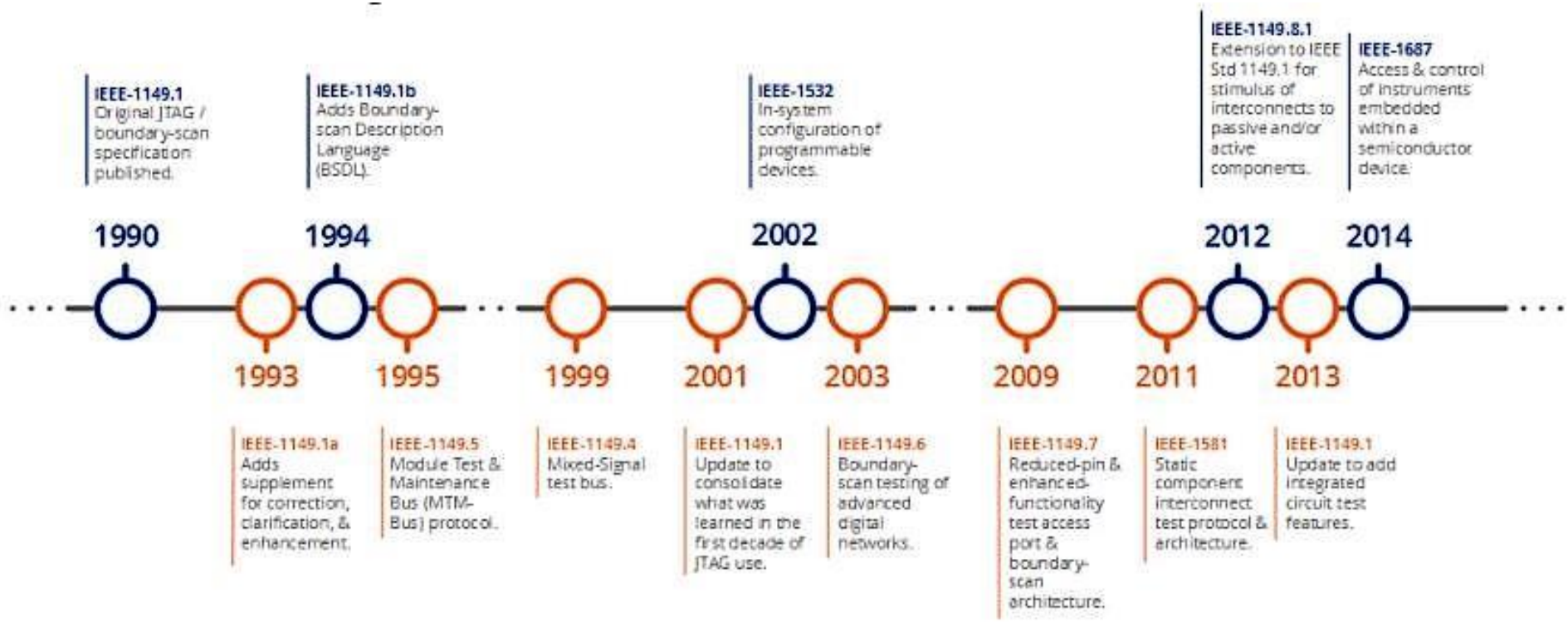
JTAG/1149.1

Joint Test Action Group - IEEE 1149.0/.1 (1990)

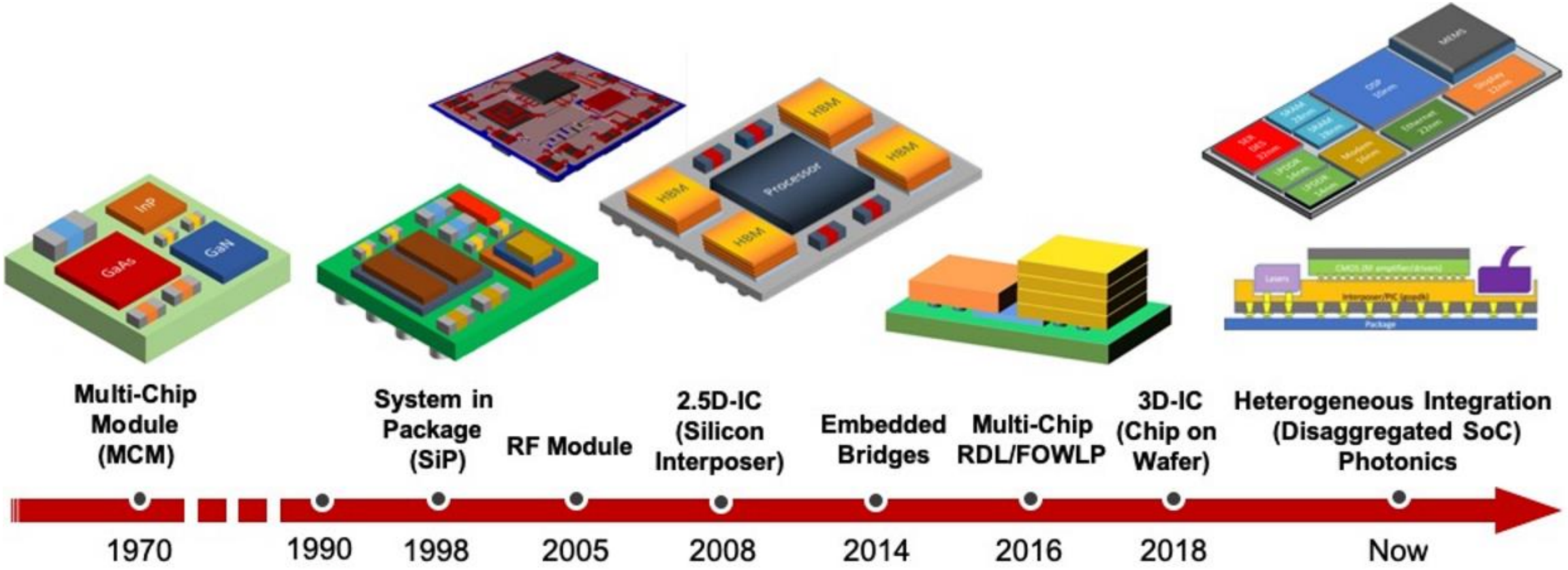
- **Define a standard of test logic architecture**
  - Board connectivity test - check for assembly fails
  - Interconnect test
  - Scan chain integrity testing
  - Configuration of functional registers for test modes
  - Configuration of DFT/Structural testing: BS, Scan, BIST, Calibration, Trim
  - DFT execution
  - Device trim mode
  - Flash BIOS & embedded Memories



JTAG and Beyond



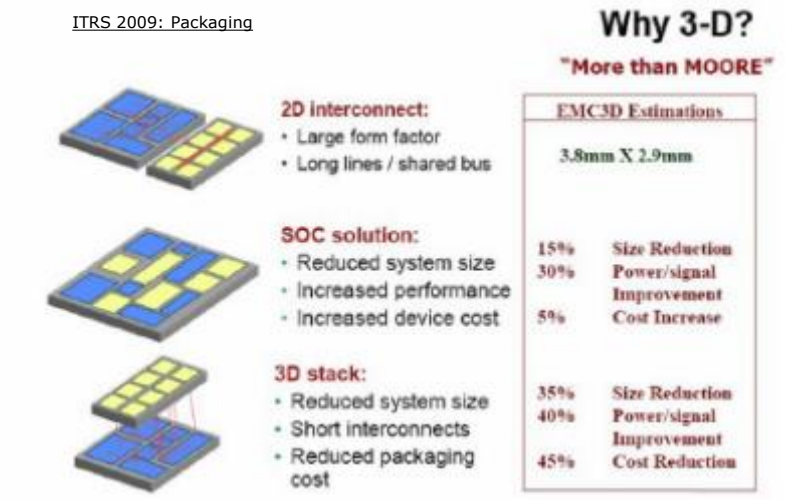
Evolution of Multi-Chip Integration Technology

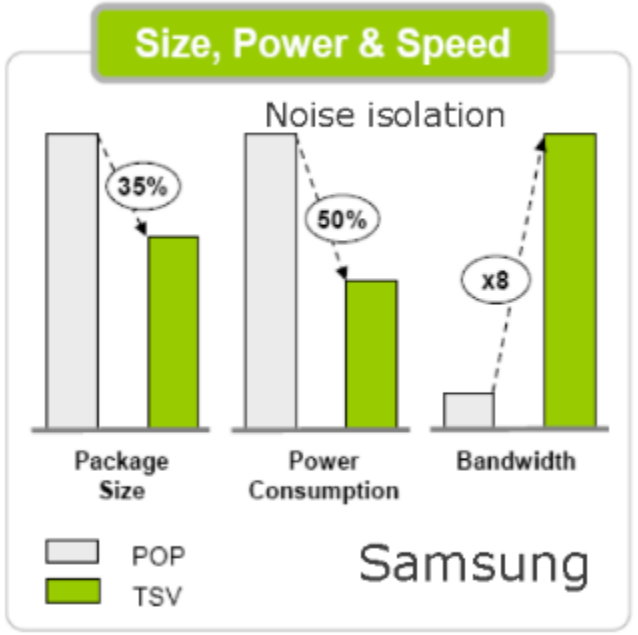


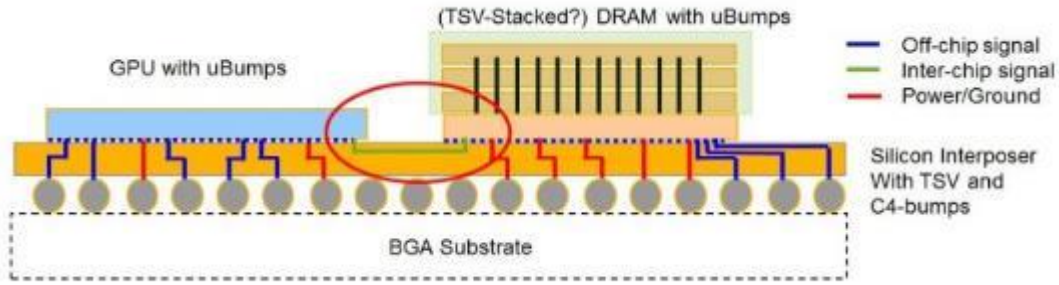
Source: Cadence

- Multi-Chip integration technology has more than 30 years of history.
- **What test challenges will the new era of multi-chip integration bring?**

Heterogeneous Integration: 2.5 & 3D ICs

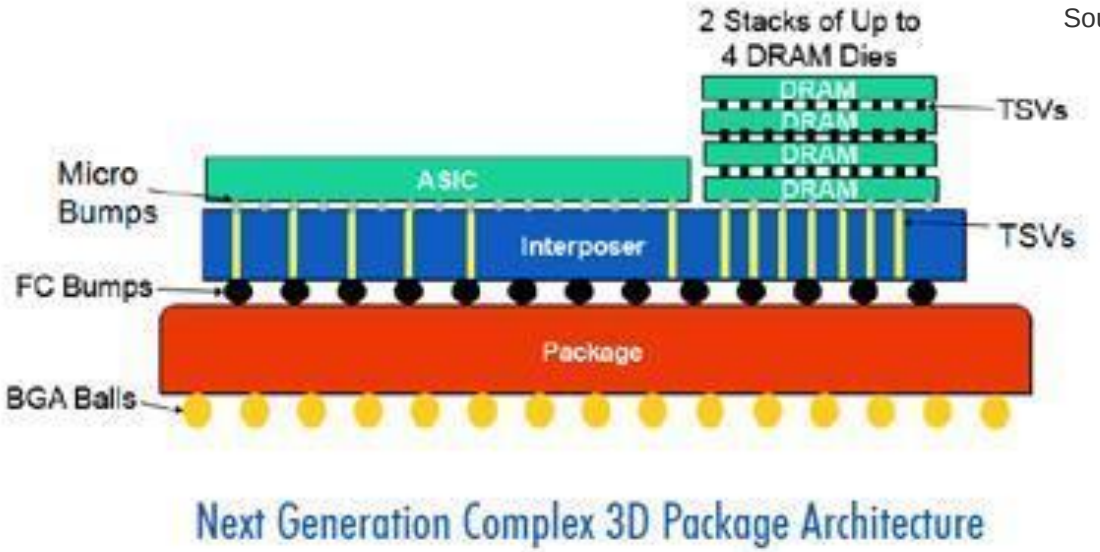






9

Test Implications



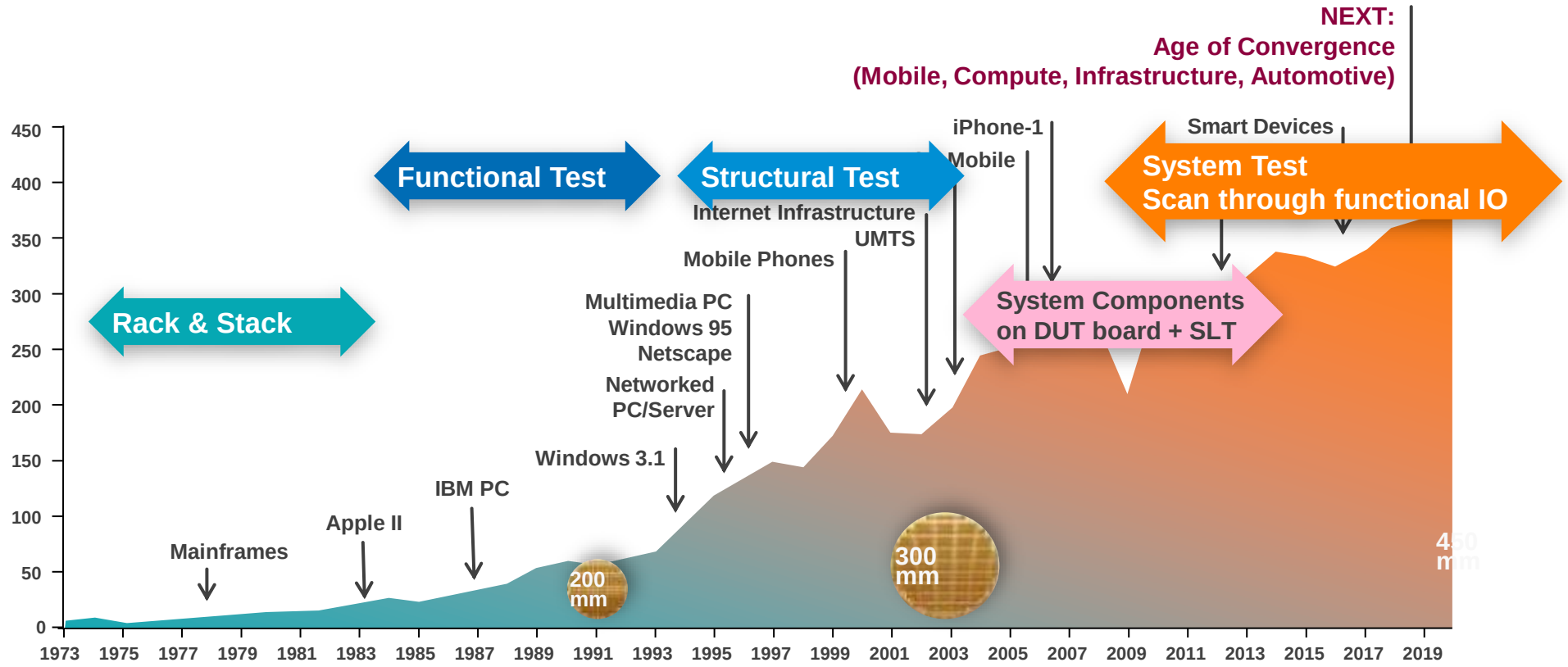
Next Generation Complex 3D Package Architecture

Source:
TSV Stacked BGA,
Amkor Technologies, Inc

- Limited test access from outside
  - IEEE / JEDEC test access ports
- Test of partially assembled system
  - New test insertion points in manufacturing flow
- Issues
  - Multiple device suppliers – how to ensure test coverage for DPPM
  - Test access ports allow identification and debugging of problems, but cannot prevent scrapping of system – yield issue
  - Yield of a combined device is the product of the component yields

    YTotal = YPart1 * YPart2 * YPart3 * … * Ypackage

Paradigm Shifts in ATE



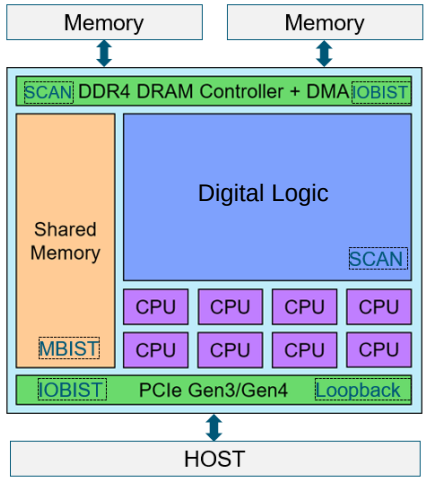
Chiplet Test and Data Impacts

Many aspects of test and data influenced by chiplet-based products

- **Larger systems within a package scale the amount of test data up dramatically**
  - HPC and HIR devices need larger scan and complex workloads for execution on devices
- **Known Good Die (KGD) ensure that each chiplet is extensively tested, binned and matched before integration**
- **Software Defined Functional test content and system level test increasing**
  - Electrical failure analysis is more complex and data-intensive
- **Need to migrate more test content earlier in the flow**
  - Detect defective units earlier prior to integration, decrease end of line yield loss
  - Requires more correlation work to identify tests at wafer that detect downstream system level failures
- **Die traceability**
  - Debug, root cause analysis, and die matching
  - KDG and low DPPM require more management, data collection and tracking from origin of each chiplet

New Test Requirements Drive New Methodologies

High integration multi-core architecture

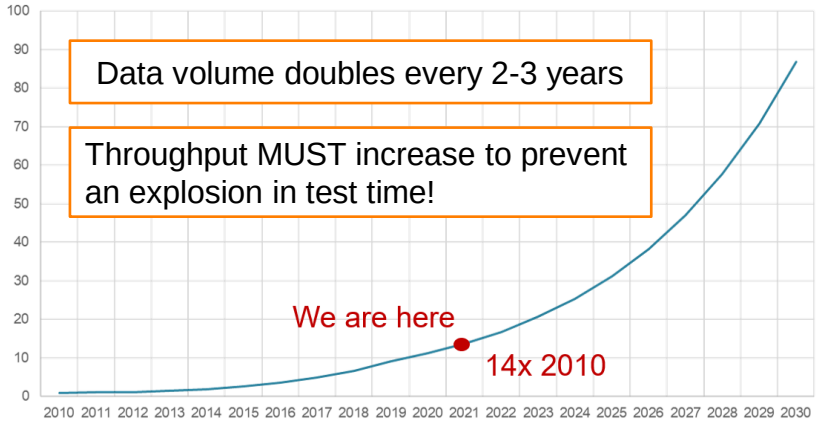


Good individual core coverage: SCAN, BIST,..

Complex functional test cases across cores

SLT like Host interaction

ITRS SCAN pattern volume projection



Software-based functional test

Device boots firmware through USB or PCIe
Supporting application software runs on the card
=> Close functional test coverage gap on ATE

Correlation and test content exchange with SLT

Use similar test content on ATE and SLT
Enable correlation and test content re-use
=> Support industry trend for higher quality wafer test

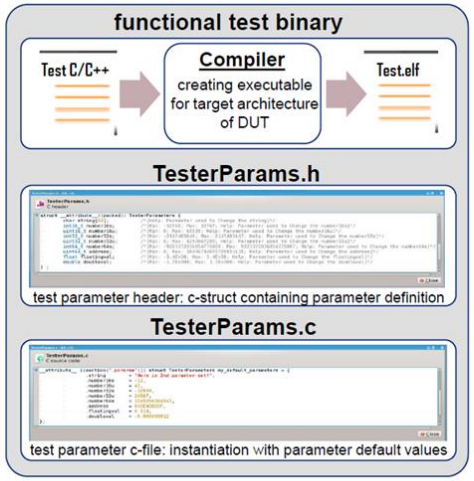
SCAN through functional HSIO

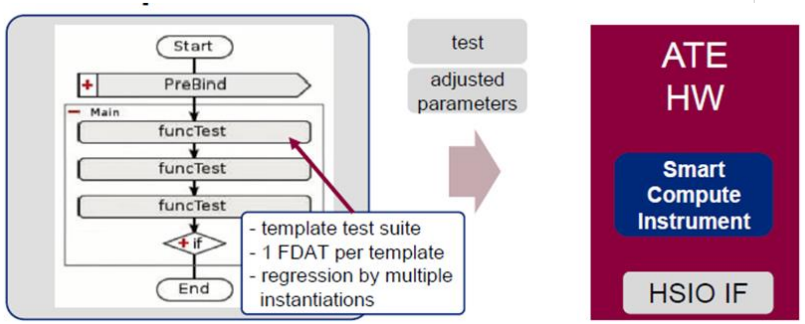
High speed SCAN data transfer through USB or PCIe
Supporting result processing software runs on the card
=> Keep test time under control with HSIO SCAN

Chiplet DPPM

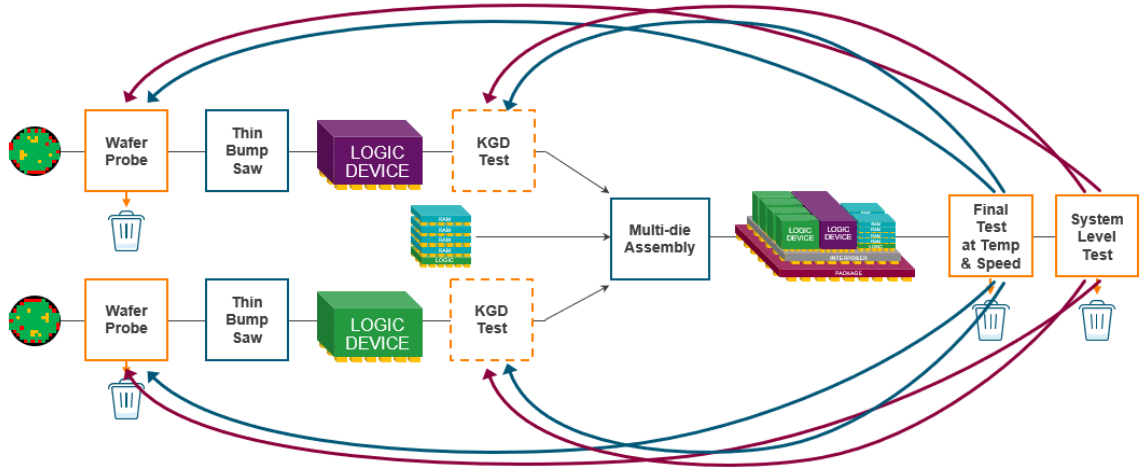
Assumption:
- 13 Chiplets in one package, 1@100dppm, 12@50dppm plus stacked SRAM 12x30dppm
- This results in 100+12x(50+30) = 1060dppm
  → **How to provide "better" KGD quality with lower DPPM?**

How to improve individual chiplet & overall package coverage:
- **Better and more scan types**
- **Functional tests**
- **Additional Insertions**
- SLT





More Functional, Less SLT possible?

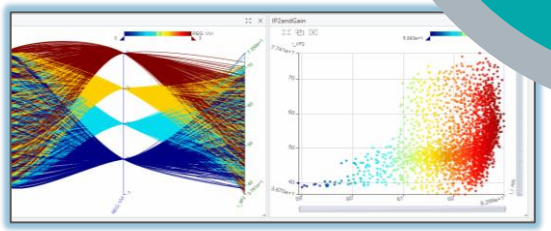


Challenge:
- SLT content is growing
- SLT content is always added, but no measure if still required and/or how to fix (How to back map to design, process, SW..)
- How to bring efficiently test content from SLT to ATE

Potential Strategy:
- Reduce DPPM to range of 100s
- Use advanced scan methodologies and add software defined functional test
- Make SLT an optional step; move test content to ATE insertions

AI-based PSV Manages Complexities of Post Silicon Validation

For RF / mixed-signal / HSIO / PLL, system-level digital, ...



TTM

- Automate tedious tasks
- Faster insight / debug
- Efficient communication

Quality

- Comprehensive, quantified coverage

Yield

- AI-based tuning improves yield or performance / power consumption

Integrated workflow automation based on data-driven, AI-powered PSV methodology

Multi-Chip Integration Testing for HIR

Heterogeneous multi-chip packaging is a technology in HVM that introduces many new test challenges.

- More test content and HSIO phy testing at probe, package and KGD
  - Protocol usage increases with SmartCompute test instruments
- High power and multi-power domains require PDN design for ATE supplies on critical device power rails
- HSIO DFT support needed for test access over multiple die packages
  - Increasing scan vector data and higher speed behind HSIO pins
- Variety of test functions are needed on a tester
  - Power profiling, DUT firmware, training, calibration and multi-step trim
- Low overhead high volume data collection
  - Edge Machine Learning(ML) for die-matching, extended binning, real-time analytics
- Accurate thermal control required for high quality stable testing
  - Die Level Thermal Control, ATC, Pre-trigger, Fluid cool socket or chuck

Thank You - Questions?

Contact: bob.bartlett@advantest.com

- **Acknowledgements:**
  - Dave Armstrong, Advantest
  - Ken Butler, Advantest
  - Zoe Conroy, Cisco
  - Abram Detofsky, Intel
  - Martin Dresler, Advantest
  - Rich Lathrop, Advantest
  - Keith Schaub, Advantest
  - IEEE-EPS
  - VLSI Research

COPYRIGHT NOTICE

www.meptec.org

MEPTEC
THE NEXT GENERATION