Road to Chiplets: Design Integration

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SUBSTRATE DESIGN OPTIMIZATION FOR CHIPLET ARCHITECTURE

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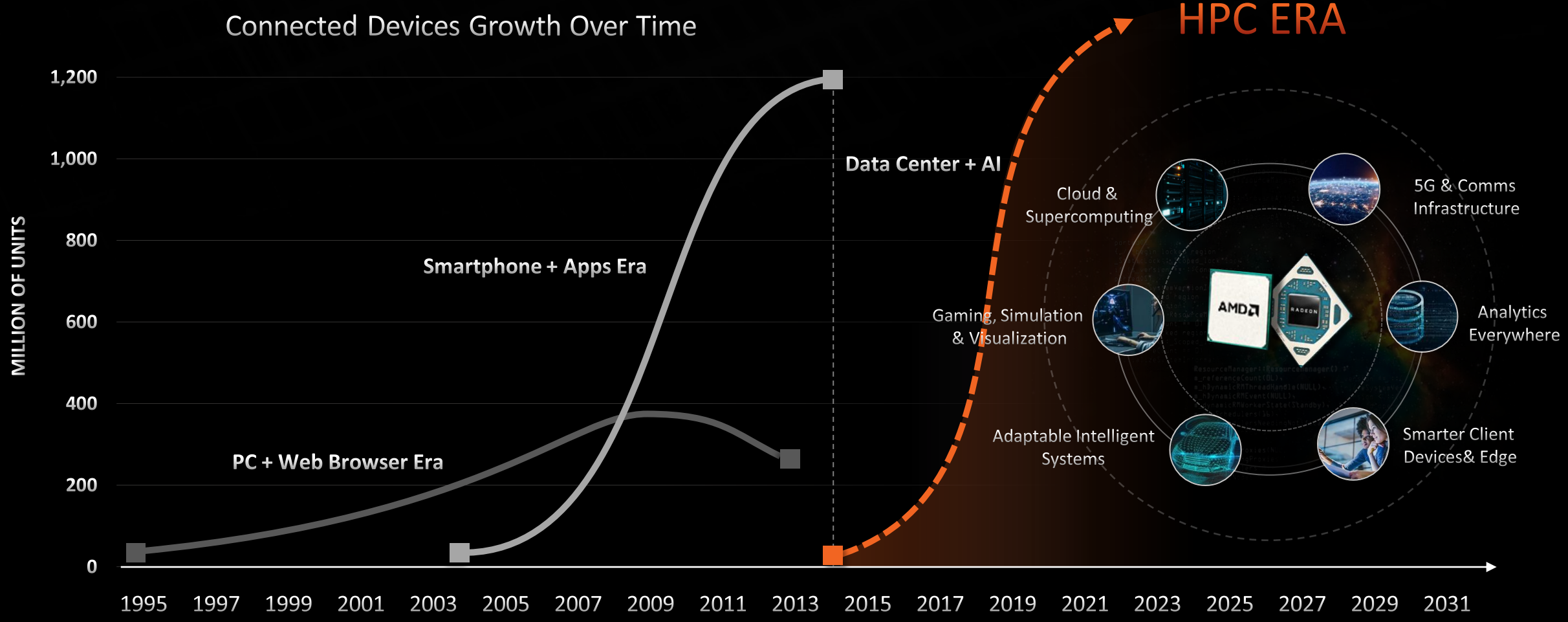
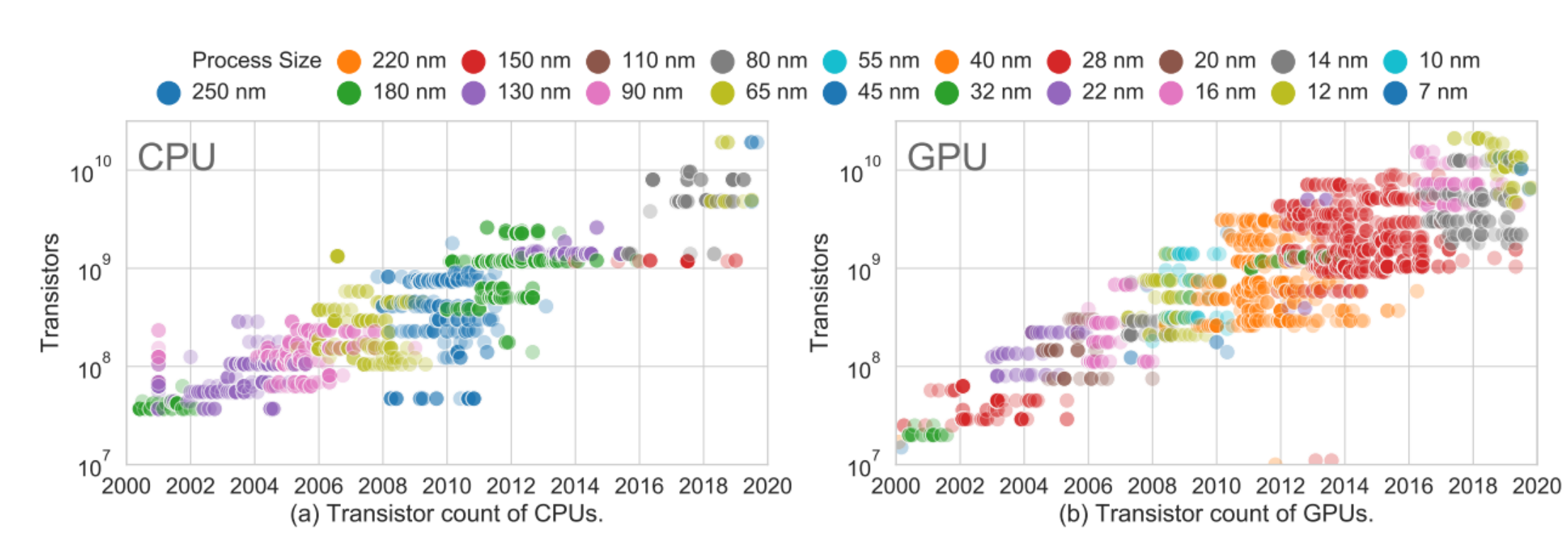
EXPLOSION OF CONNECTED DEVICES



GROWING COMPLEXITY OF CPU & GPU



Courtesy: Yifan Sun, et.al., 2019, Summarizing CPU & GPU design trends with Product data, ArXiv

CPU & GPU transistor counts continue to grow at exponential rates

In many cases high-end devices exceeding silicon reticle limits

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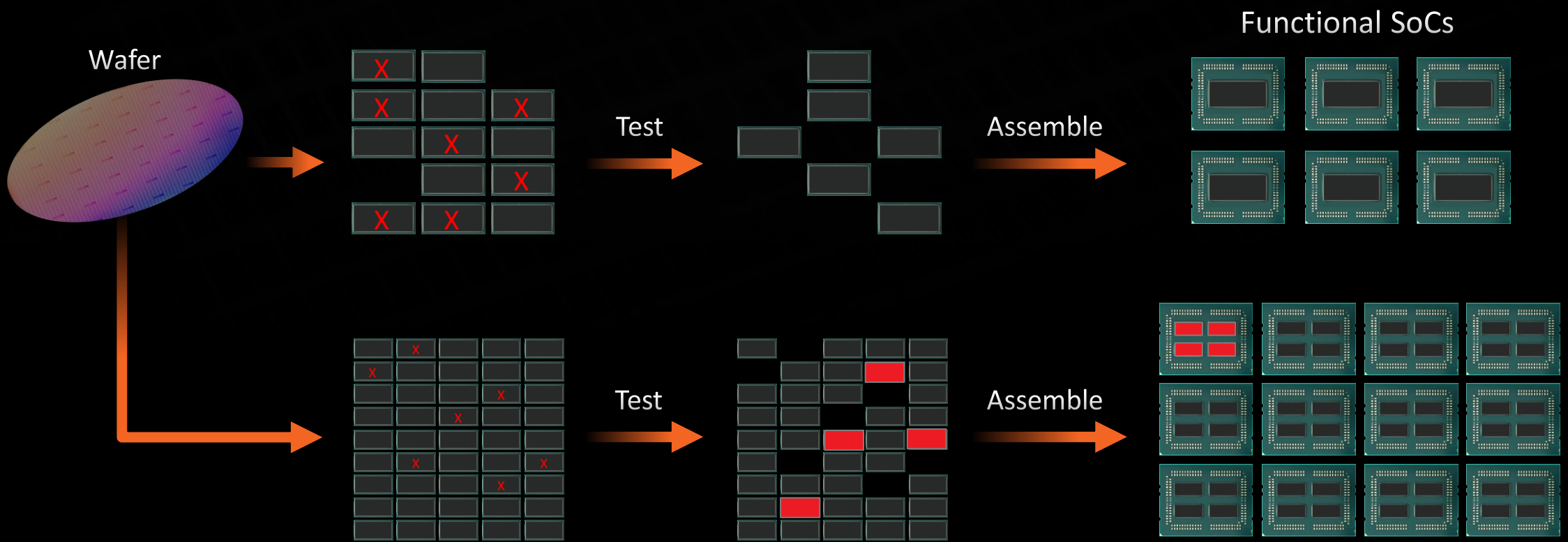
HIGH-LEVEL APPROACH TO CHIPLETS



Many More Functional SoCs

Ability to mix and match at a finer grained level

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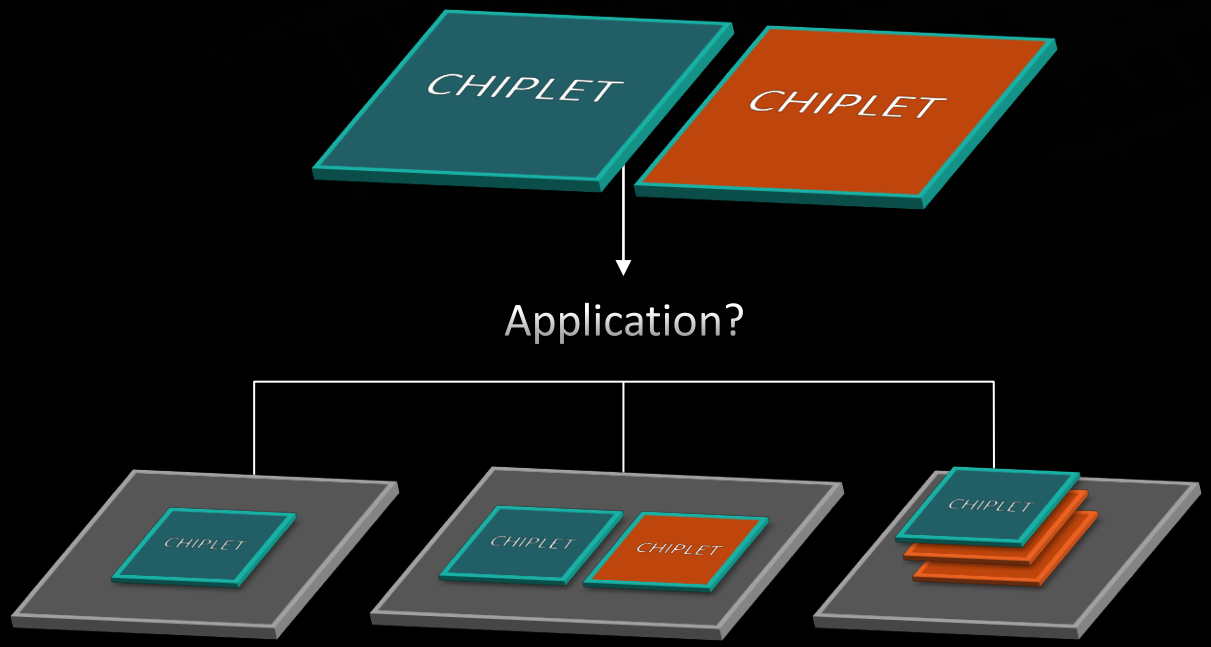
MODULAR ARCHITECTURE GOALS

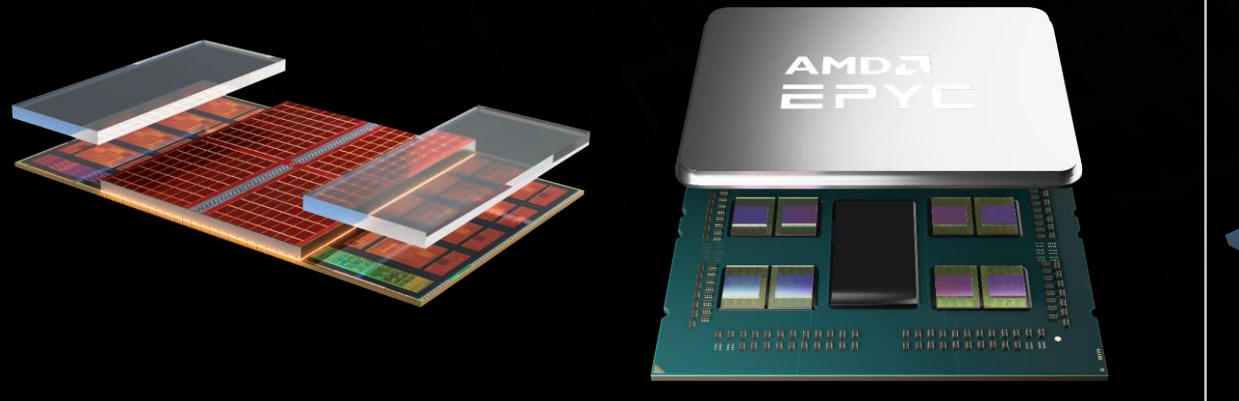
ENABLING A MORE FLEXIBLE APPROACH



- We want to build tailored products for specific markets by mixing and matching chiplet types
- We can now specialize a domain specific chiplet and include more or fewer of them for a given product
- More domain-specific products at higher yields … provided we can build low-overhead chiplets

ROLE OF SUBSTRATES

INCREASED INTEGRATION ON PACKAGE



3RD GEN AMD EPYC™ CPU
WITH AMD 3D V-CACHE

AMD INSTINCT™
MI200 SERIES WITH AMD 2.5D EFB

- More complex substrates with higher body size, layer count
- Increased power delivery demand
- Increased data rates driving novel HSIO solutions

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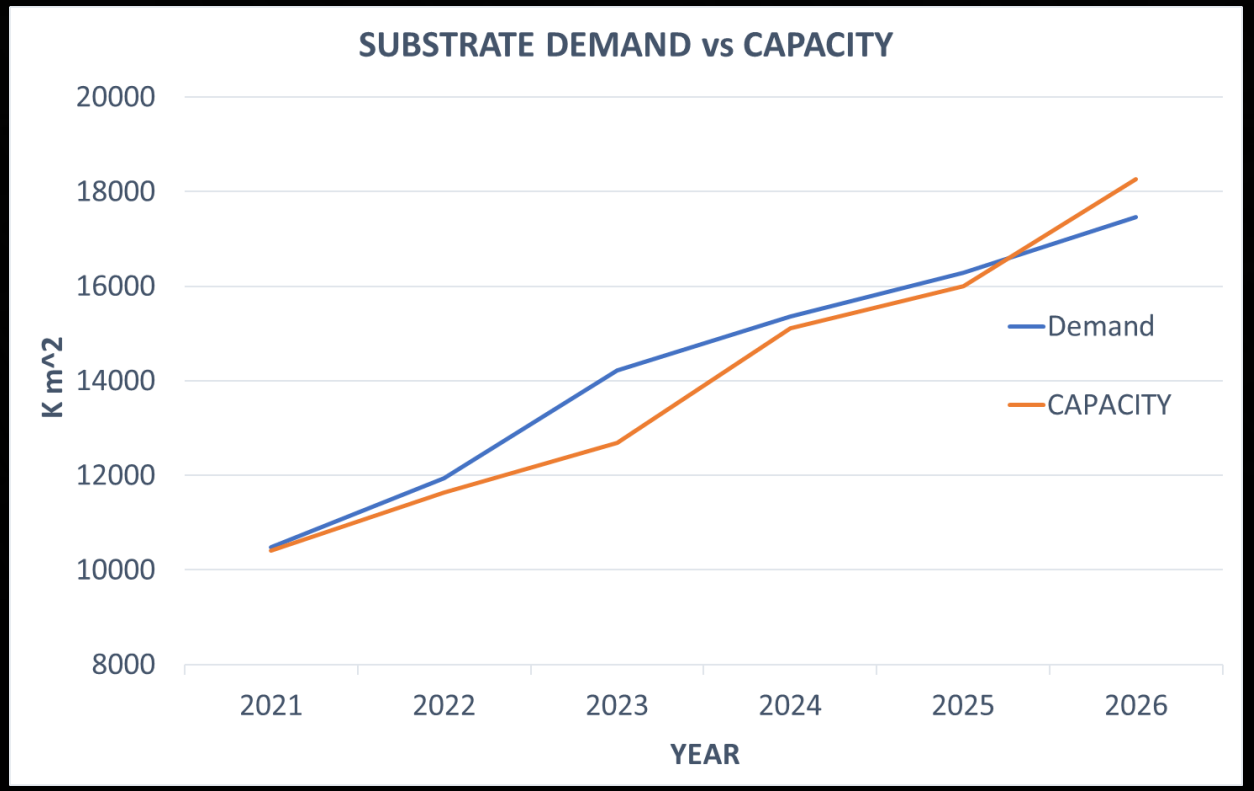
SUBSTRATE CAPACITY CHALLENGES



Courtesy: TechSearch

CPU, GPU packages continue to grow in complexity

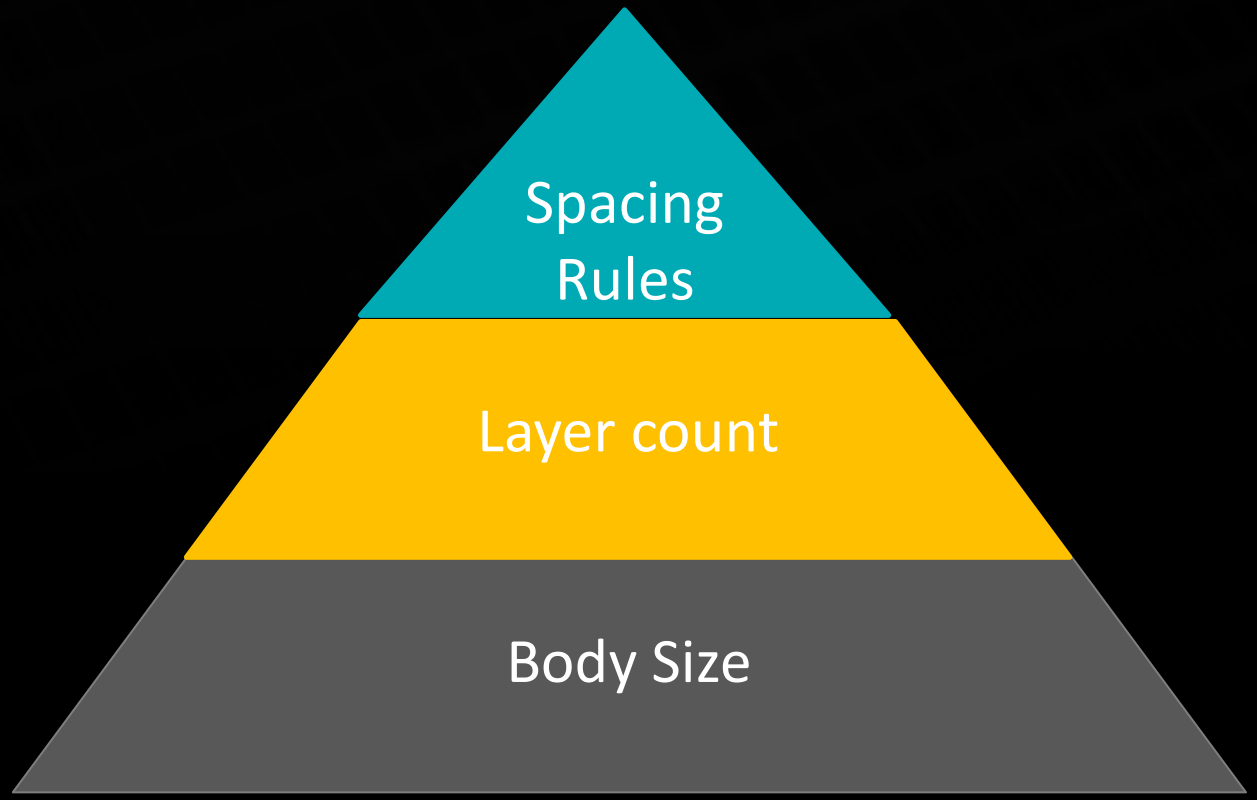
Demand for substrates continues to outstrip supply till 2026

SUBSTRATE DESIGN OPTIMIZATION

Co-optimization with silicon floor plan

PD/SI routing requirements

Top & Bottom side fit study
Board requirements



Maximize spacing DFY

Optimize layer count and routing density DFM

Minimize body size to improve panel utilization

Design for Manufacturing & Design for Yield need to be initiated from concept phase to enable co-optimization of product design

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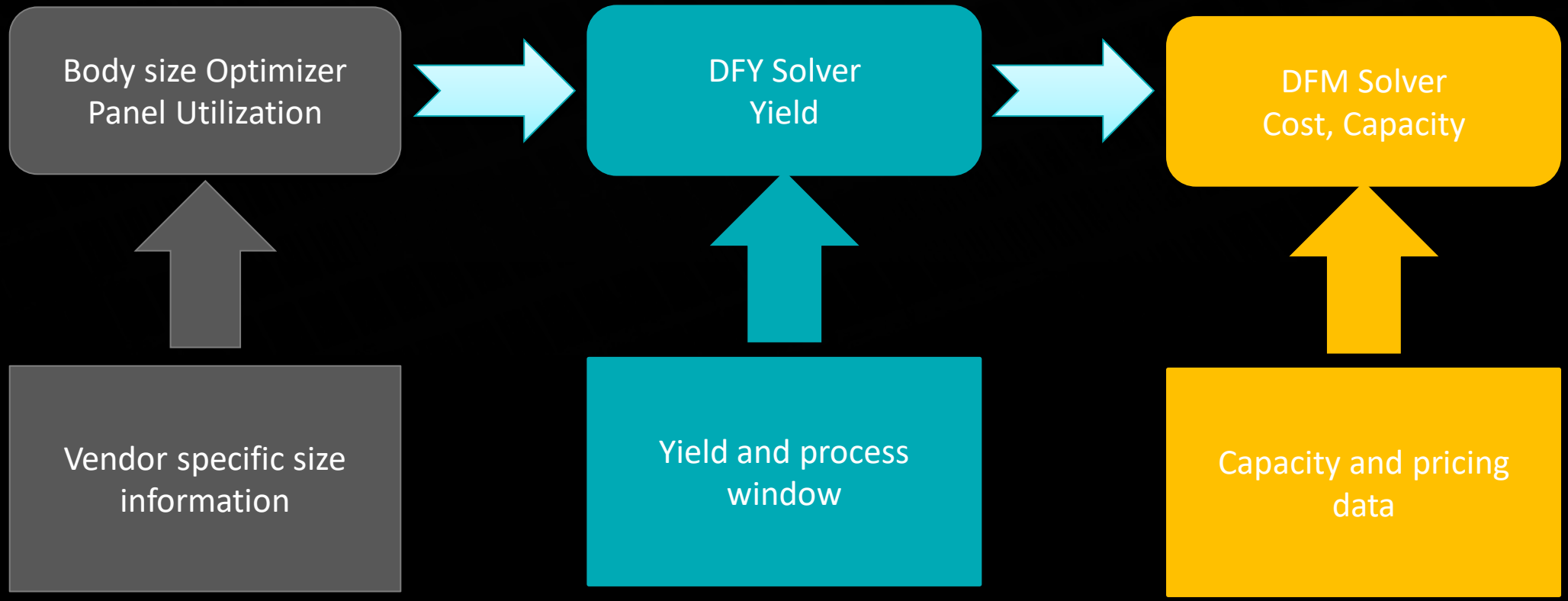
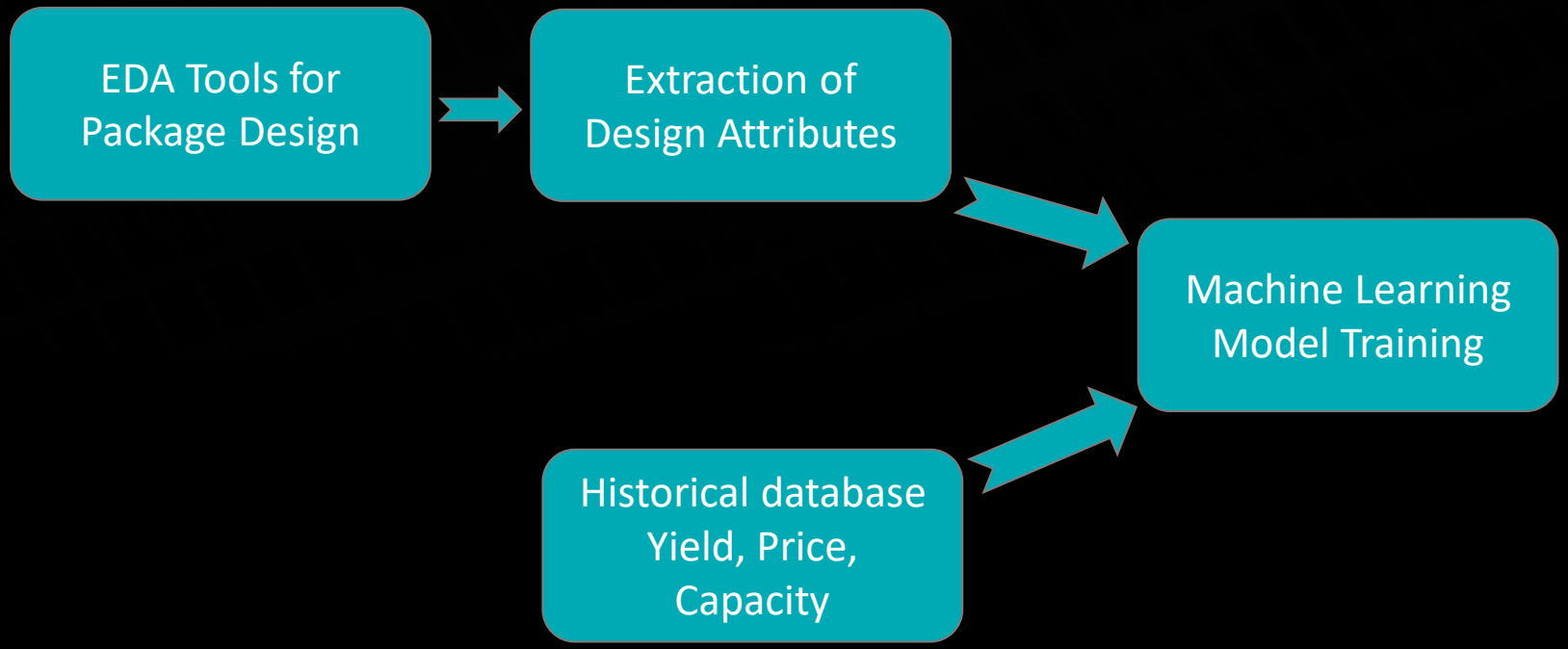
END-TO-END ANALYTICS



End-to-end analytics tools developed to ‘learn’ from historical data and provide quantifiable metrics for co-optimization

DFM/DFY: MACHINE LEARNING APPROACH

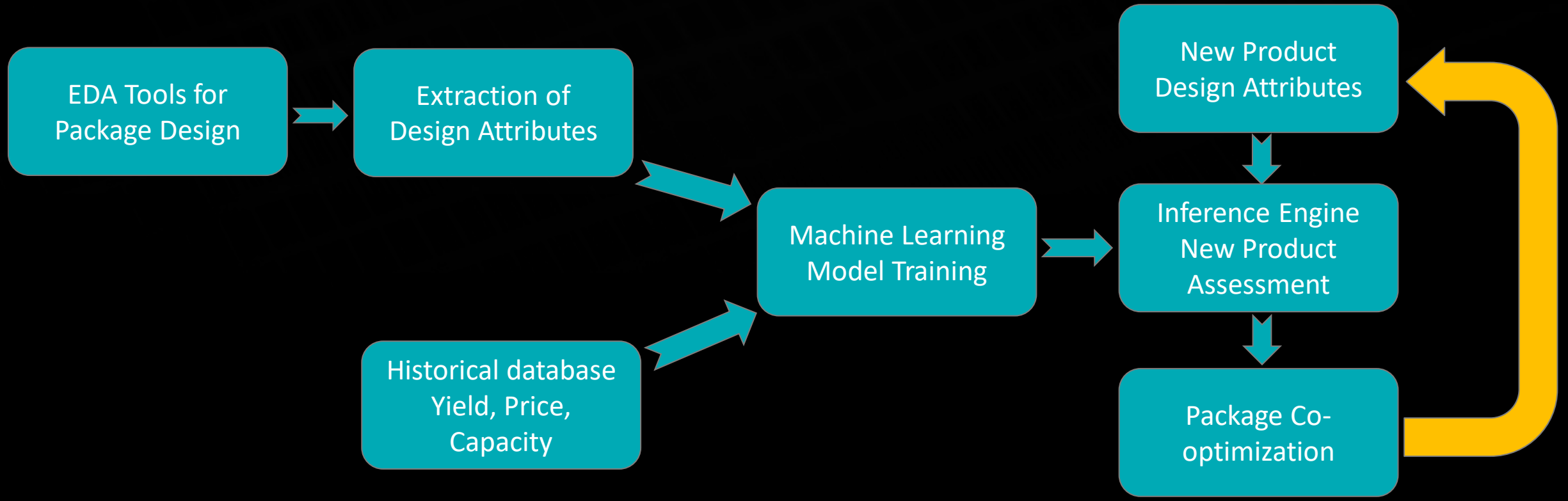
TRAINING METHODOLOGY



Model trained based on historical database of design, yield, cost, and capacity

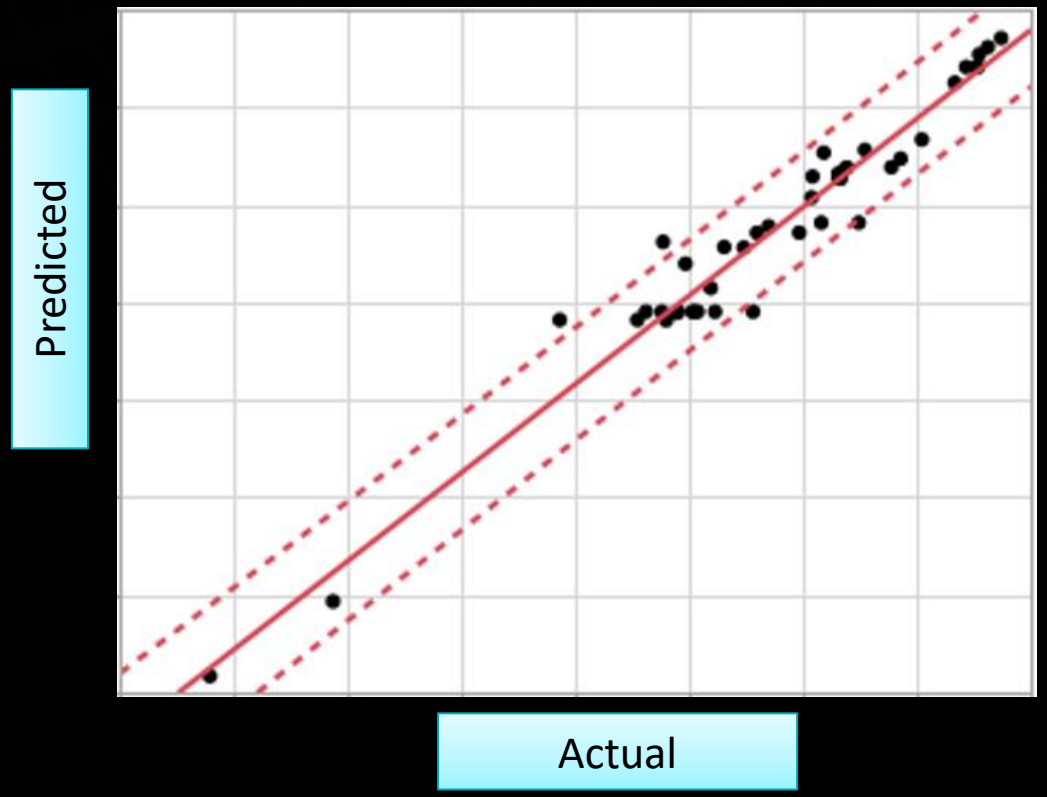
DFM/DFY: MACHINE LEARNING APPROACH

CONTINUOUS LEARNING & OPTIMIZATION



Methodology provides framework for continuous learning and optimization

DFY/DFY: MACHINE LEARNING RESULTS



Machine learning model shows good correlations to actual data

BENEFITS OF DFM/DFY OPTIMIZATION

10% to 30% CAPACITY IMPROVEMENT

Significant improvement in capacity through design optimization

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ROAD AHEAD

- 2.5D & 3D packaging continues to blur the boundaries between silicon and package
- Design co-optimization needed to balance performance, cost and capacity
- Increasing design complexity expected to drive adoption of machine learning tools
- Opportunity for designers, EDA tool vendors, manufacturing firms to collaborate

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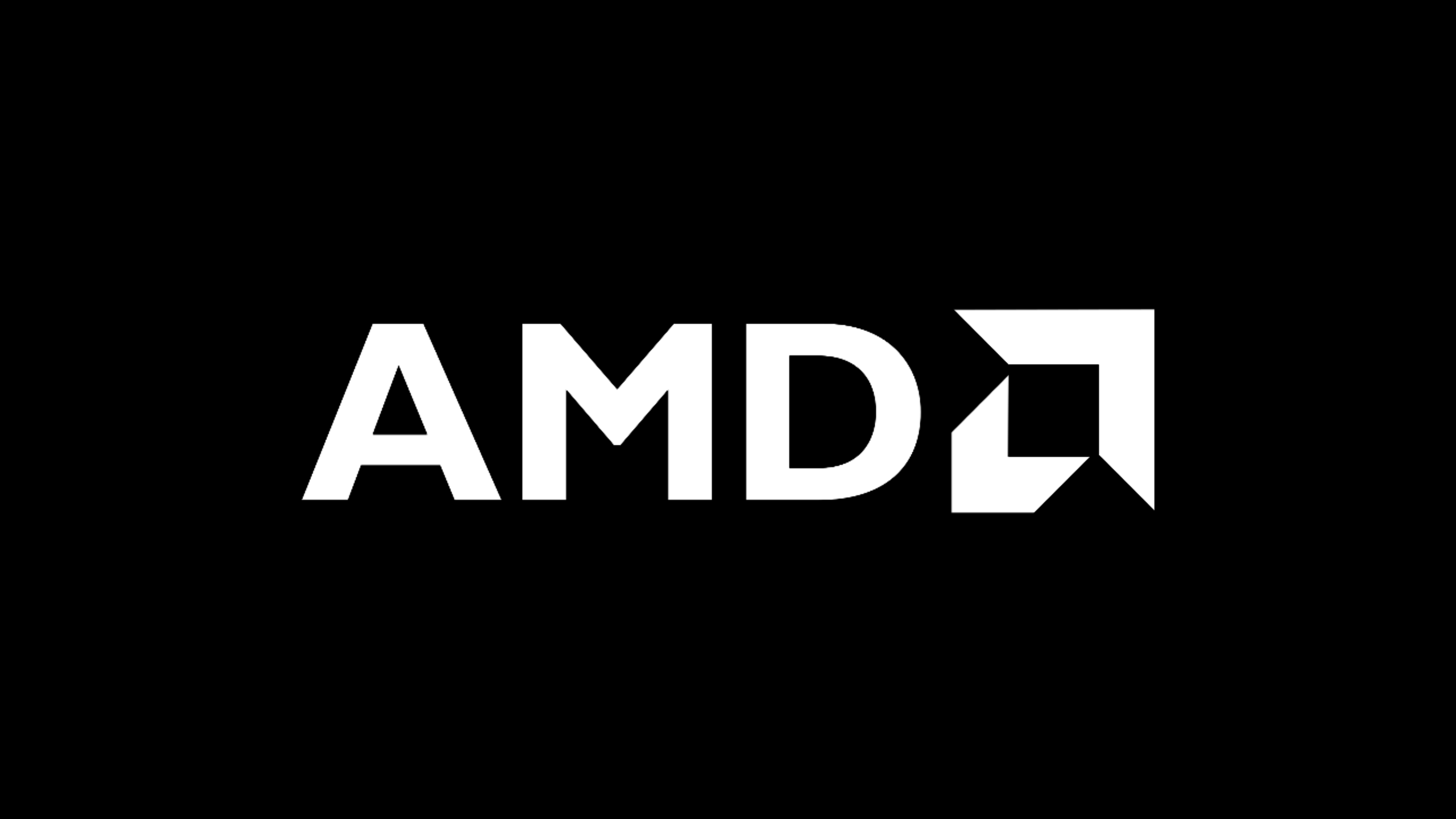
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