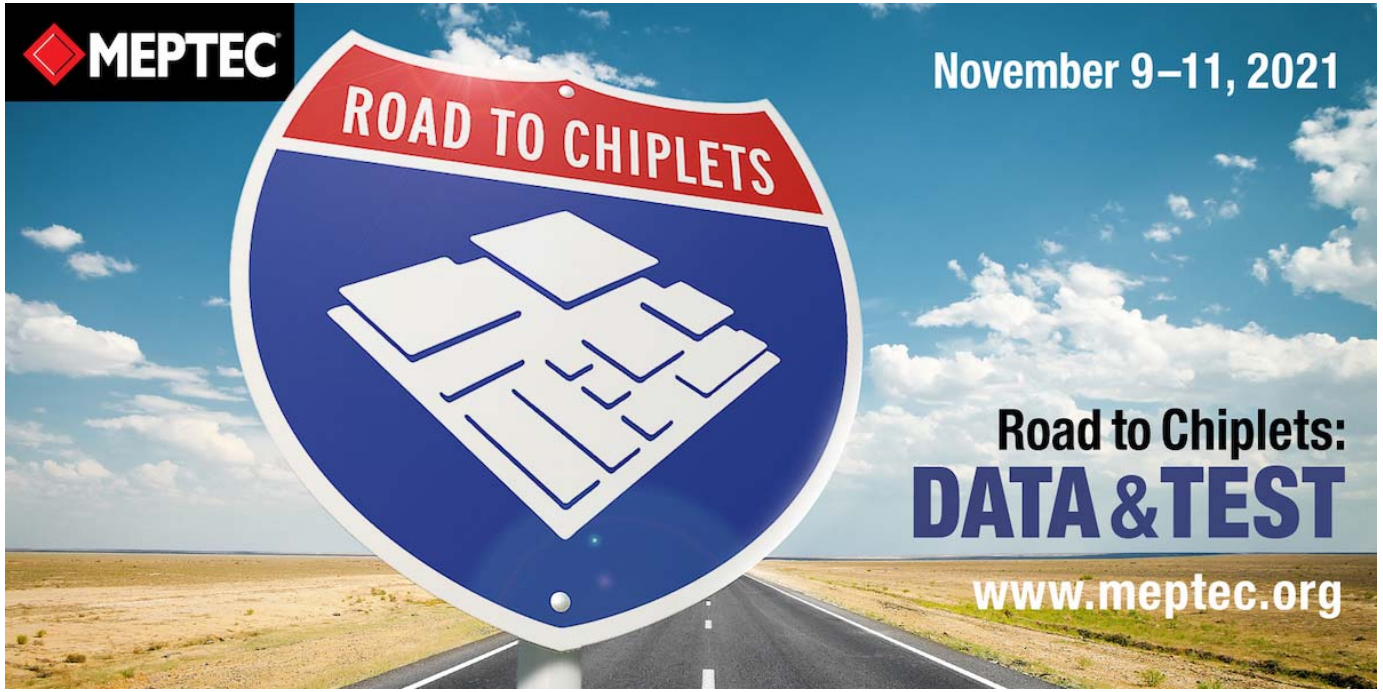

Road to Chiplets: Data & Test

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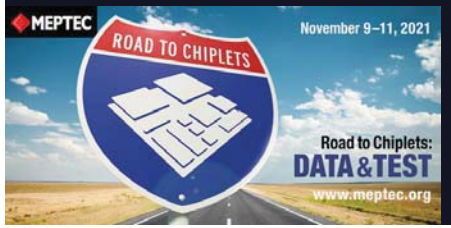
3DIC Test Challenges, Trends and Solutions – An EDA Perspective

Wu Yang
Technical & Foundry Programs Manager

Siemens EDA



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Contents

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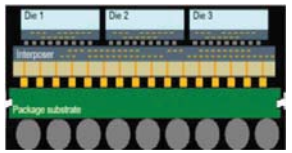
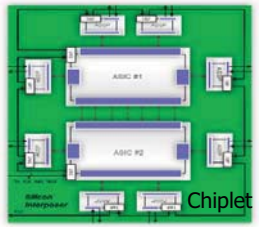
Understand 2.5D and 3D Test Challenges

2.5D (in production)



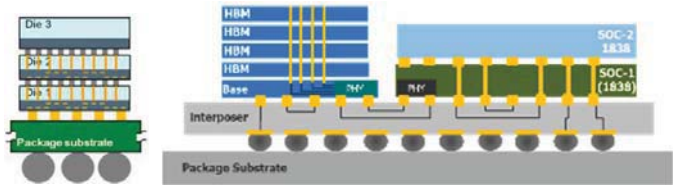


J. Reynick, Session 6C, VLSI Test Symposium, 2019

- More die DFT pins accessible at package

- Across die 1149.1 compatible TAP
- Scan data path
- Die pattern retarget to package
- Die2die tests

3D (anticipate production 2022)



- DFT pins accessible only through base die

- Setup has to go through base die
- Serial & flexible parallel port (FPP) support
- Cost, pin count, low power & automation
- Compliances to standards

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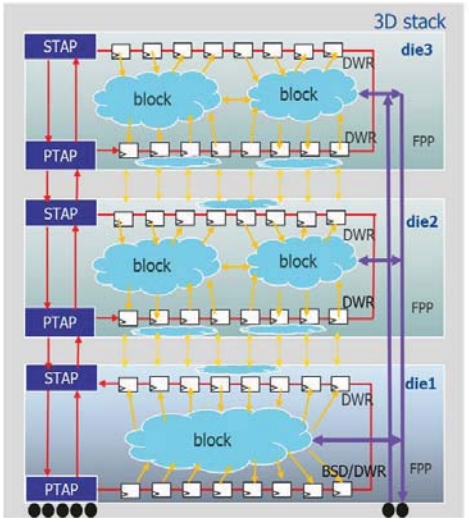
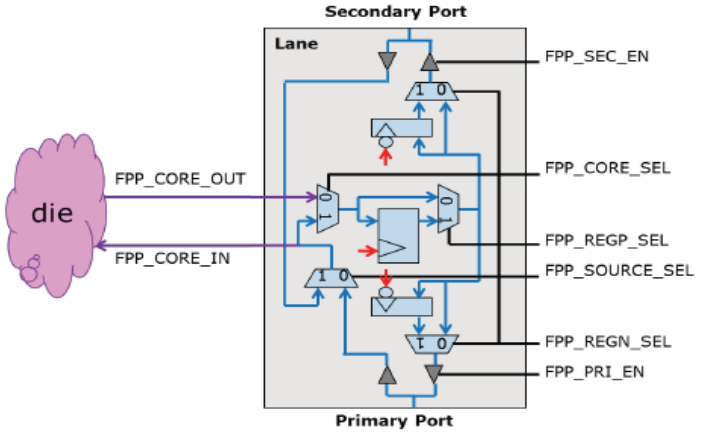
IEEE1838 for 3DIC Testing

IEEE 1838 addresses
- A standardized die DFT infrastructure for inter die integration
- Hardware and protocol

IEEE1838 doesn't
- Differentiate requirements for 2.5D and 3D
- Provide an operation language
- Discuss how to do the DFT and test



Possible logic between DWRs (die wrapper register) and IOs



Flexible parallel port (FPP)

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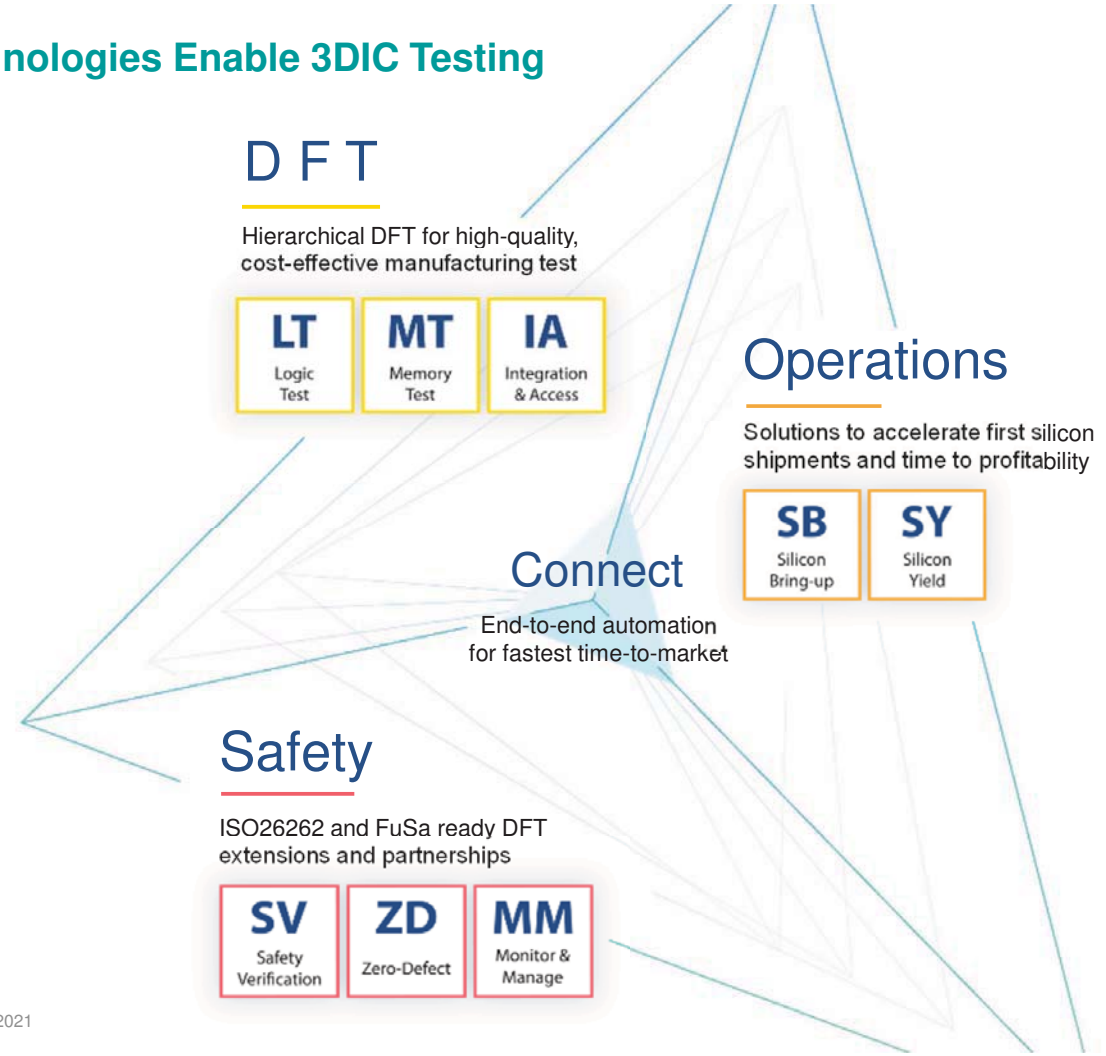
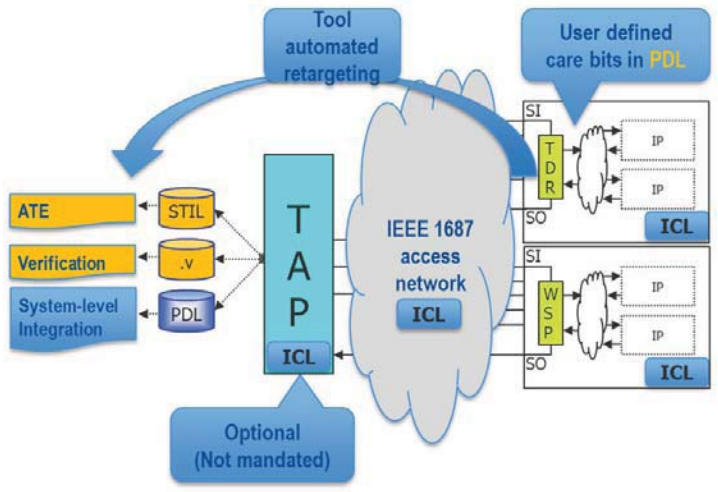
Existing DFT Technologies Enable 3DIC Testing

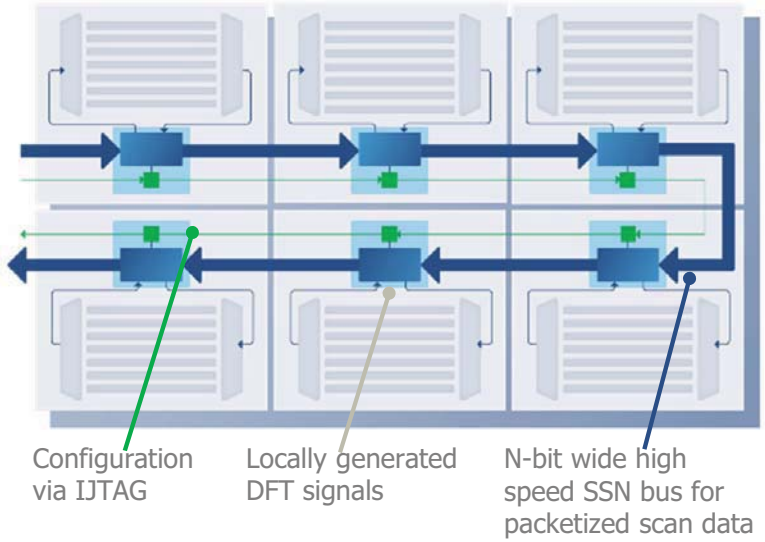


Existing DFT Technologies Enable 3DIC Testing

- Plug-and-play iJTAG infrastructure improves automation efficiency
  - Universal method to integrate any IEEE 1687/1149.1 compliant IP



- Streaming scan network (SSN)
  - Save DFT development time
  - Eases routing and timing closure
  - Up to 4X test time and volume reduction
  - Low pin & low power



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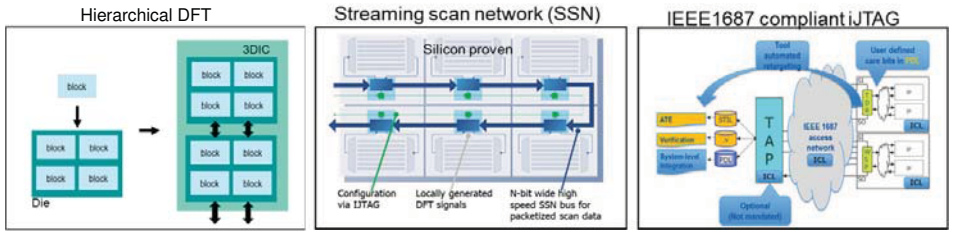
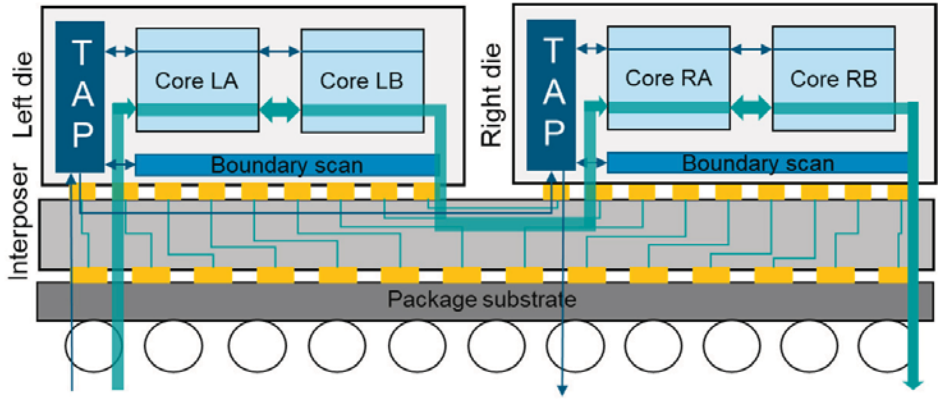
2.5D DFT Methodology

- 2.5D DFT infrastructure
  - 2.5D 1149.1 compliant TAP
  - Package-level BSDL for PCB test
  - IJTAG support for IO BIST, PHY support
- 2.5D wafer-level die test
  - Regular hierarchical DFT
- 2.5D die test in package
  - Pattern re-targeting to package
- 2.5D die-to-die test
  - BSDL-based ATPG
  - Interposer test utilizing die greybox based hierarchical DFT



IEEE Standards
(i.e. 1149 specific)

New DFT
Advancements



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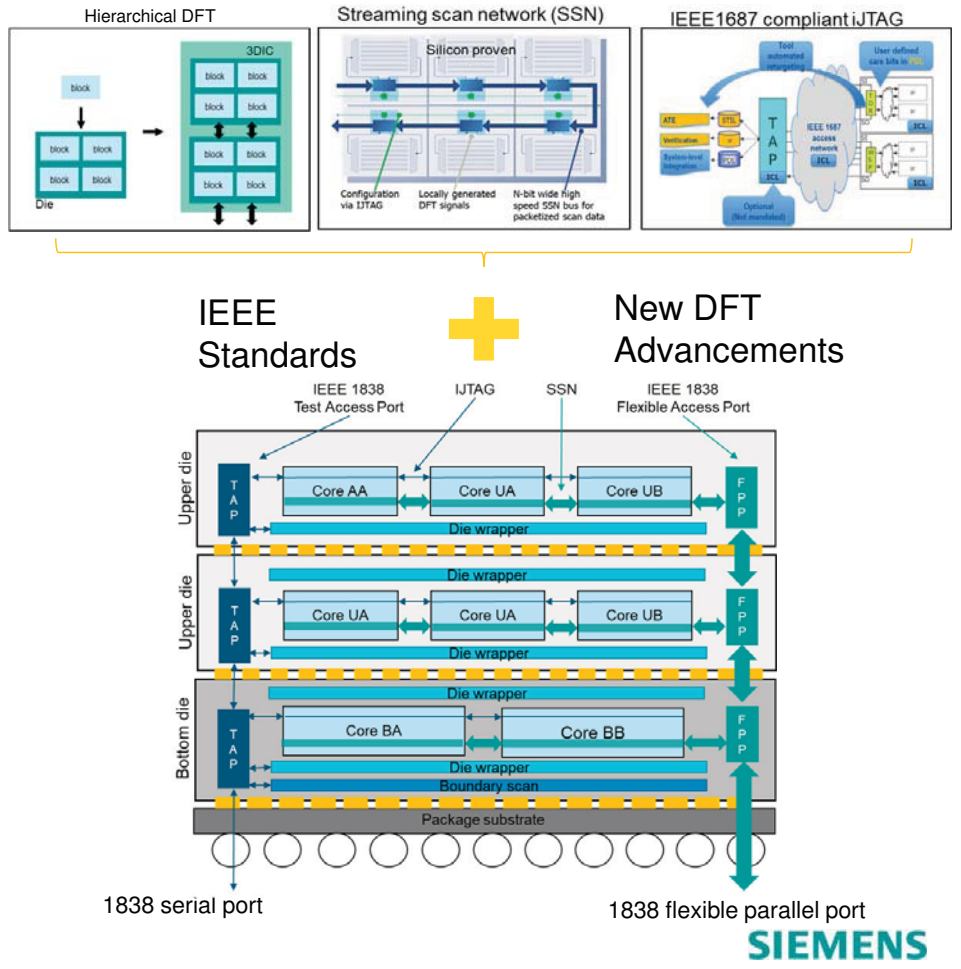
3D DFT Methodology

- 3D DFT infrastructure
  - IEEE 1838 compliant TAPs & FPP using SSN
- 3D wafer-level die test
  - Die wrapper register analysis and insertion
  - hierarchical DFT
- 3D die test in package
  - Hierarchical DFT for pattern regarget
  - SSN broadcast to dies in package
- 3D die-to-die test
  - ATPG based on package-level Verilog and graybox views of dies
- Multiple standards are needed
  - IEEE 1838, IEEE 1687, IEEE 1149.1/6/10, IEEE 1500 and etc



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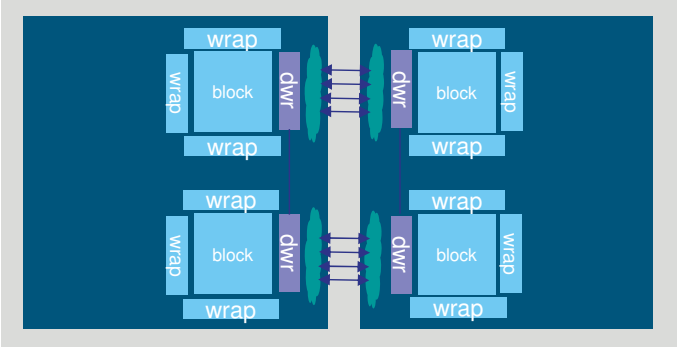
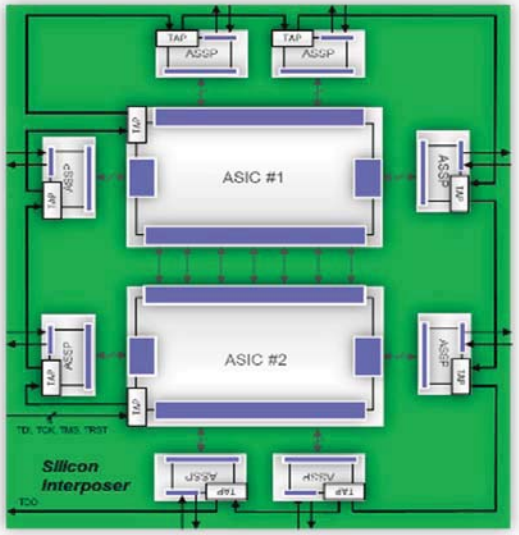
Die to Die Test





J. Reynick, Session 6C, VLSI Test Symposium, 2019

Types	Die IOs driven by BS Cells	Die IOs driven by wrap cells (logic between wrap cells and IOs)
• Low speed • Diagnosis	• Pattern gen w/ die BSDLs as inputs • Diagnosis to be supported	• D2D ATPG with low speed clock • Automatic diagnosis
• At speed • Diagnosis	• D2D atpg, or D2D snake test ○ Clocks sync-up across dies w/ Tessent OCC • Automatic diagnosis w/ at-speed pattern	
• High speed	• iJTAG hook up to custom SerDes IO BIST	

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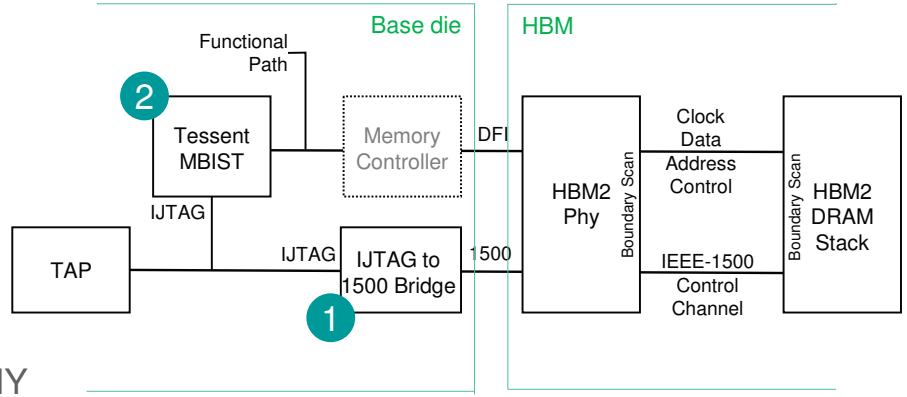
External Memory HBM (e.g. HBM2) Support

- HBM2 comes with
  - IEEE 1500 interface
  - Embedded MBIST in HBM2 stack, operational through IEEE 1500 interface
  - Other embedded features like IO repair

- Two Memory BIST tasks
  1. Connect to and operate the embedded HBM2 MBIST through the IEEE 1500 / IEEE 1687 integration
  2. If desired, implement a MBIST to connect to the PHY



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3D IC Reference Flow and ITC Exposure

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Plano, TX, USA, 26 October 2021

Siemens collaborates with TSMC on design tool certifications for TSMC's advanced technologies and other industry milestones

Ongoing collaboration with longtime foundry partner TSMC has resulted in an array of new product certifications, and that the companies have reached key milestones for cloud-enabled IC design, as well as for TSMC 3DFabric, TSMC's comprehensive family of 3D silicon stacking and advanced packaging technologies

Today at the TSMC 2021 Online Open Innovation Platform® (OIP) Ecosystem Forum, Siemens Digital Industries Software announced that ongoing collaboration with longtime foundry partner TSMC has resulted in an array of new product certifications, and that the companies have reached key milestones for cloud-enabled IC design, as well as for TSMC 3DFabric™, TSMC's comprehensive family of 3D silicon stacking and advanced packaging technologies.

The Siemens EDA offerings recently certified for TSMC's N3 and N4 processes include the Calibre® nmPlatform, Siemens' industry-leading physical verification solution for IC sign-off, as well as the Analog

Siemens has also partnered with TSMC to build a Design for Testability (DFT) flow for TSMC's 3D silicon stacking architecture. Siemens' Tessent™ software provides a leading-edge DFT solution based on hierarchical DFT, SSN (Streaming Scan Network), enhanced TAPs (test access ports) and IEEE 1687 IJTAG (internal joint test action group) network technologies, all of which are IEEE 1838 compliant. Designed for scalability, flexibility and ease-of-use, the Tessent solution helps customers optimize resources associated with IC test technology.

"Siemens continues to increase its value to the TSMC OIP ecosystem by offering more features and solutions in support of our most advanced technologies," said Suk Lee, vice president of the Design Infrastructure Management Division at TSMC. "We look forward to our continued collaboration with Siemens to help our mutual customers accelerate silicon innovations with design solutions combining Siemens' leading-edge electronic design automation (EDA) technologies with TSMC's latest process and 3DFabric technologies."

Finally, Siemens' close collaboration with TSMC recently enabled the Calibre tools to demonstrate dramatic performance and scaling improvements for one of the world's foremost IC design firms within a leading cloud computing environment. Made possible by the optimization of the latest setup, decks and engine technologies for cloud environments within Calibre, these advancements can help joint customers realize faster time-to-tapeout and time-to-market. To learn more, please make plans to view Siemens' technical presentation during the TSMC 2021 Online OIP Ecosystem Forum.

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Siemens has also partnered with TSMC to build a Design for Testability (DFT) flow for TSMC's 3D silicon stacking architecture. Siemens' Tessent™ software provides a leading-edge DFT solution based on hierarchical DFT, SSN (Streaming Scan Network), enhanced TAPs (test access ports) and IEEE 1687 IJTAG (internal joint test action group) network technologies, all of which are IEEE 1838 compliant. Designed for scalability, flexibility and ease-of-use, the Tessent solution helps customers optimize resources associated with IC test technology.

Conclusion

- 3DIC test solution built upon both existing technologies and new advancements
  - Hierarchical DFT, SSN and IJTAG provide a solid foundation
  - IEEE1838 hardware and lots of enhancements make 3D solution available
- 3DIC is a Moving Target
  - Heterogeneous die support using different DFT vendor solutions
  - Interposer test during stacking
  - Redundant IO & lane and their repair requirements
- Call for an all-industry collaboration to enable 3DIC ecosystem for testing
  - Build reference flows
  - Define standard interface for die to die communication and data exchange if using different DFT vendor solutions

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— **Risto Puhakka**, President VLSIresearch


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