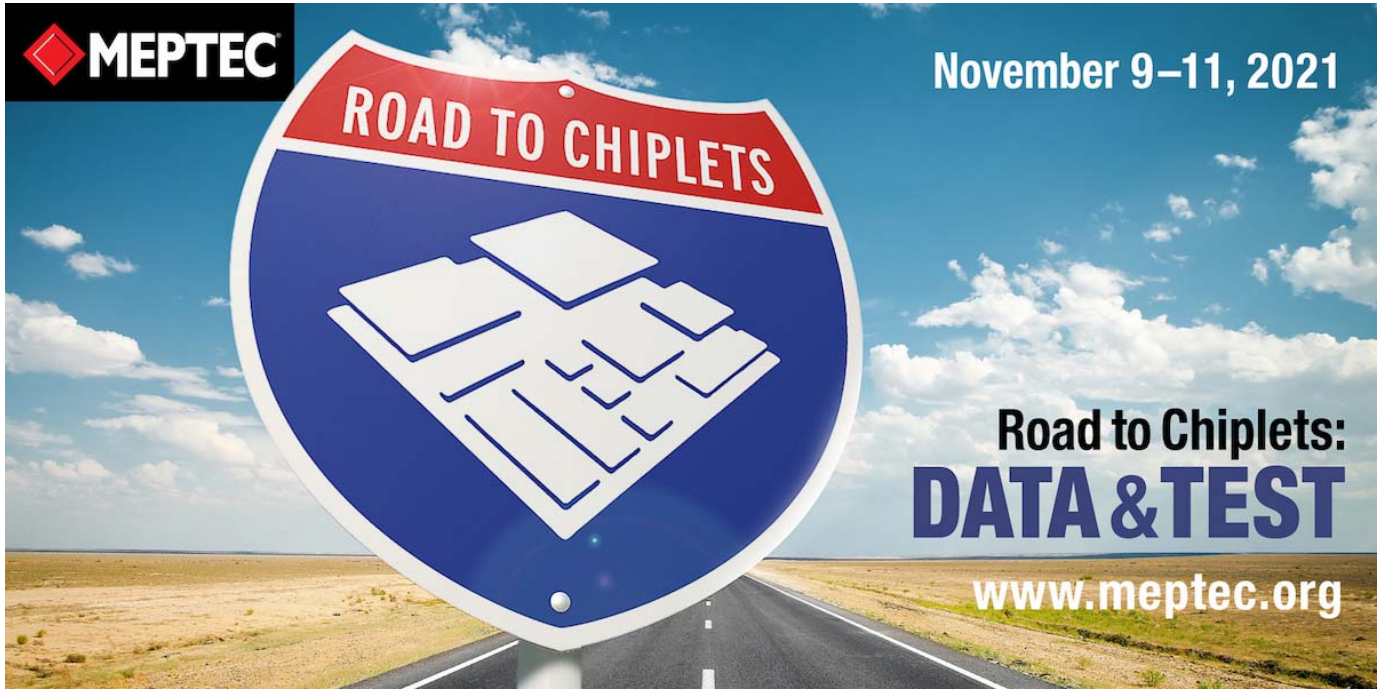

Road to Chiplets: Data & Test

November 9 - 11, 2021

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Chip to Chip Interface Testing

Adam Wright

Ack. Ann Poh Gan, Ching Sia Lim

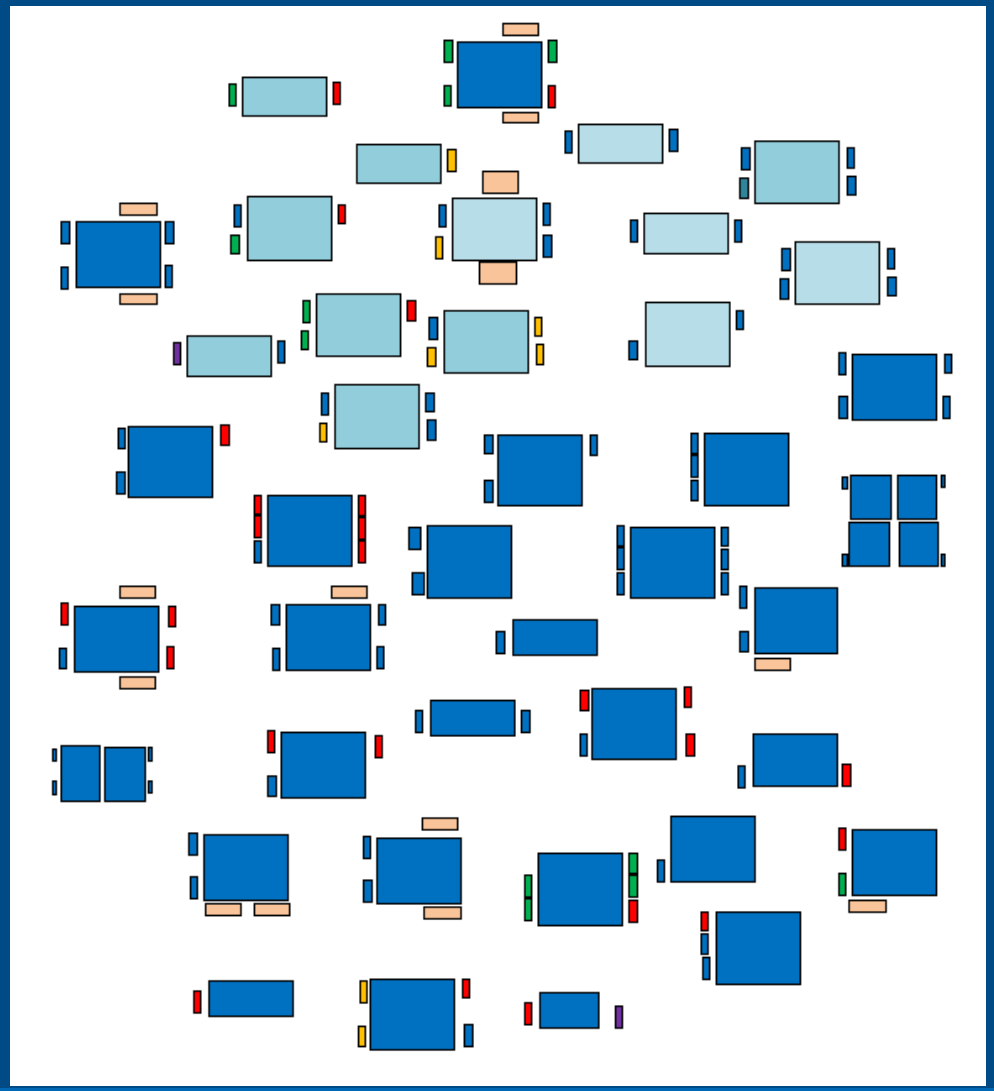
November 2021

Agenda

- FPGA multichip variations
- Types of Development Partnerships
- Challenges
- Calls To Action
- Conclusion

FPGA Application

- FPGAs are a magnet for chiplet integration
  - Forgiving as a mother chip
  - Already experts at fungible IO
- Product Benefits for our customers
  - Cost Reduction paths allow us to chop tiles, use lower cost mother FPGA
  - Known-good high-speed serial interfaces between product families

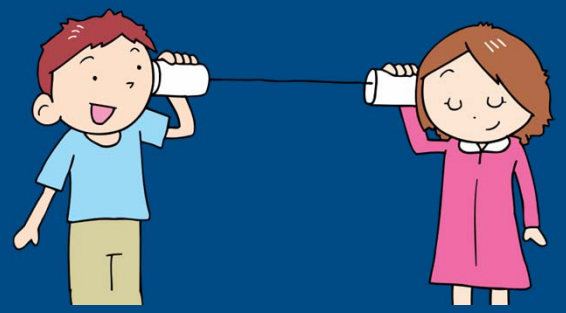


Development Partnership Evolution

Single Vendor Codesign

- bends toward proprietary testing
- With no established standard will evolve into a closed ecosystem

Multiple Vendor Codesign



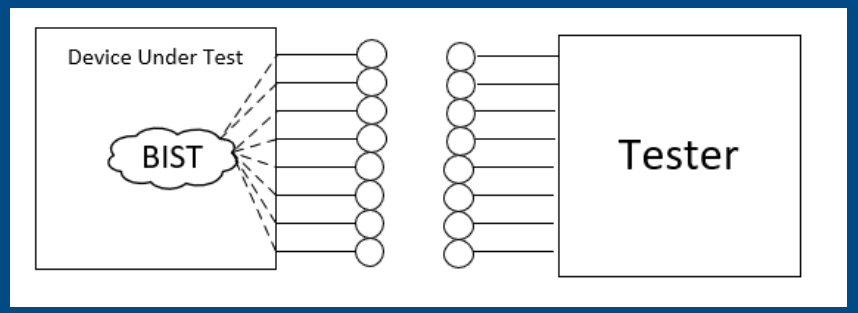
- Steps toward heterogeneous ecosystem
- Requires rigorous specification of the test approach

Ala Carte

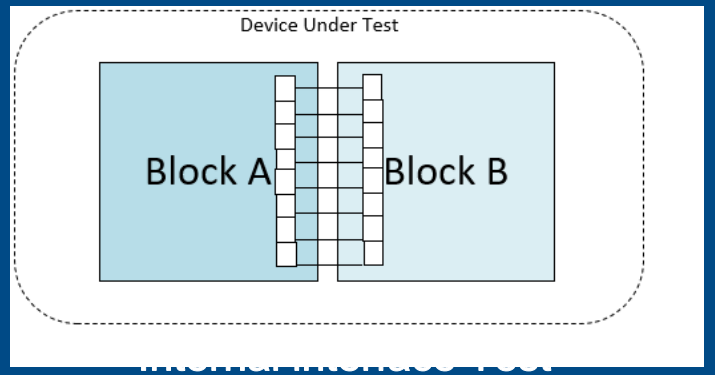
- Durable standardized test approach
- Persistence and backward compatibility

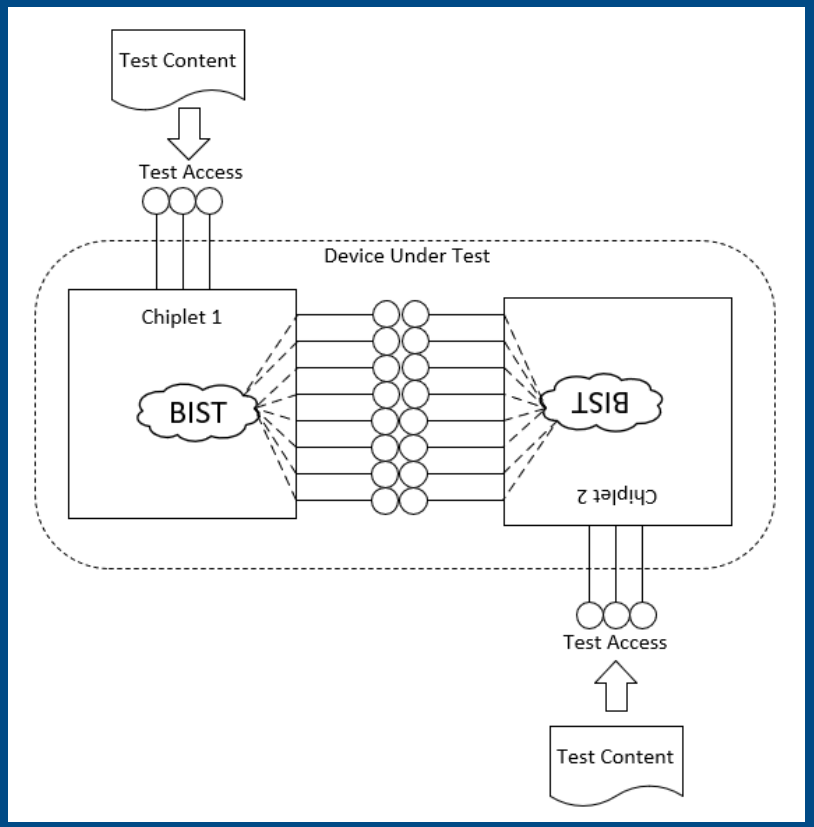
Designing System level DFX

- Chip2Chip testing is a unique DFX challenge – system level test between two separate chips during packaged unit test



External interface test Test





Maintaining Manufacturing Alignment over Decade(s)

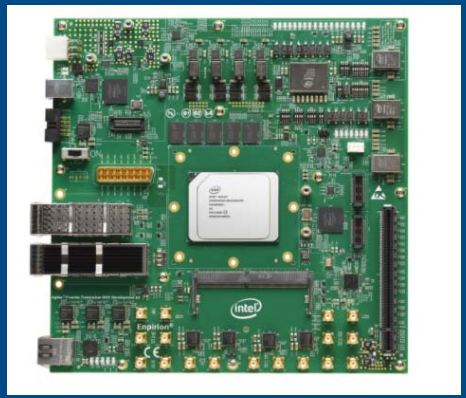
- We are constantly learning – need to maintain legacy compatibility while advancing the art
- Chiplets can have lifetimes equivalent to any typical component
  - Only mother die/chiplet codesign was in 2015, all other improvements are leapfrogging between mother/tile

Mine, Yours, Ours

Root causing problems significantly more to dispose across vendors than discrete components

- Vendors responsible for PVT DPM coverage on components
- Vendors responsible for qual
- PCB a “DMZ” - well understood interface between components
- Well defined component to component interface standards
- Clear quality criteria for each vendor in the system

Traditional PCB

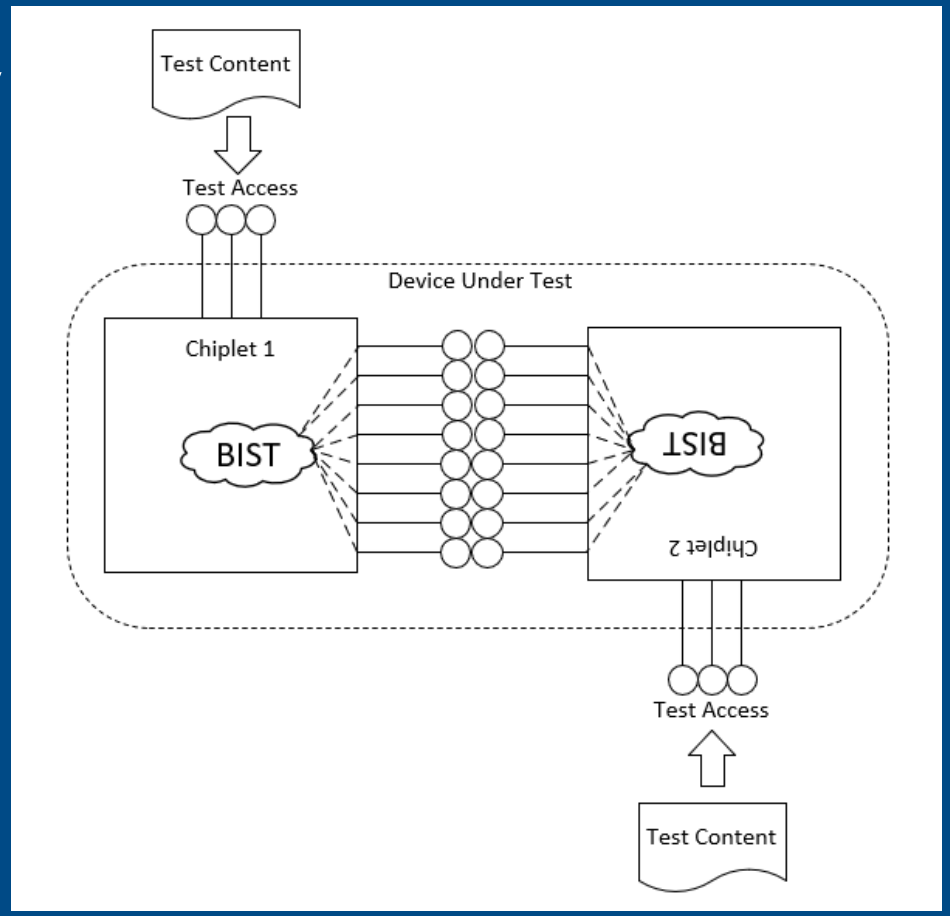


Heterogeneous Integration

- Vendors can only screen to the die level
- Package/integration qual becomes the integrators task
- PCB “DMZ” replaced by embedded, proprietary interconnect
- Inter package IO interfaces standards in infancy
- Quality criteria incomplete for chiplets delivered to the integrator

System Level DFx Investment

- Need full recognition that C2C DFx requires system level coordination early
- Inter chip BIST compatibility
- Visibility to next gen interfaces
- Backward compatibility
- Standardized test access
- Failure Isolation capability
- Security and test need to play well together
- Overinvest instead of underinvest

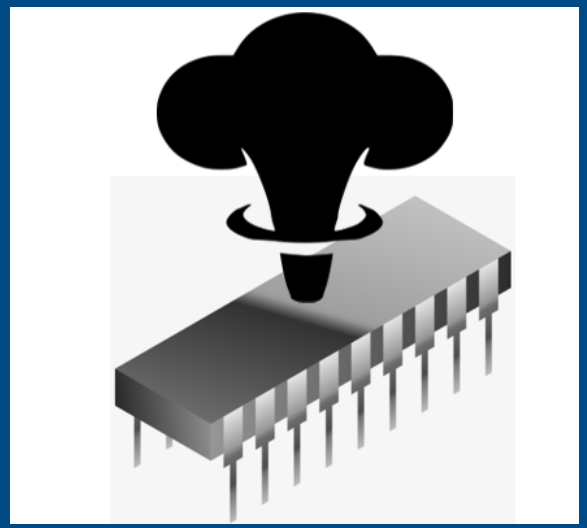


Develop Chiplets Like Components

- Chiplets as a full-blown product: Documentation, C2C interface characterization, Qual
- Accretive approach, avoid too much, too soon
- common PLC parameters: cost, lifetime, DPM
- Ensuring *support* over chiplet lifecycle
- Develop C2C interfaces and standards with the same rigor and robustness of intercomponent protocols
- CAD Ecosystem to support integration, common system level understanding among vendors and customer
- Standardize inter-vendor handoffs and requirements (or intra vendor for that matter)
- Good contracts make good partners – make sure that negotiations include manufacturing requirements

Getting to the Root of the Problem

- Need rapid *vendor level* failure analysis capability
- Service Level agreements on debug
- Service Level agreements on debug
- Fungible across integrators, platforms, heterogeneous permutations
- Controlling debug TAT among vendors and products of differing maturity
- Investment in physical isolation
- Robust design and integrations
- Can we compare and contrast to the PCB system debug model?



Ensuring that the Customer Succeeds

- We are replacing an established integration model – need to understand the challenges we are taking from the board/system design into the product
- “Designing-in” quality is the bedrock foundation of semiconductor and system success
- Continuous improvement to ensure quality early and often is a large investment
- Need the design investment in quality up front AND observability to drive effective cost reduction and quality assurance

Final Thoughts

- 1% inspiration, 99% perspiration – to move to a manufacturable mix and match heterogeneous ecosystem requires significant investment from both technical and business perspective

- Overinvest in test, debug and failure isolation for these buried interfaces
  - Think of the investment we have for other standard genres of circuits (MBIST, ATPG), how do we get to that level of manufacturing efficiency

- There needs to be an openness among vendors if we want an ecosystem thrive

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