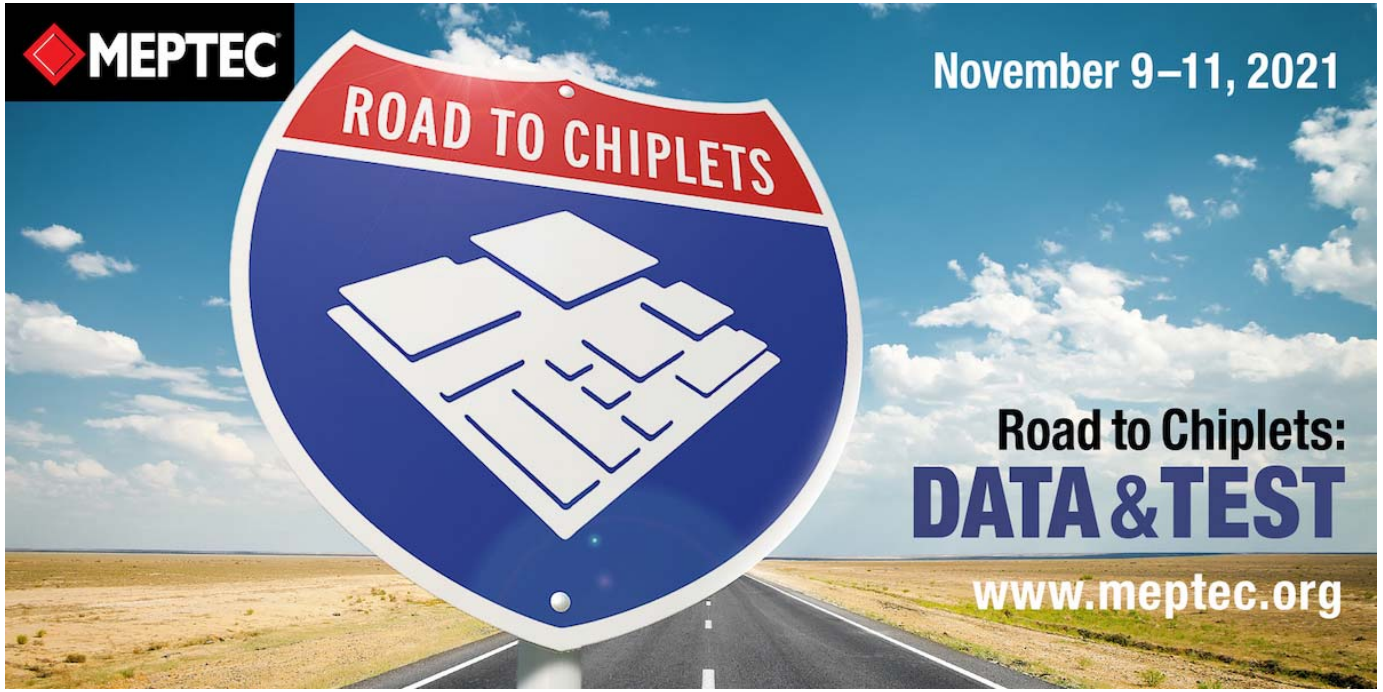


Road to Chiplets: Data & Test

November 9 - 11, 2021

MEPTEC
THE NEXT GENERATION

www.meptec.org

MEPTEC 2021: Road to Chiplets DATA & TEST

Debug and Fault Isolation Strategies as the Industry moves towards 3D-ICs

Tan, Terrence Huat Hin

terrence.huat.hin.tan@intel.com

Senior Principal Engineer

Manufacturing and Product Engineering, Intel Malaysia

Acknowledgement:
Letchumanan, Devanraj devanraj.letchumanan@intel.com
Leow, Teng Jun Nicholas teng.jun.nicholas.leow@intel.com

Outline

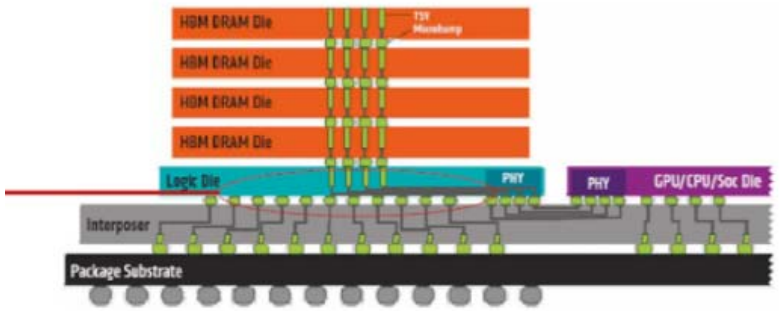
- Test and Debug Challenges
- 100% Package Test Equivalence at Bare Die for Test/Debug
- Package Test with Inline Debug/Fault Isolation Capabilities
- DFT for 3D-IC Debug Considerations
- Call for Actions
- Summary

The main concern isn't really testing – it is yield and quality

Wafer Test → Package Test → System Test → Field Test

HBM
Logic Chiplet
Interposer (Active)
CPU Chiplet
GPU Chiplet

→ Package Assembly



For illustration purpose only

"30 bare die, each 99% quality … Final package yield loss: 26%"

- How do we effectively debug and isolate failures at final package test?
- What is needed in each chiplet (bare die suppliers) to provide effective debug and fault isolation at final test
- How do we make use of debug capability for each die at package level?"

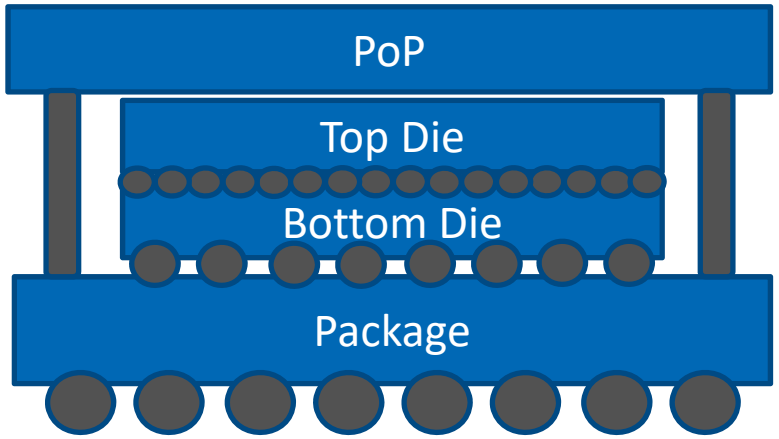
"KGD does not mean all shipped die will pass package, system and field"

- How do we deal with field return ?
- How do we debug system test failures which is a measure of DPM ?

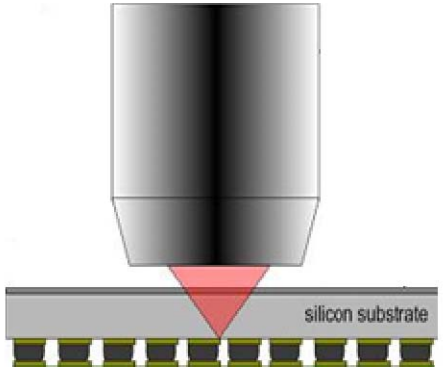
In 3D-IC, Physical FA and Probing is a Huge Challenge

***Reference**: Letchumanan Devanraj,*
ITC 2020 3D Chiplet Test, "Who's At Fault? A Creative Way To Isolate and Debug Internal IO"

Intel Foveros Example:



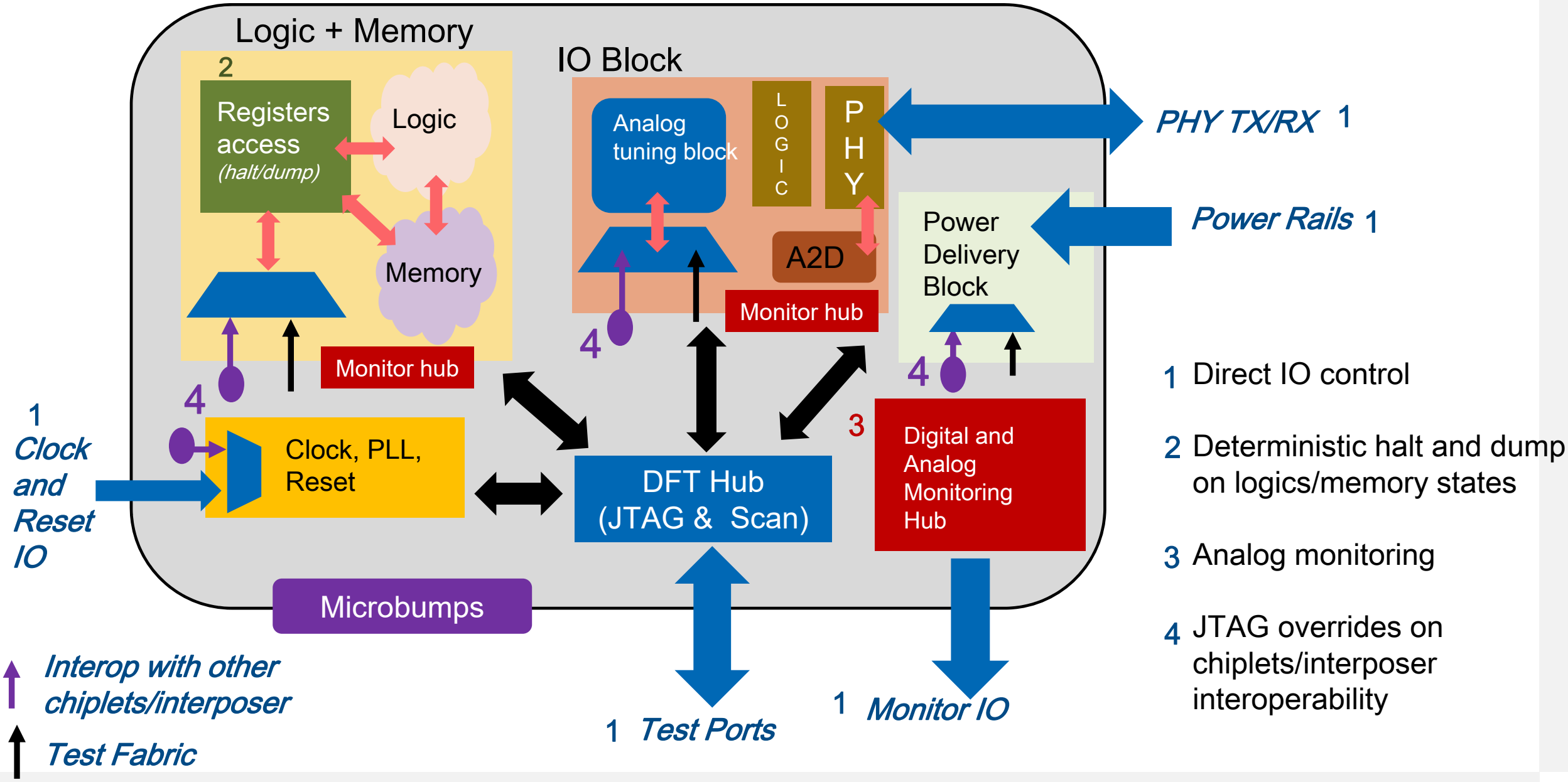
Monolithic die optical probe:



Successful defect finding and time to root-cause is key

- Need 100% Package Equivalence at Bare Die for Test and Debug
- Test Flow with Inline Debug/Fault Isolation Capabilities
- Design for Debug Hooks for 3D-ICs

Need 100% package equivalence test/debug at bare die



1 Direct IO control

2 Deterministic halt and dump on logics/memory states

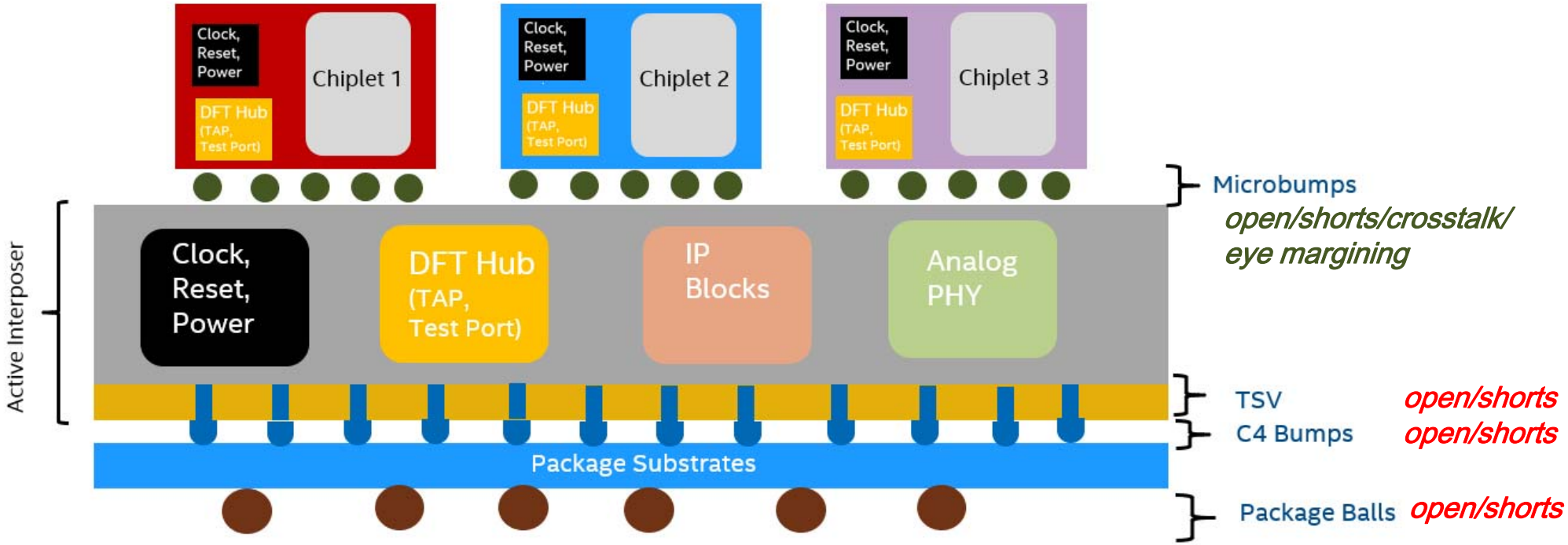
3 Analog monitoring

4 JTAG overrides on chiplets/interposer interoperability

Steps in Final Test for Inline Debug/Fault Isolation

Assembly Screen → Test Access Mechanism → Clock, Reset, PLL, Power Delivery → Die to Die Interconnects → Test Coverage (logic, array, analog, performance)

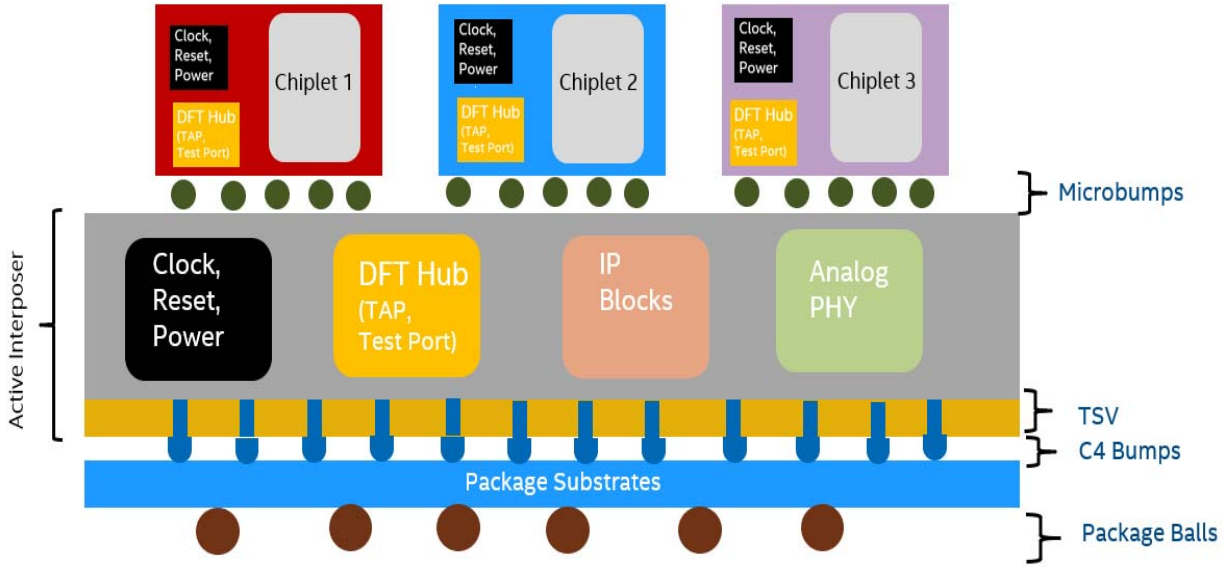
Unique failures introduced upon 3D-IC package integration



3D-ICs need have DFT hooks in for test coverage as well as providing diagnosis feedback during product debug

Design for Debug/Fault Isolations Hooks for 3D-ICs

- Bare minimum bring up of each chiplets
  - Power delivery schemes works by default
  - Simplification of clock and reset generations and distributions (e.g. can be done w/o PLL)
- Test access mechanism (JTAG & Parallel Test Port) check can be done in loopback mode at test port speed
- Die to die interconnects has sufficient diagnostic capabilities via JTAG
  - Data pattern types
  - Which d2d signal fails
  - Margining data/clock relationship
- Interoperability handling i.e. cross-chiplets, active interposer-chiplets
  - Direct JTAG overrides
  - Isolate active interposer
  - Disable all handshakes between chiplets
  - Able to enable/disable each chiplets



Die2Die Interconnect Diagnosis Best Practices

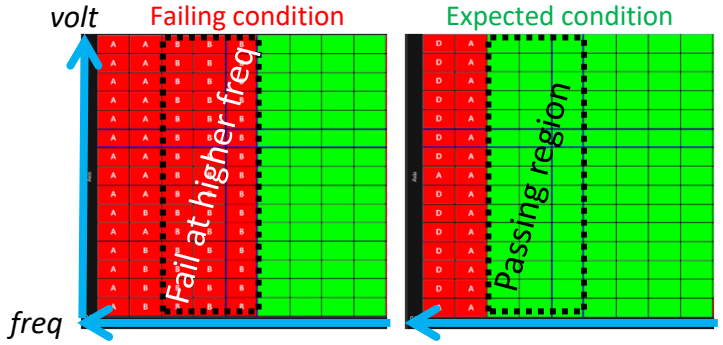
1. ***Test*** **-** A stacked die package had failed die-to-die interconnect test at-speed while passing at lowered frequency
2. ***Diagnose*** **–** Enabling various die2die diagnostic patterns to pin point failing modes. Both die need to have similar diagnostic capability.
3. ***Isolate*** **–** Diagnostic patterns narrowed down to failing path.

Without sufficient DFT coverage, a more invasive debug/FA approach would be required to root-cause the failure

DieA NELB	Die-to-die (B to A only)	Failing mode(s)
fail	fail	Short at A/B/Diodes/Bump
fail	pass	Die A logic
pass	fail	Open Bump OR Die B logic

Reference: Letchumanan Devanraj, ITC 2020 3D Chiplet Test, "Who's At Fault? A Creative Way To Isolate and Debug Internal IO"

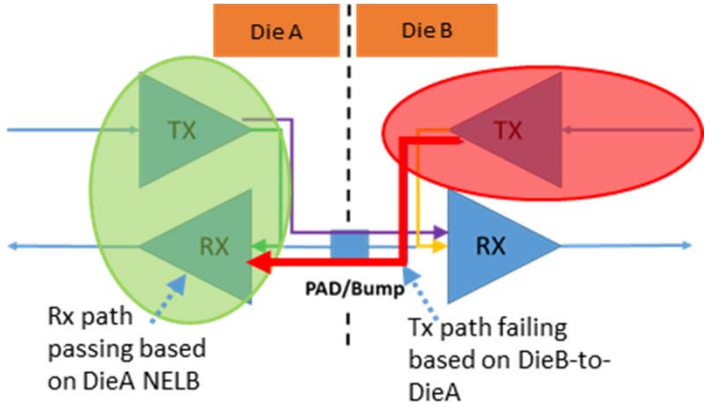
1



2

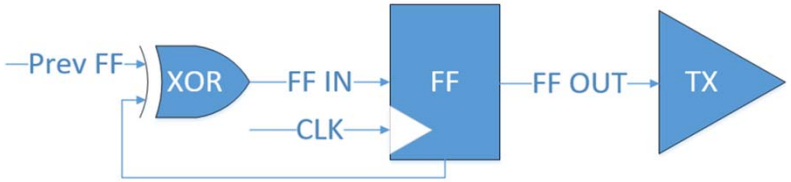
DieA NELB	DieB NELB	Die-to-die	Failing mode(s) for NELB at PAD
fail	fail	fail	Short at A/B/Bump
fail	fail	pass	Marginal/Resistive if fail at-speed NELB only
fail	pass	fail	Die A logic: TX if A-to-B OR RX if B-to-A failed
fail	pass	pass	Die A logic
pass	fail	fail	Die B logic: TX if B-to-A OR RX if A-to-B
pass	fail	pass	Die B logic
pass	pass	fail	Open at Bump

D2D test is uni-directional, based on mission mode



Failing path identified

3

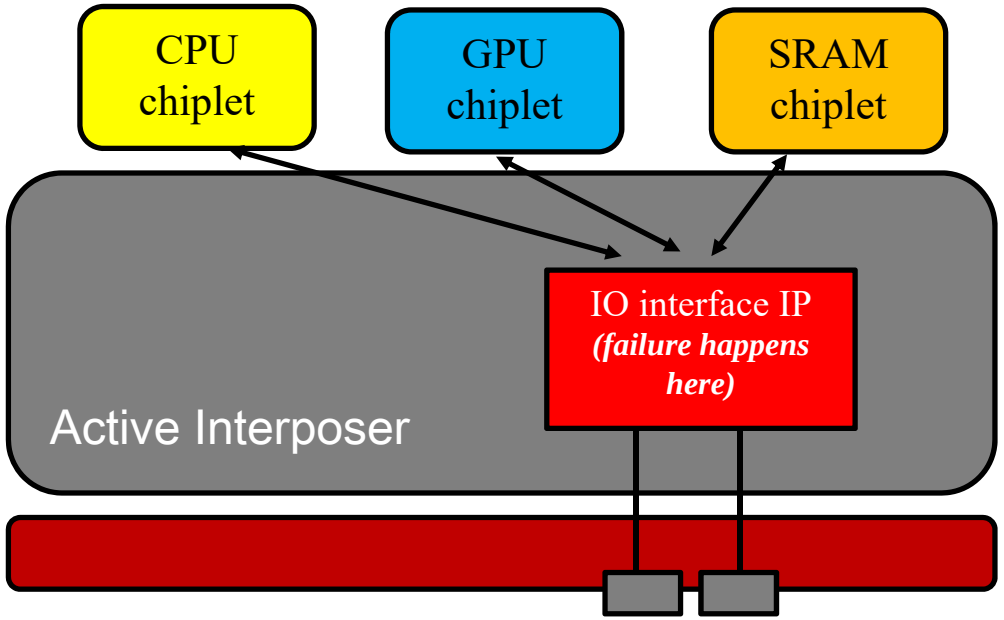


Dealing with Field Returns

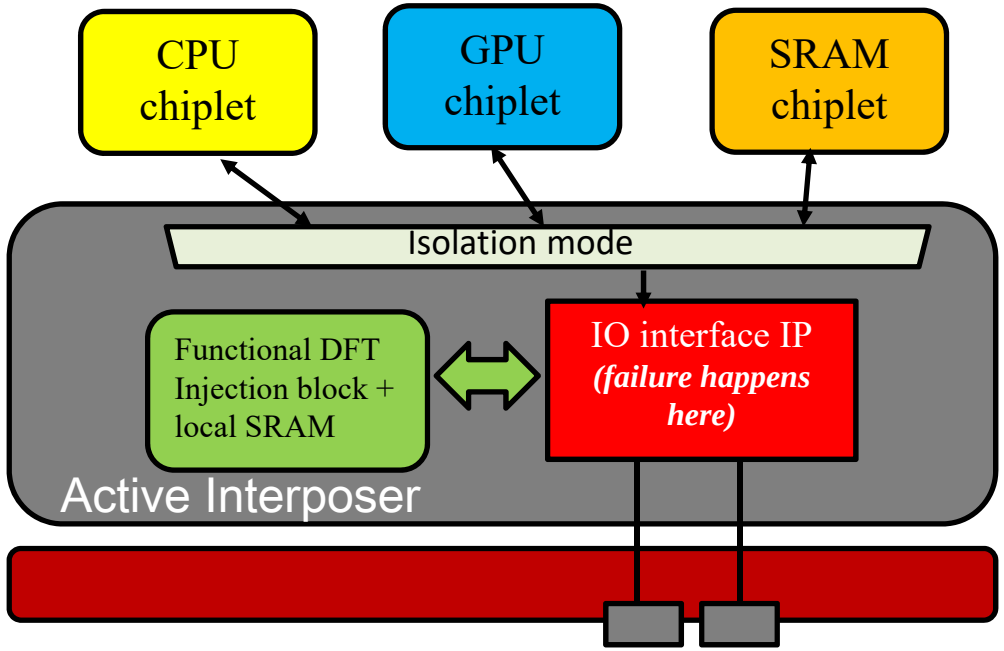
Field Failures → Reproduce Failure In House SLT → SLT and ATE Correlation → ATE Characterization and FAFI

- On die system debug capabilities via JTAG
- Isolation is critical here (which block, sensitivity to PVT)
- Able to run ATE chiplet test on SLT environment

System: requires CPU/GPU/SRAM to co-interact with failing block to reproduce the failure



ATE : Any functional test that we need to perform on the active interposer need to be standalone, isolate from chiplets



How should industry evolve to support debug requirements for 3D-ICs as we get chiplet from different vendors?

- In a multi-vendor chiplet product, debug and fault isolation best practices also must be added to the standards. This is not an issue for multi-die from one company with mixed process node.
- IEEE 1838: extend to include 3D product debug and bring up, currently does not
- IEEE P2929: standardized chiplet debug requirements (scan/array) at die, package and system
- Die to die interconnect (OSDA, BoW): need to comes with ATE friendly diagnostics best practices
- Analog IP suppliers: die level analog tuning overrides via JTAG and die level observability
- JTAG is often used in product bring up and debug to access and dump out internal registers, including debug registers not normally part of user visible state.
  - The industry will need to develop a format (adhere to security) to exchange and access internal register states that can be “dumped” to root-cause failures.

Industry need specify an interoperation standards that chiplets can work together for test, bring up sequence, and debug (low yield, DPM and RMA).

Summary

- Debug and fault isolation is a key aspect when come to test.
- Test flow need to comprehend inline fault detection and isolation.
- Shift left to die level test is key when come to **test, repair, debug, and binning** for 3D integration.
- Chiplet market place needs to transfer all **these** information from die supplier to package and system integrator.
- Existing IEEE standards for 3D test need to evolve to comprehend debug and fault isolation at die, package and system level.

Coming Dec 2021....
One stop shop for Requirements on 3D-IC Test and Debug


IEEE ELECTRONICS PACKAGING SOCIETY
Test Technical Committee

Heterogeneous Integrated Product Testability Best-Known Methods (BKM)

Draft Revision 0.5

Sponsor

Test Technical Committee of the IEEE Electronics Packaging Society

Approved *TBD* December 2021
IEEE EPS Test TC

Legal Notices

This presentation contains the general insights and opinions of Intel Corporation (“Intel”) that are provided for informational purposes only and subject to change without notice. Statements in this document that refer to Intel’s plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel’s results and plans is included in Intel’s SEC filings, including the annual report on Form 10-K.

Any forecasts of goods and services needed for Intel’s operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation. Intel technologies’ features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.


intel

Thank you sponsors!

Amkor's Differentiators

Technology

Advanced Packaging Leadership
Engineering Services
Broad Portfolio

Quality

QualityFIRST Culture
Execution
Automation

Service

Design & Test Through Drop Ship
Manufacturing Footprint
Local Sales & Support

Global Companies Rate Advantest THE BEST ATE Company 2021

Advantest receives highest ratings from customers in annual VLSIresearch Customer Satisfaction Survey for 2 consecutive years.

Global customers name Advantest THE BEST supplier of test equipment in 2020 and 2021, with highest ratings in categories of:

Technical Leadership – Partnership – Trust – Recommended Supplier – Field Service

"Year-after-year the company has delivered on its promise of technological excellence and it remains clear that Advantest keeps their customers' successes central to their strategy. Congratulations on celebrating 33 years of recognition for outstanding customer satisfaction."

— **Risto Puhakka**, President VLSIresearch


SYNOPSYS®
Silicon to Software™

COPYRIGHT NOTICE

www.meptec.org

MEPTEC
THE NEXT GENERATION