Road to Chiplets: Data & Test

November 9 - 11, 2021

MEPTEC
THE NEXT GENERATION

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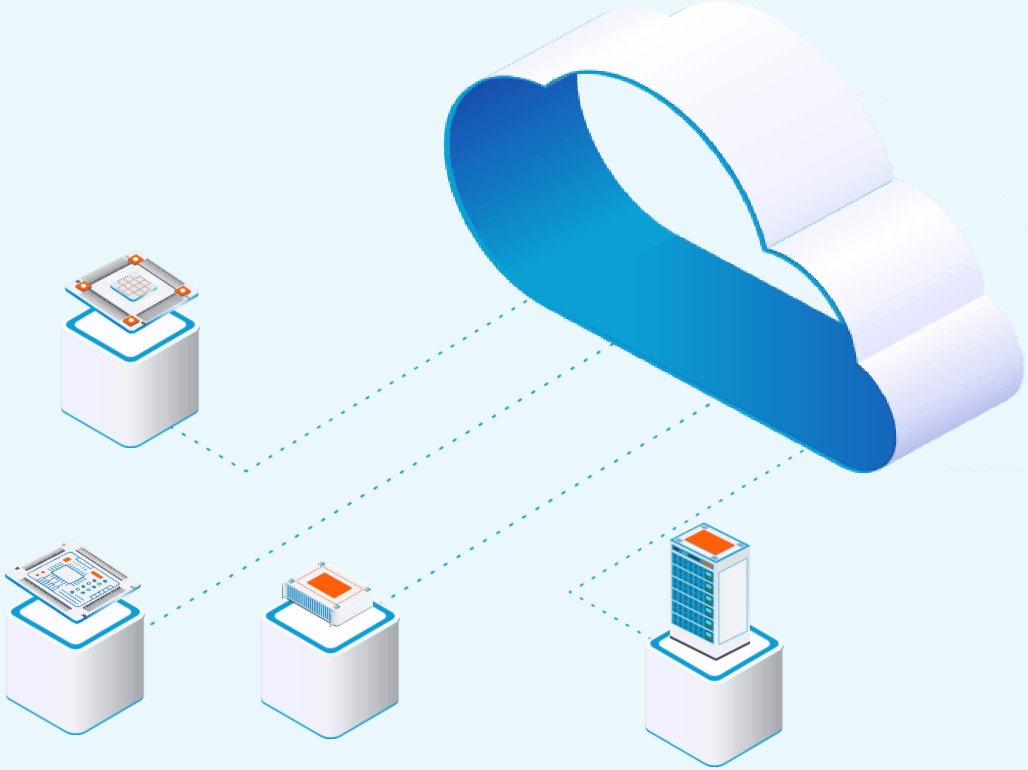
proteanTecs
Electronics visibility. From within.

Lifetime performance and health monitoring of high bandwidth, die-to-die interfaces using chip telemetry



November 9-11, 2021

Nir Sever, Senior Director of Product Marketing

proteanTecs Leading a New Category

Deep data health & performance monitoring for advanced electronics

Founded in 2017 by industry leaders and **co-founders of Mellanox**

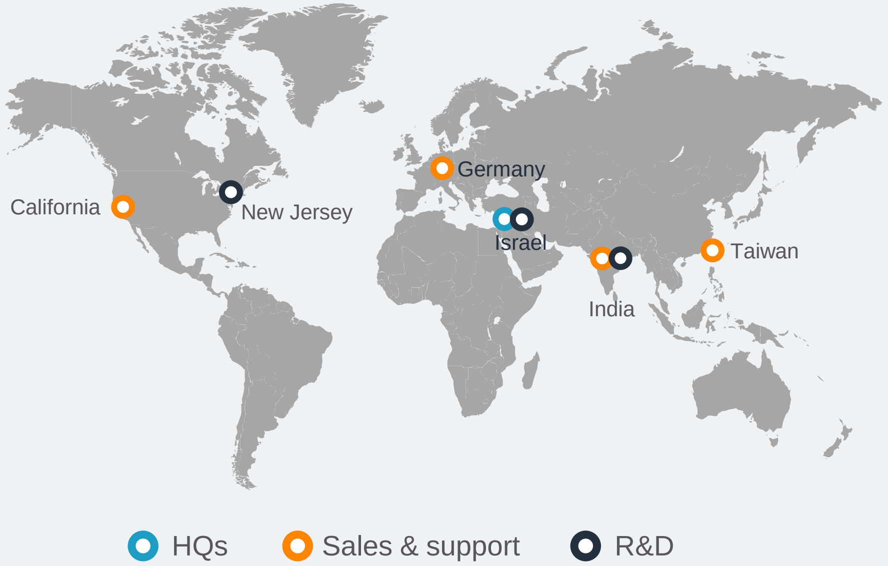
Addressing industry-wide challenges of **scale**

Production proven in 28/16/7/5nm

Customers in multiple key segments including **Datacenter, Automotive, and Communications**

New category with a **multi-disciplinary** approach

Global Footprint



Responsibility moves to the machine

- → Electronics everywhere
- → 24/7 availability
- → As-a-service

A siloed industry unprepared for scale

12-18 months
of chip **debugging**

Warranty claim rates
2.7% of
product revenue

50% of fault
investigations **inconclusive**

1 car failure
per hour

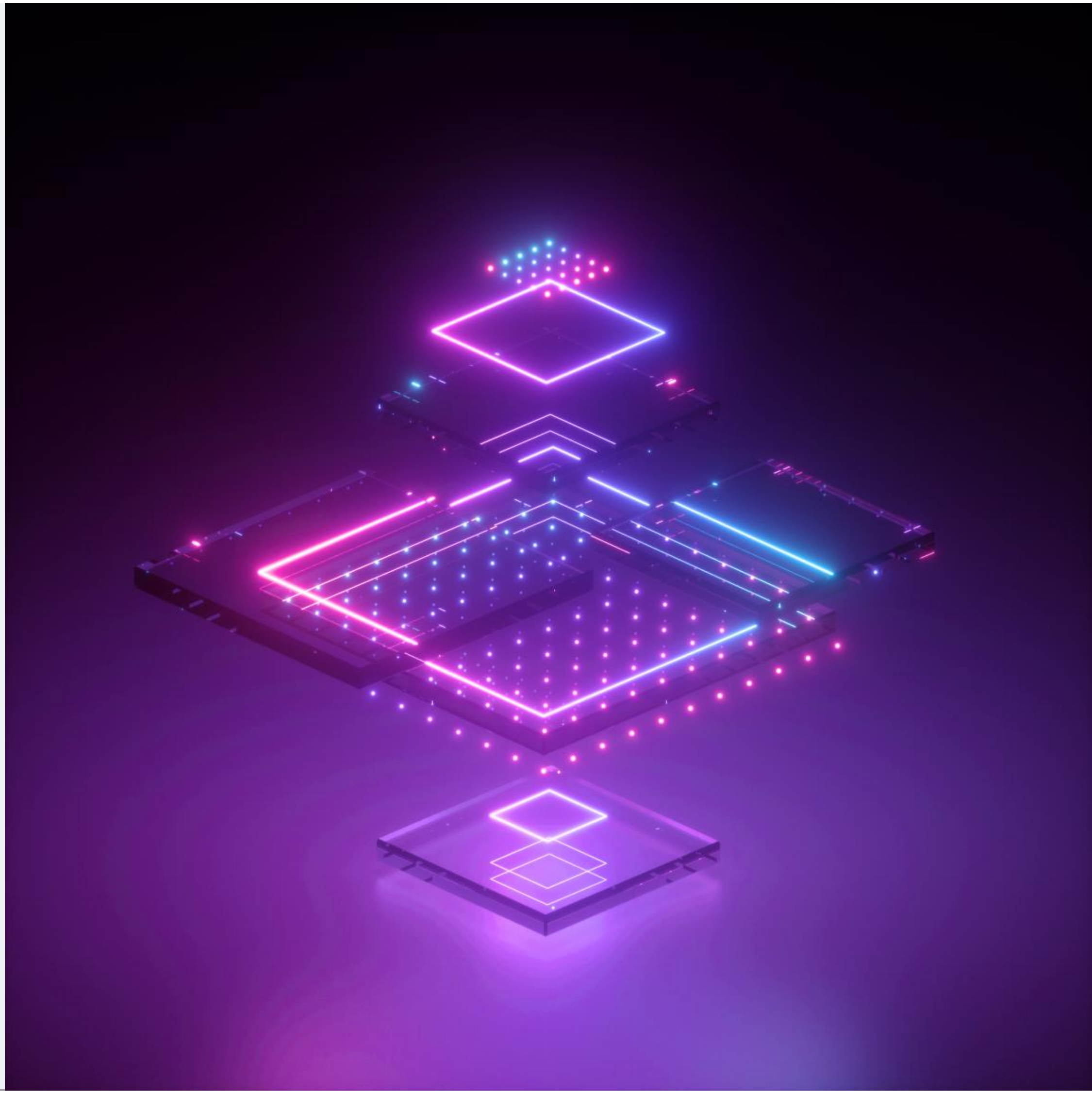
Mega functionality

- → Advanced technologies
- → Quality/ performance tradeoffs
- → Surging costs

Sources:
1. McKinsey & Company, Advanced Analytics in Semiconductor Manufacturing; 2017
2. Warranty Week, Warranty Claims Rates by Industry; 2019
3. Internal calculations
4. Audi, DVCon Munich, 2017

More Than Moore

- Allow overcoming reticle size limitations for large devices
- Improve yield: Yield goes down exponentially with size but with tiling, it is linear
- Allow hybrid devices: Each IC in a SiP can be manufactured at a different process:
  - CPU/GPU/NPU/TPU on latest CMOS technology
  - DRAM on DRAM process
  - Wireless/RF on Analog RF process
- Support “economies of scale” with Chiplet
  - Uses the same building block multiplied according to application instead of multiple designs



Different Technologies, Similar Challenges

Substrate Technologies

Silicon Interposer

CoWoS®

Organic Substrate

InFO

Physical Interconnect Technologies

Serial

XSR/USR

SERDES

Parallel

HBM2, HBM2e, HBM3

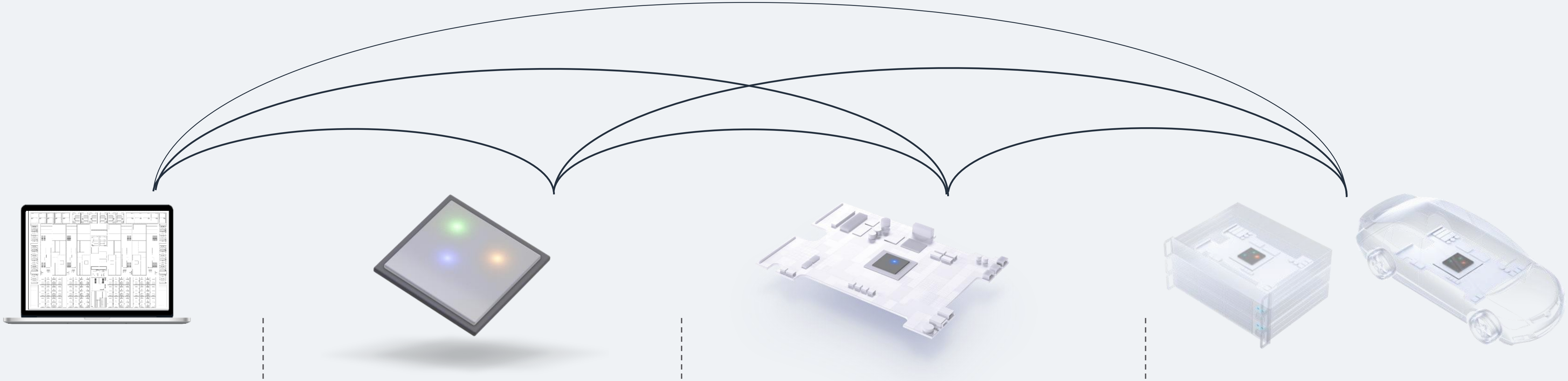
OpenHBI (-2, -3)

Glink™, AIB (Gen1, Gen2), BoW

Common Challenges

- Many 1000’s of possible failure points (u-bumps, traces, TSVs)
- Degradation over time
- No visibility after assembly
- **No operational mode visibility**

Visibility at Every Stage



Chip Design

Variability Analysis
Production Visibility

Chip Production

Higher Confidence Volume Ramp
Outlier Detection
Performance Yield

System Production

Performance Optimization
Workload Analysis
Environmental Monitoring

In-Field

Performance Monitoring
Alert on Faults before Failures
Predictive Maintenance

Faster Time to Market **10X Lower DPPM** **Reduced Costs** **Failure Prevention**

Multi-Pillar Solution

Deep Data

Universal Chip Telemetry™ (UCT) with on-chip Agents

Machine Learning

Agent fusion and inference with ML algorithms

Cloud & Edge Analytics

Advanced analytics for actionable insights

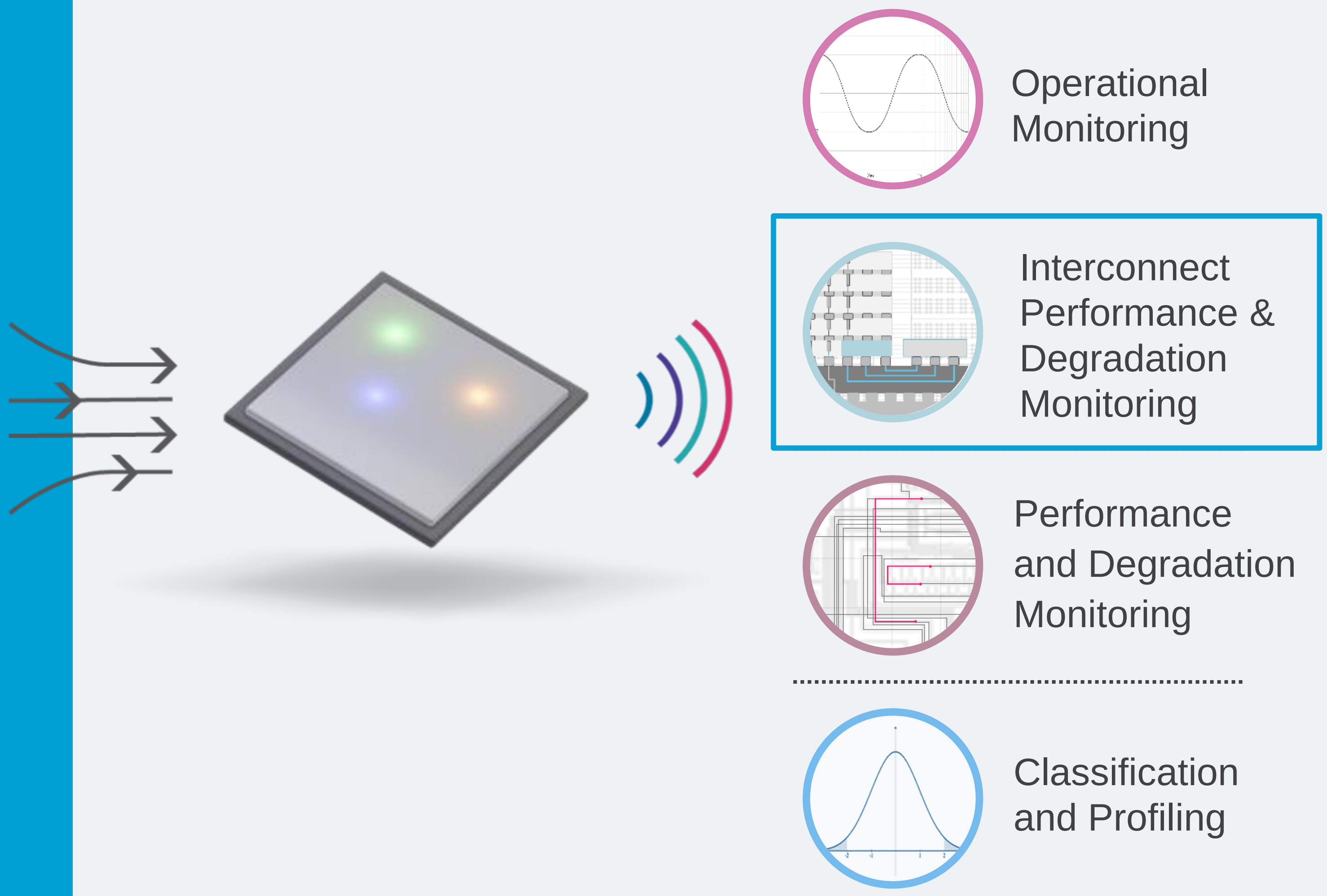
Automated insertion tools

Universal Chip Telemetry™ (UCT)

28nm 16nm 7nm 5nm

On-chip Agents

- Parametric measurements
- High coverage & high resolution
- Minimal PPA penalty
- Operate in mission-mode
- Sense the surrounding electronics and applications



Operational Monitoring

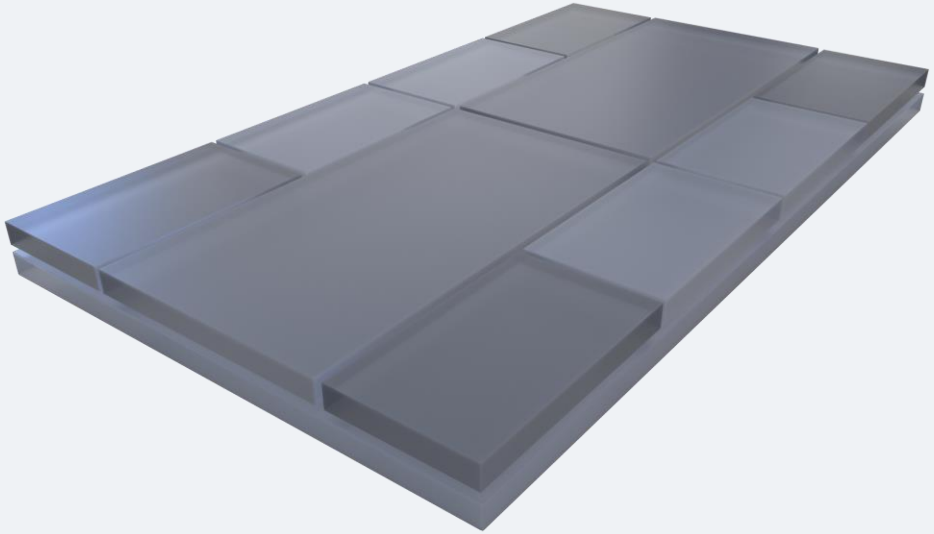
Interconnect Performance & Degradation Monitoring

Performance and Degradation Monitoring

Classification and Profiling

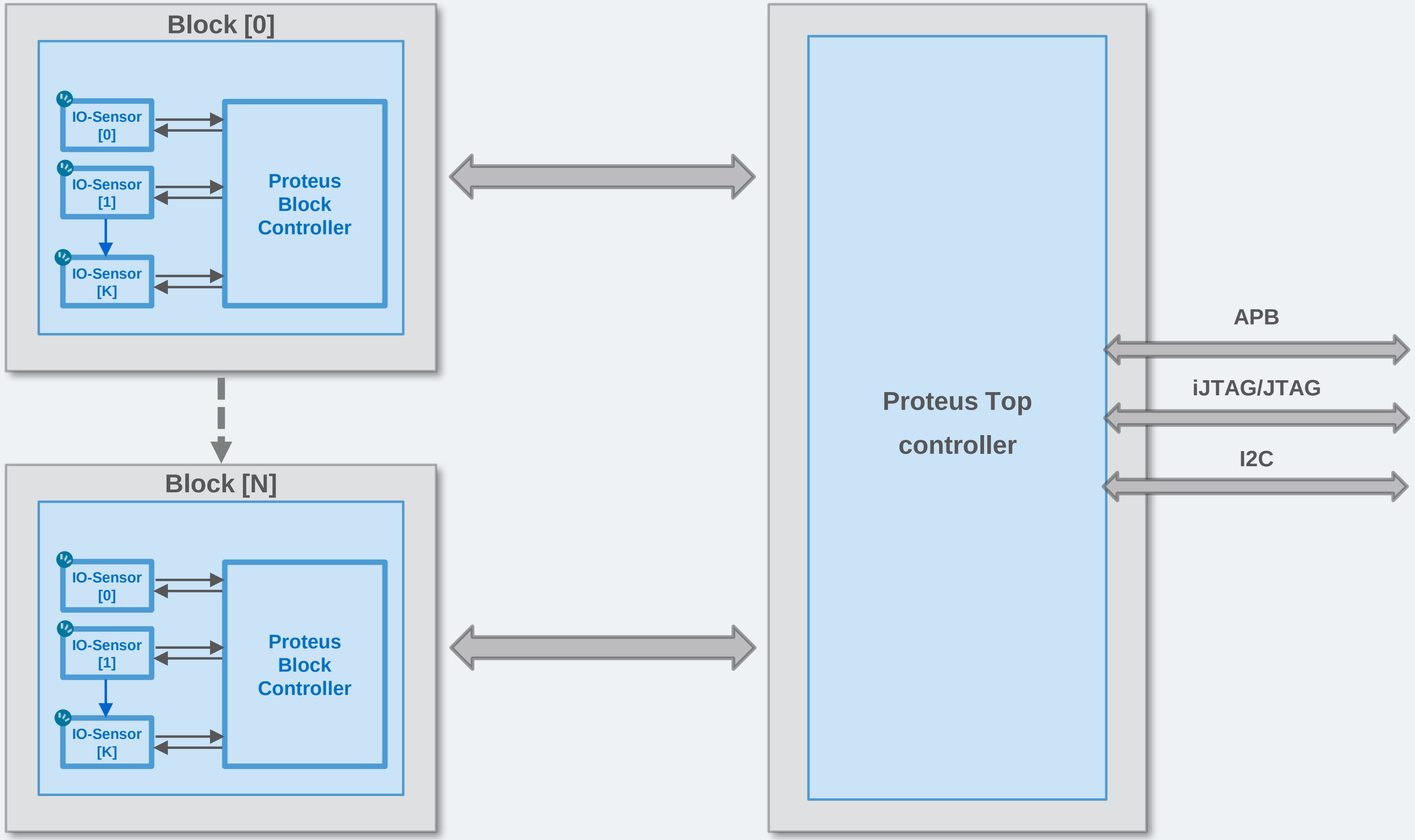
Proteus™ for D2D Connectivity

- General Purpose
  - InFO™, CoWoS™, 3DFabric™, EMIB
  - Glink™, AIB, HBM3, OpenHBI, BoW, and counting…
- Based on ongoing tracking of the signal timing at the receiver (margin to failure)
  - Per lane, in mission mode, and no impact on signal
- Wide speed range: 2GHz (4Gb/s DDR) to 8GHz (16Gb/s DDR)
- Full eye visibility for DDR signals:
  - Setup and Hold to positive and negative edges of reference clock
- Same Agent, all signal types:
  - Rx only, Tx only and Bidirectional
  - Single-ended and Differential
  - Single side monitoring (e.g. HBM3) or both



Complete System Level Solution

- Synthesizable RTL for simple IC integration
- APB standard bus interface to Host CPU
- JTAG and I2C interfaces for external control



Introducing Proteus™ Platform

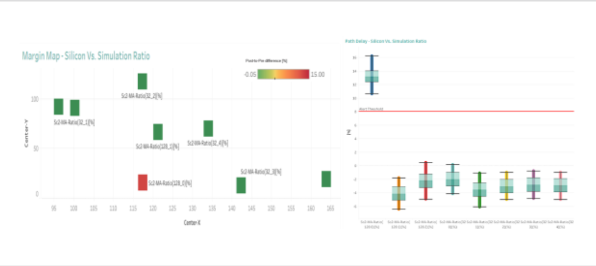
Health & performance monitoring has never been easier

Flexible, easy-to-use and deep lifecycle analytics for advanced electronics

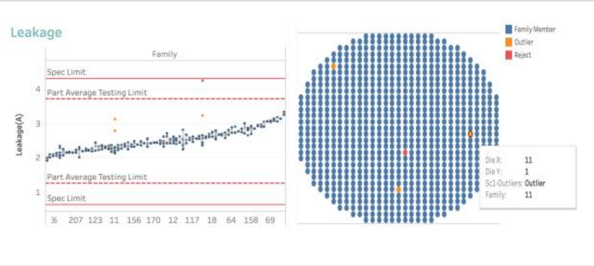
Cloud based, enterprise grade	Cloud agnostic technologies | Secure and robust | Scalable for big data
OOTB targeted solutions	Machine learning | Actionable insights | Dashboards and alerts
Open for innovation	SDK enabled | DIY ML Ops development | Customizable data delivery
Open for integration	Multiple data sources | Automated feedback deployment | API integration
Actionable at edge	Insights on edge devices | Near real time | Minimal footprint

Proteus
Targeted Analytics

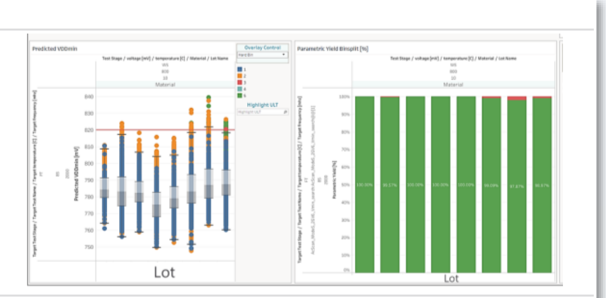
Chip Production



Fast Ramp-Up with Higher Confidence



DPPM Reduction



Shift-Left Decisions

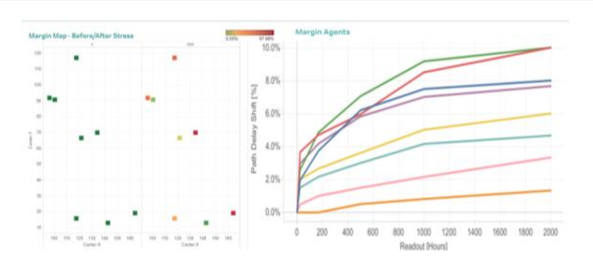
System Production

Correlation Between Value Chain Stages

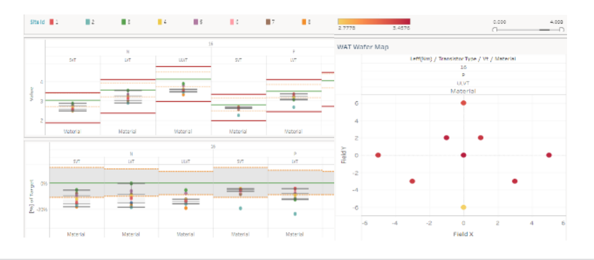
Power Optimization

System & Application Optimization

In-Field



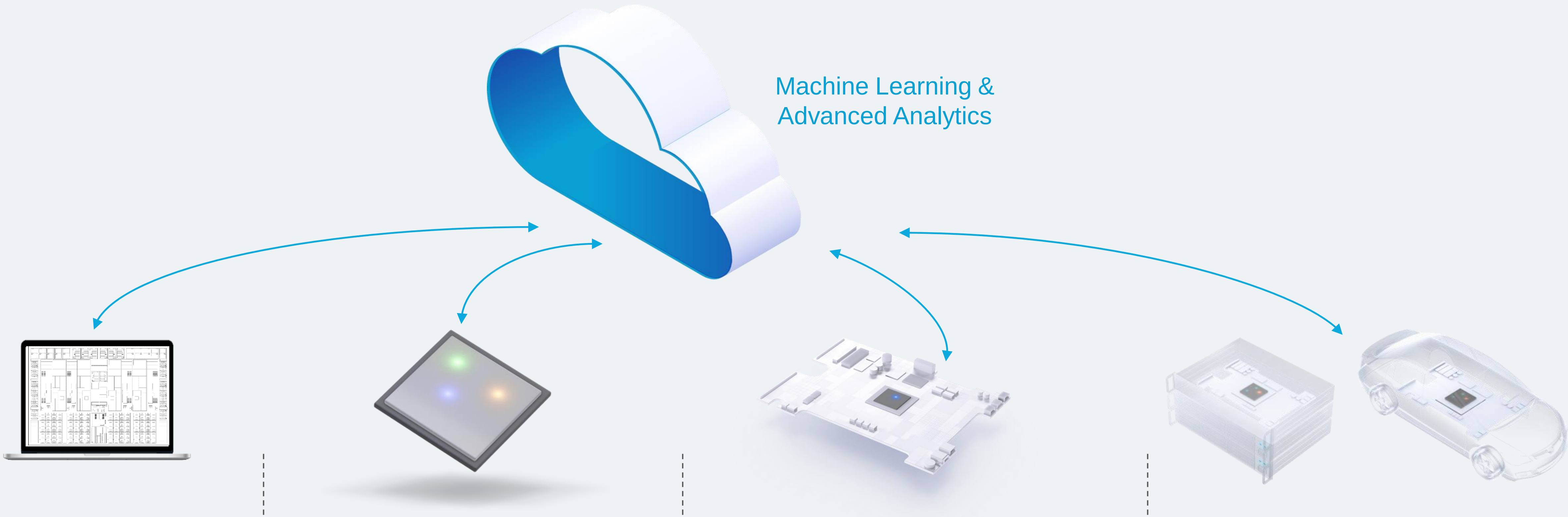
Predictive Maintenance



Predictive Functional Safety

RMA Reduction with Fast Time-to-Resolution

Actionable Common Data Language



Machine Learning &
Advanced Analytics

Chip Design
Design simulations

Chip Production
UCT measurements

System Production
UCT measurements

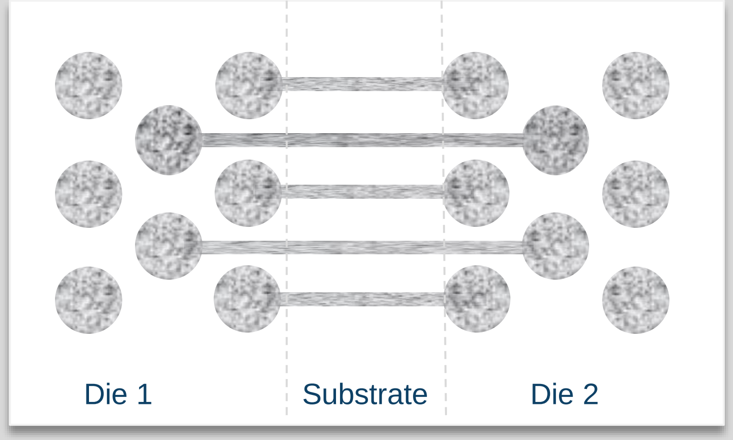
In-Field
UCT measurements

Use Cases & Capabilities

Providing Visibility of Lane Integrity

BKM

Pass/Fail



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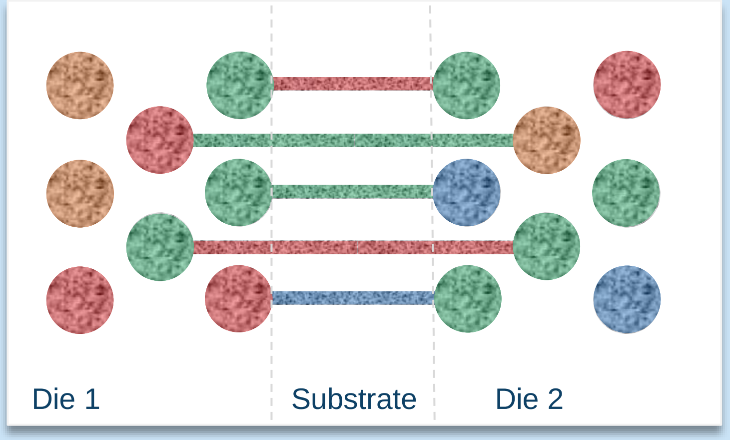
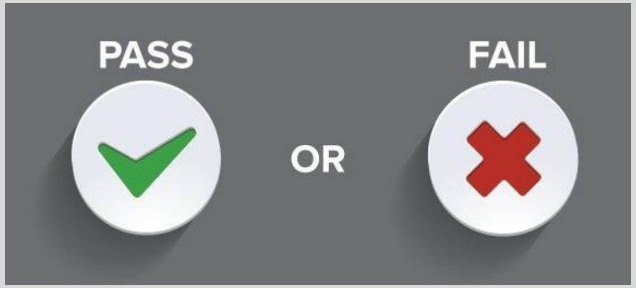
Lane Grading



- **Signal integrity grading**
- **Performance grading**

High Coverage New Product Introduction

BKM



- Go / No Go
- Worst case margin per group
- Low coverage, low volume
- Time consuming
- Labor intensive

Low visibility → Low confidence

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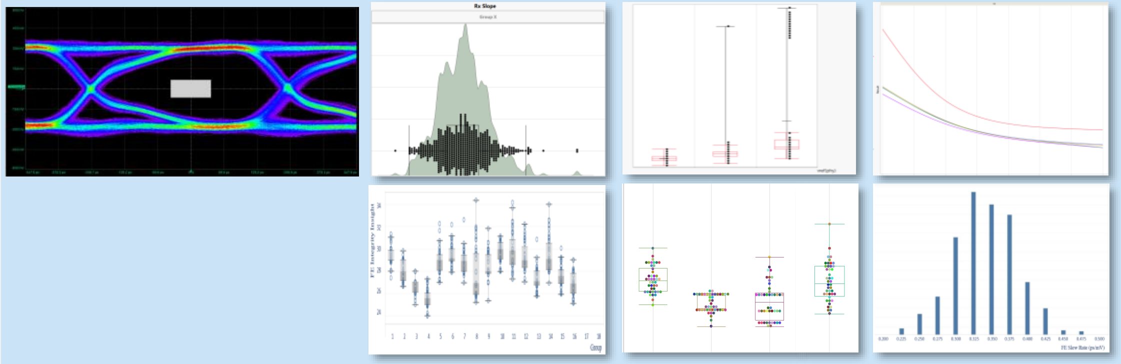
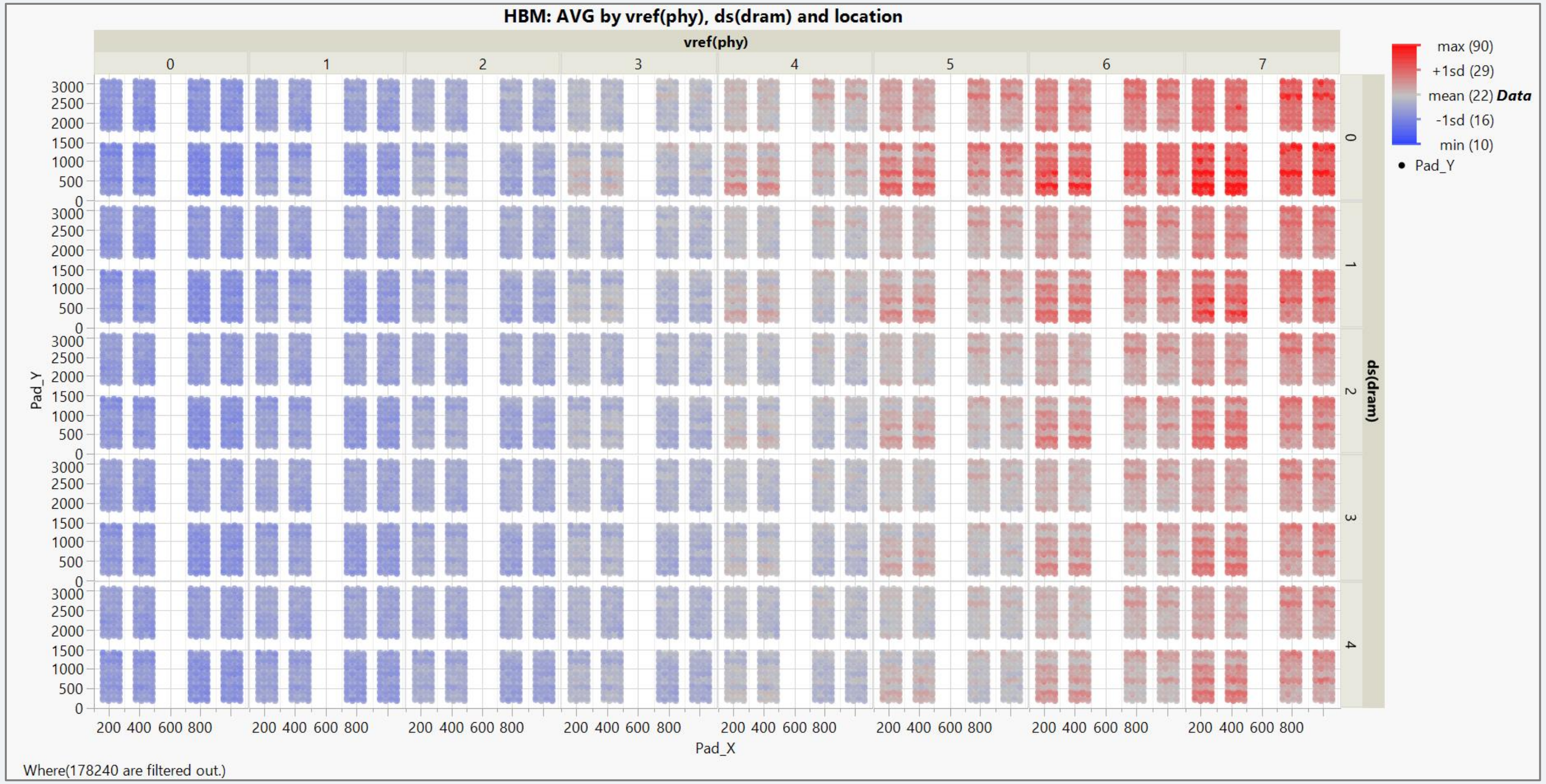


- Parametric
- Full eye visibility per pin
- All pin coverage
- Fast, immediate, during standard test
- Analytics at the click of a button

High visibility → High confidence

Silicon Proven: Lane Grading

Per pin signal quality map*:

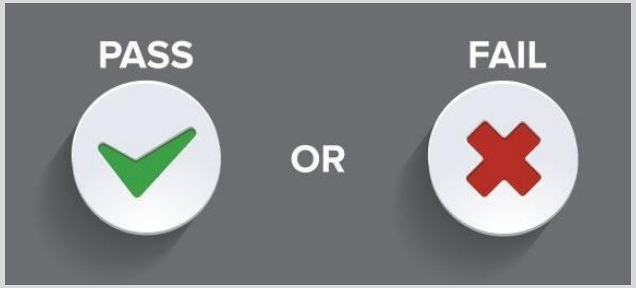


* CoWoS lines were intentionally routed beyond their spec limits

Measured in GUC's 5nm HBM2E 3.2 Gbps Test Chip

Parametric Volume Manufacturing Screening

BKM



Risk of quality escapes

- Go / No Go
- Worst case margin per group
- No correlation to other chips

Low visibility → High DPPM

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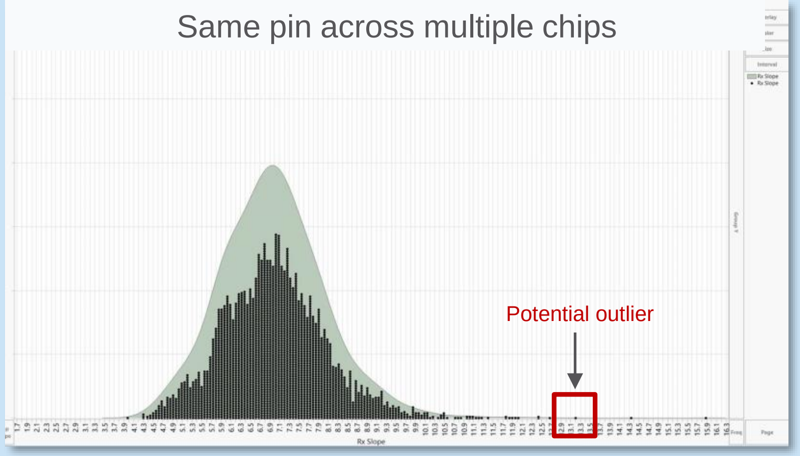


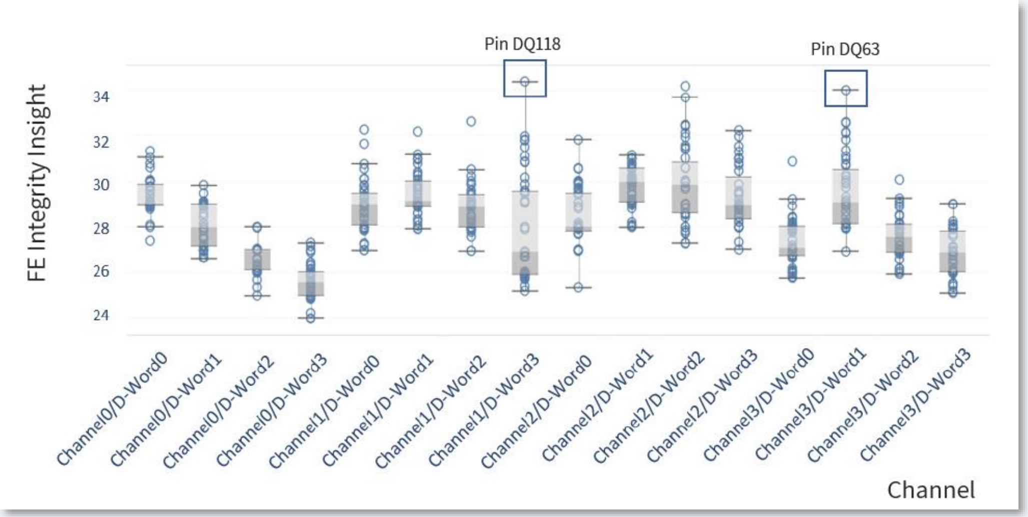
- Parametric
- Margin per pin
- Correlation of entire chip population

High visibility → Low DPPM

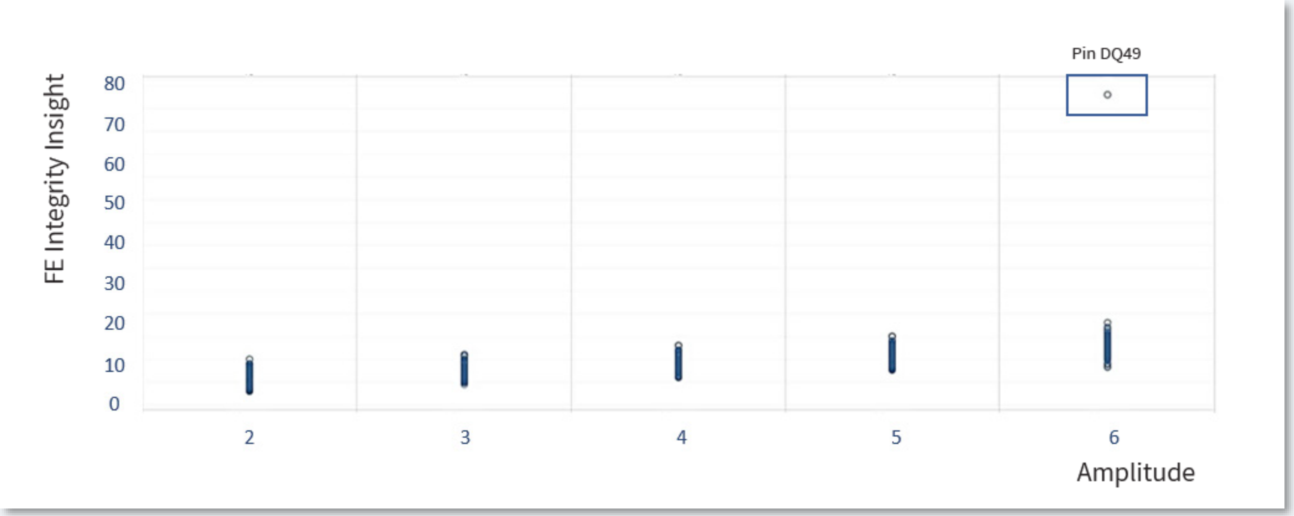
Silicon Proven: Outlier Detection*

- Lane degradation monitoring and repair at test
- Based on Rx slew rate

Far-End Integrity Insight per Channel and Pins in Channel



Rx Signal Amplitude at Pin

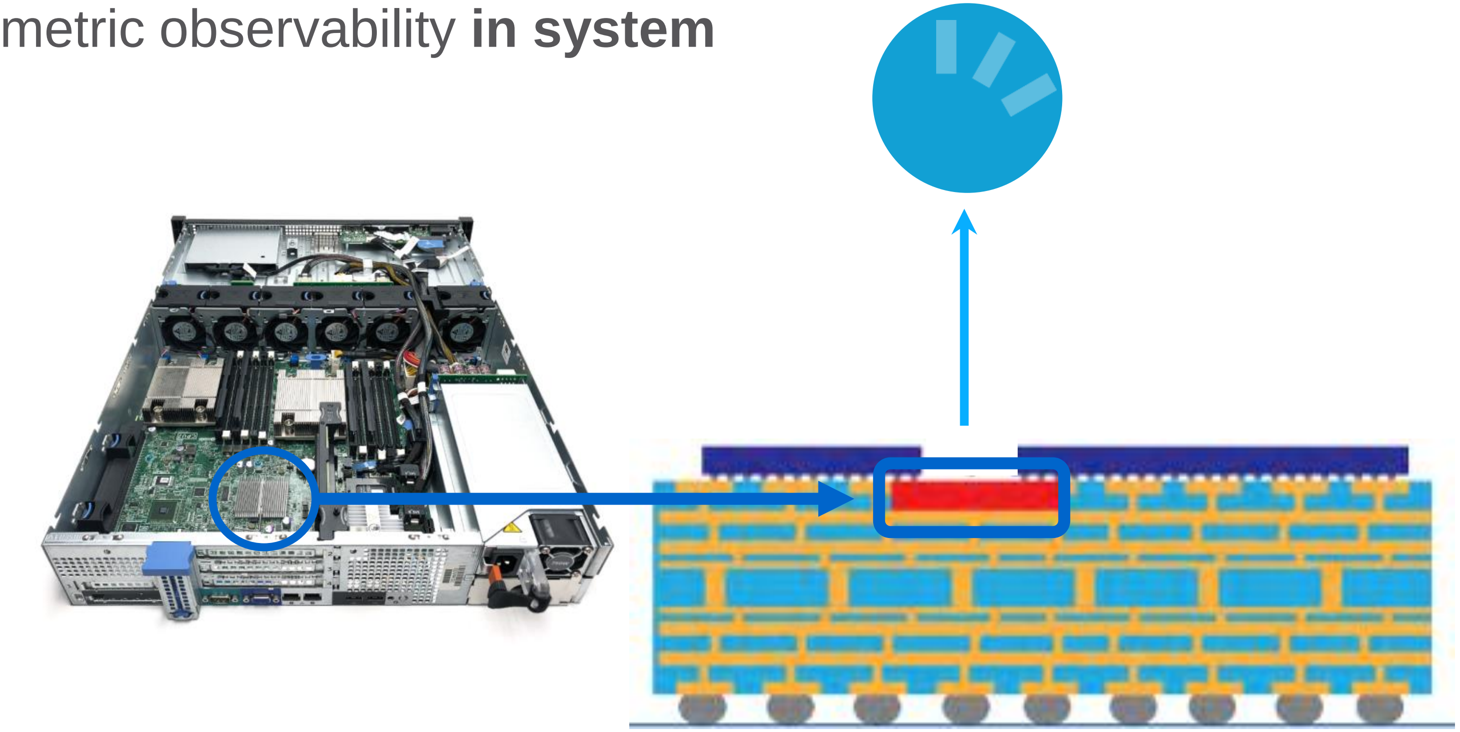


Measured in GUC's 7nm and 5nm HBM2E 3.2 Gbps Test Chips

* CoWoS lines were intentionally routed beyond their spec limits

In System Connectivity Visibility

Parametric observability **in system**



No impact on measured signal

In-field Degradation Monitoring & Predictive Maintenance

BKM

Who owns the problem?

- Risk of failures in field
- RMAs / epidemics

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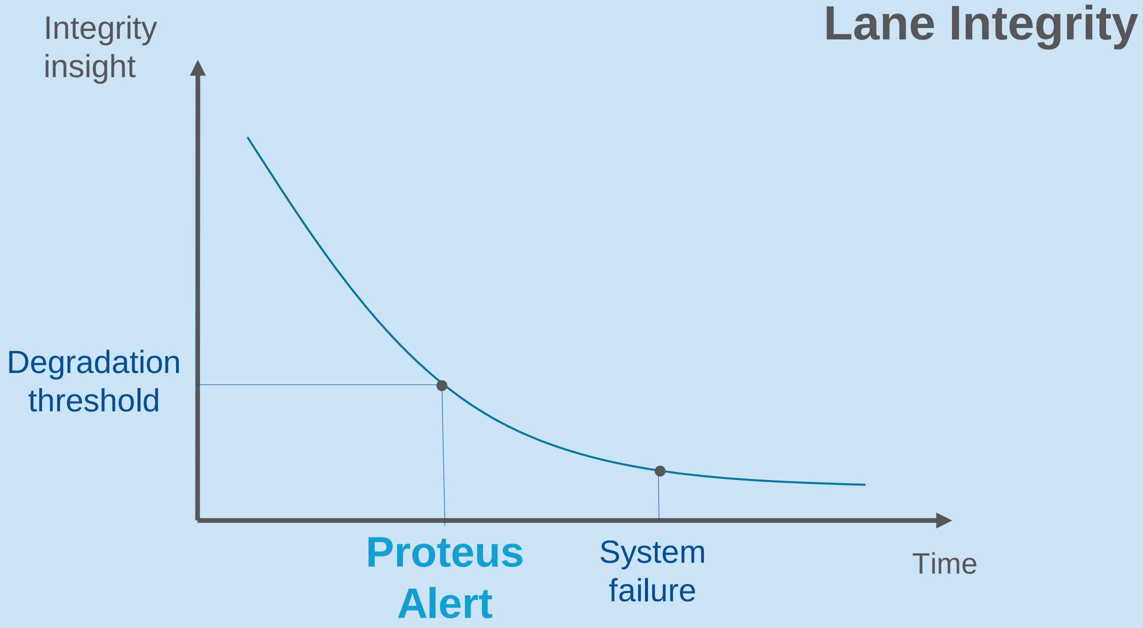
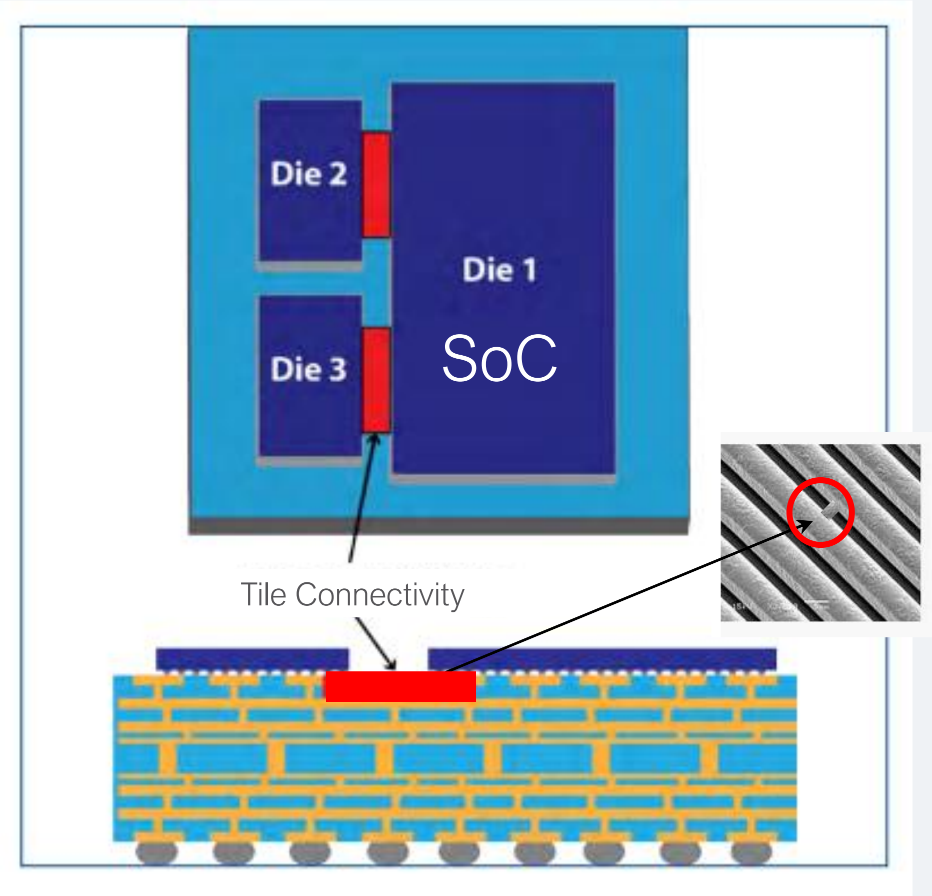
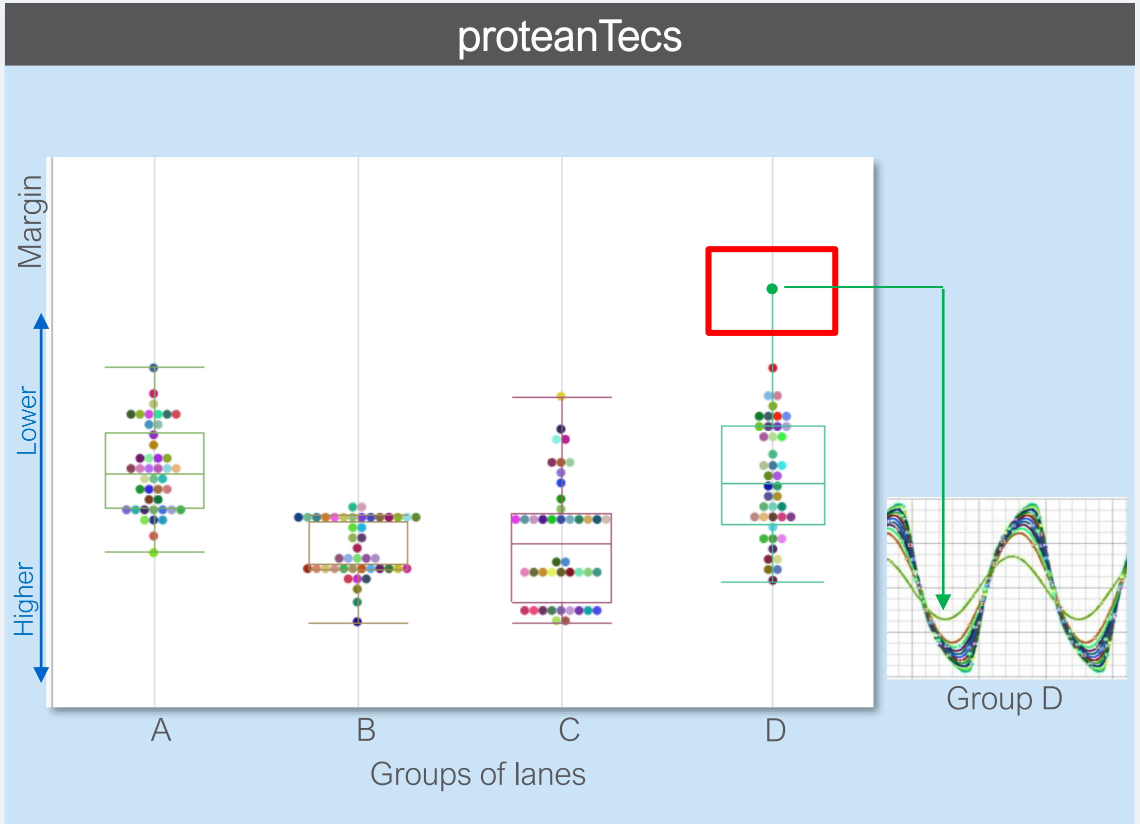


- Predictive maintenance
- Alerts on faults before failures
- In mission mode!

Lane Integrity in Lifetime Operation

Shorts start to develop between lines over time

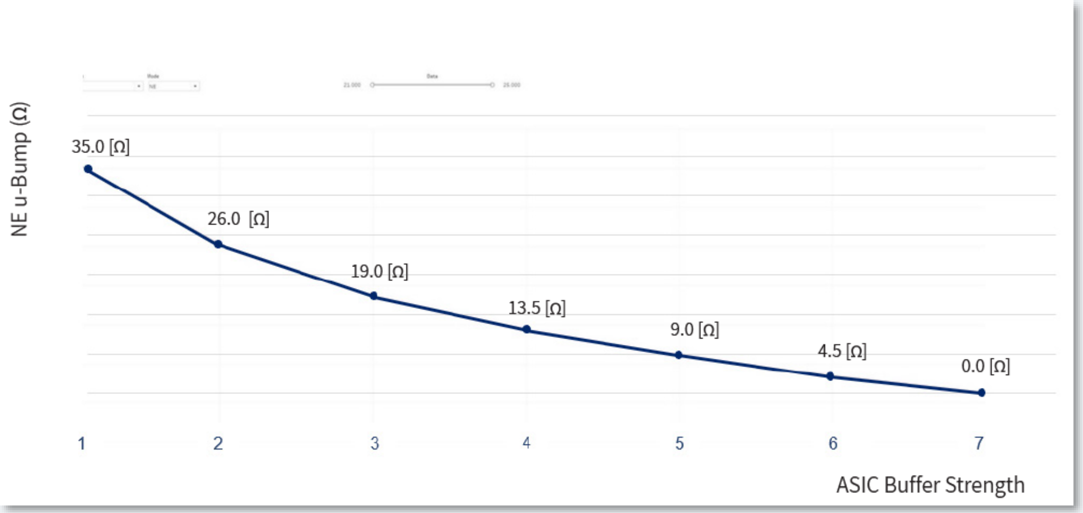


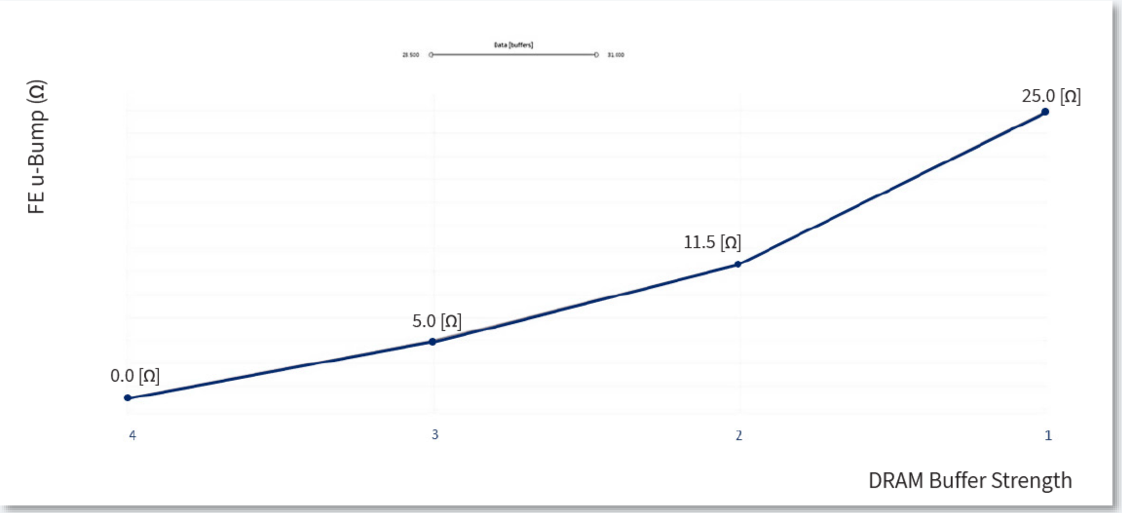


- **Lower margin detected in one of the lanes in group D**
- **User is alerted on degradation prior to system failure**
- **Lane is replaced with a good lane**

Silicon Proven: Degradation Monitoring

- Lane degradation monitoring and repair, in mission-mode*
- Based on near-end and far-end integrity insights





Measured in GUC's 7nm and 5nm HBM2E 3.2 Gbps Test Chips

* ASIC buffer strength intentionally weakened to emulate u-bump resistance change

A Complete Solution for Lifecycle Visibility

NPI

Accurate per-pin characterization

- Parametric measurements per-pin
- Eye diagram visualization
- Manufacturing limits setting during NPI

Production

High confidence production testing

- Parametric outlier detection per-pin
- Identify marginal pins candidate for spare lane swapping as early as Final Test
- Early alert on manufacturing line pandemics

In-Field

Uninterrupted service availability

- Continous per-lane health and degradation monitoring in mission mode
- Alert on threshold crossing before system failure
- Allows for proactive lane repair or whole module swap in the field

Thank you.

www.proteanTecs.com

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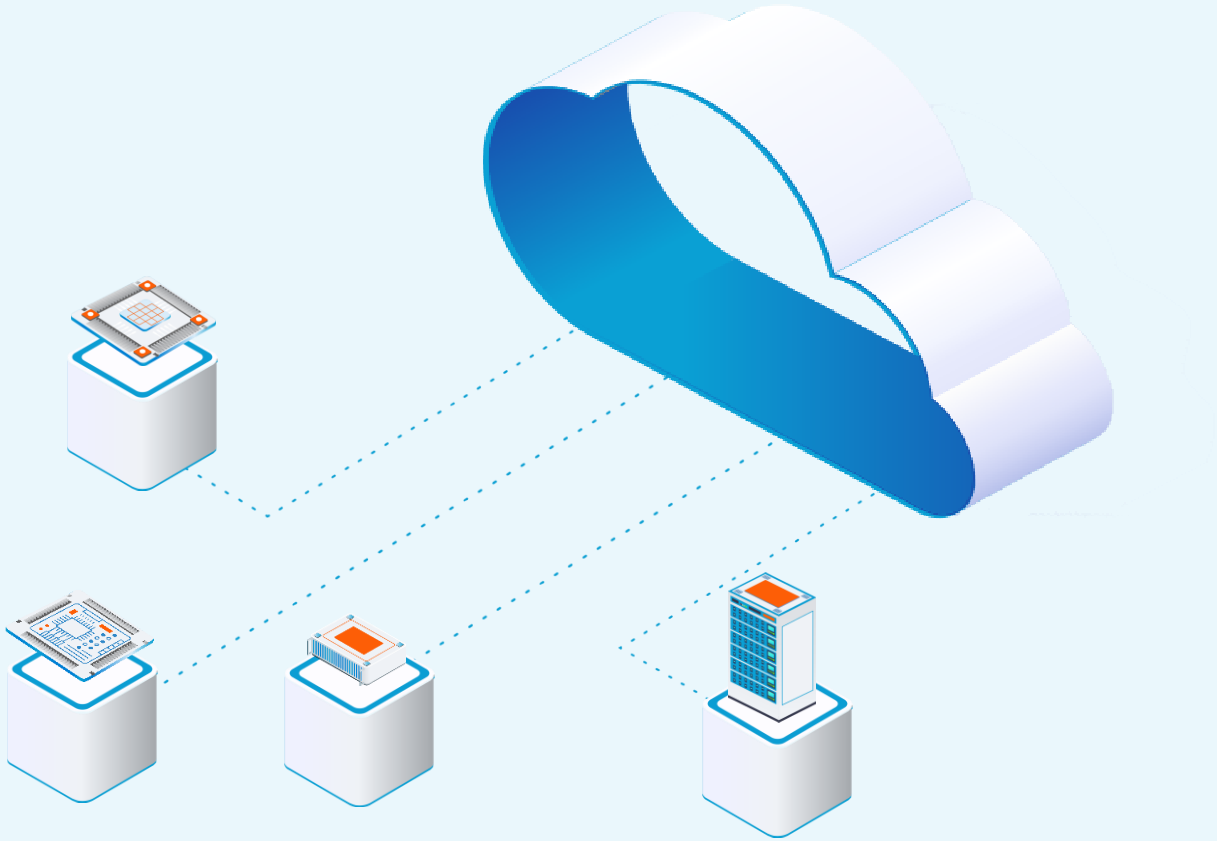

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>
> — **Risto Puhakka**, President VLSIresearch

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