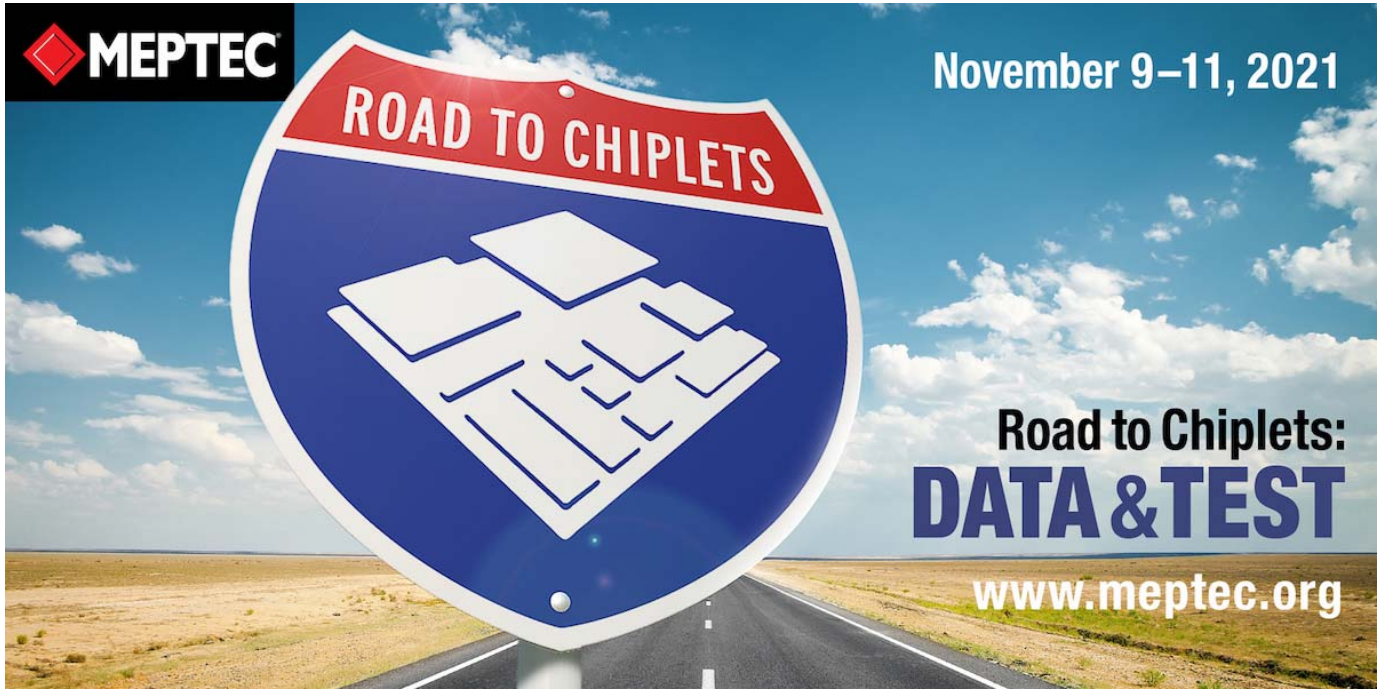

Road to Chiplets: Data & Test

November 9 - 11, 2021

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ML in Semiconductor Test
(A "Balanced Approach")

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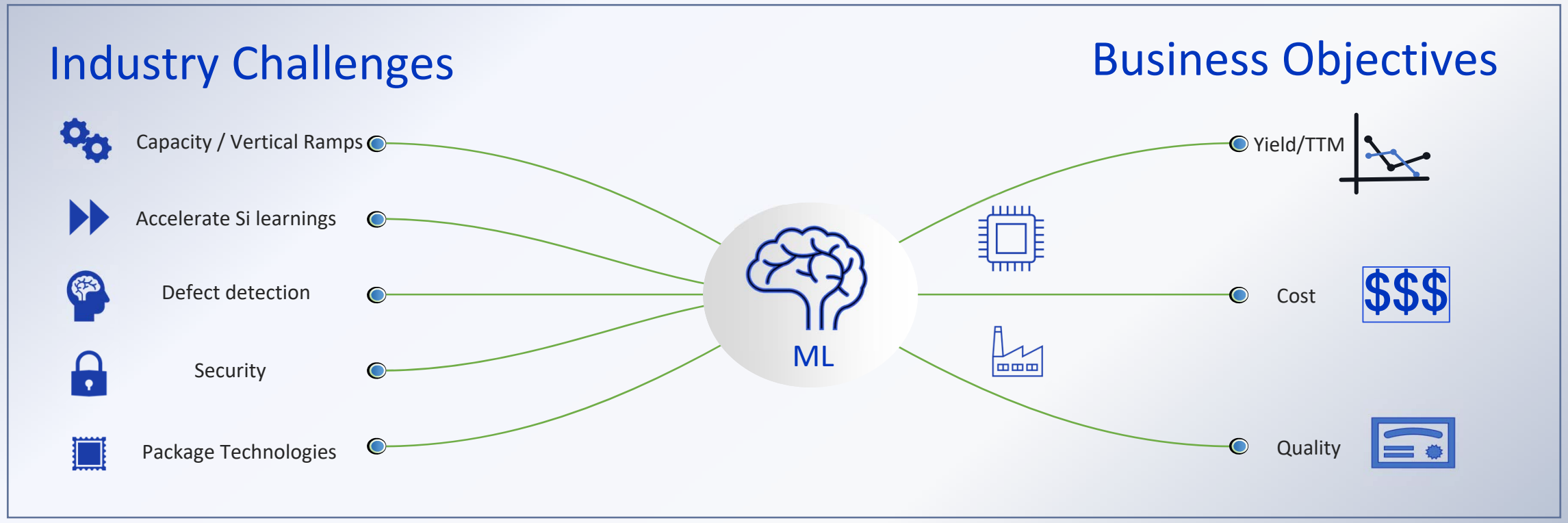
Qualcomm Technologies, Inc.

Outline

- Today's Challenges
- Existing and newly adopted test capabilities
- Offline & Test Case example
- Online and Test Case Example
- Tomorrow's opportunities
- Conclusions

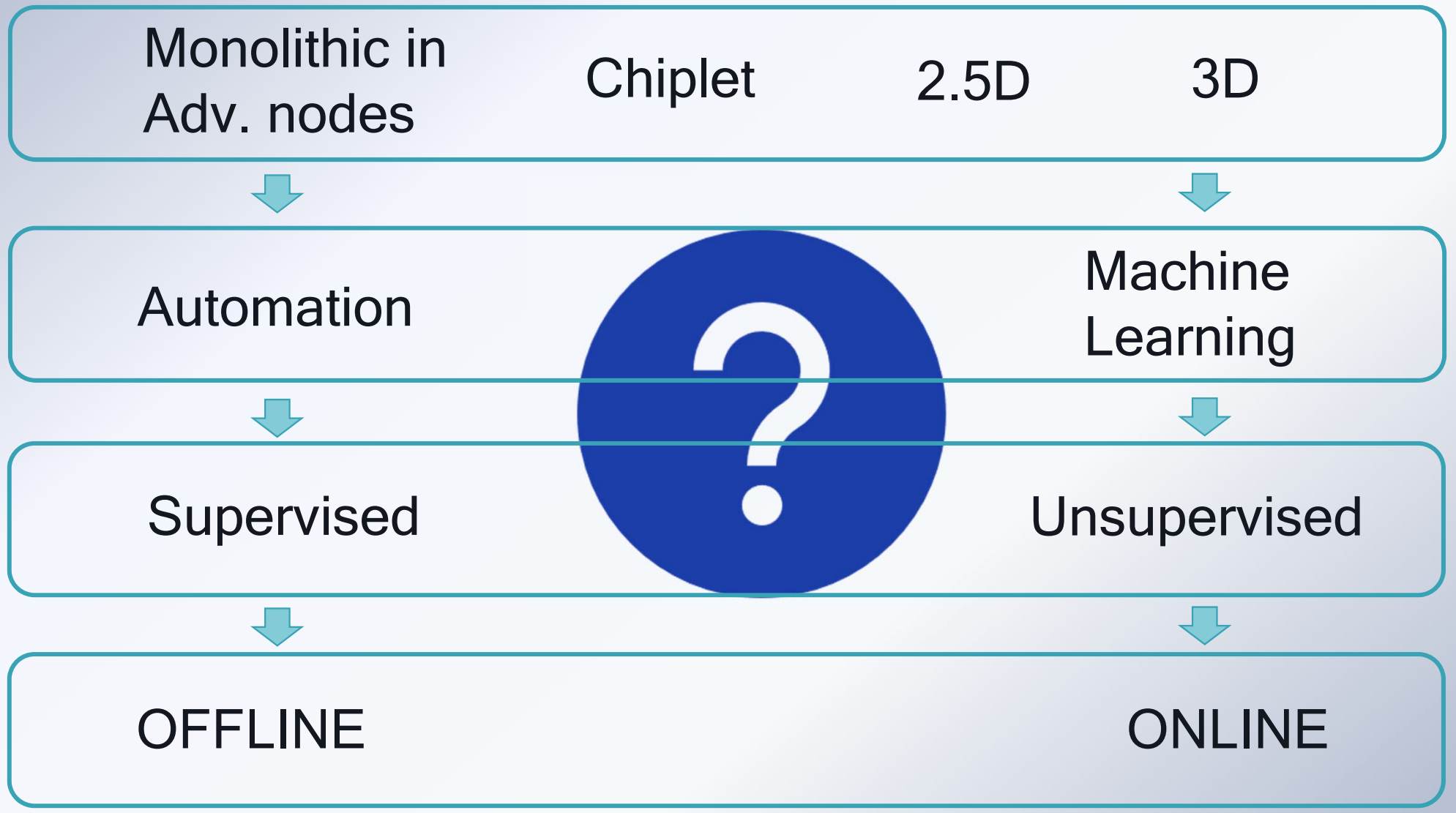
Semiconductor Challenges - Overview

Can ML at the SOC level help address Business Challenges at the Chiplet Level?



- Advanced Analytics & AI development will be significantly relied upon to accelerate the validation

Semiconductors' continuous evolution strategies



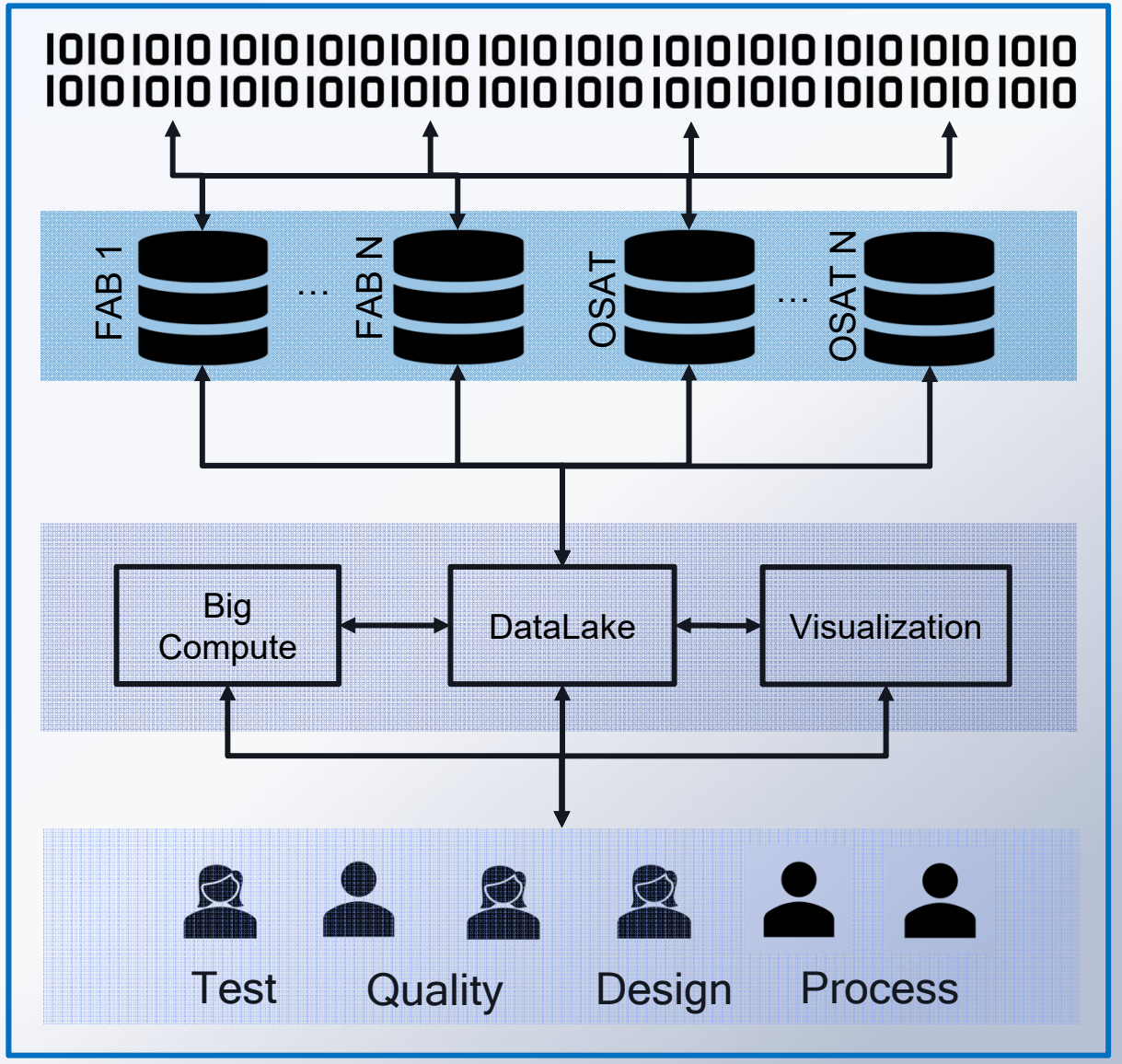
What's available: Offline Infrastructure

Benefits:

- ✓ Flexible compute power
- ✓ Scalable to multiple users / locations
- ✓ Secured
- ✓ Optimal for Training and Learning tasks
- ✓ Enables visualization & analysis tools
- ✓ Easy deployment of ML Models

Limitations

- ✓ Large Latencies (secs/min/hrs/days)
  - On-The-Fly inference – High Cost impact
  - Latency is directly proportional to the complexity
  - Latency is directly proportional to # of models
- ✓ Security:
  - Not a Zero-Trust solution for production



The Offline Case: Lot Disposition Assistant

Loc

Assisted Disposition: ML and Automation Improved Product Quality and Operational Efficiency

- Improved disposition time by 10x with >95% accuracy
- Consistent performance on matured technologies nodes
- Enables test team with potential causes on the abnormal parameters

Trigger Criteria

- ✓ Low Yields
- ✓ High Test Times
- ✓ Abnormal Binning (SBL)

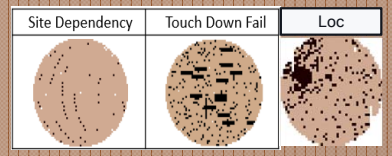
Potential Cause

- ✓ Setup
  - HW
  - Contact
- ✓ Process
  - WAT
  - Performance
- ✓ Design
  - New corner cases

Validation

Automation:
- ✓ ANOVA of Test Cell
  - ✓ SAT, FAB, Vendor, etc.
- ✓ ANOVA of HW (PC, LB)
  - ✓ Site, vendor, etc.
- ✓ Abnormal Lot Stats Analysis

ML – Wafer Pattern Recognition



Actions

- ✓ Disposition actions:
  - Retest
  - Scrap
  - **Ink off** (special patterns)
  - Put on hold
  - Release
  - **Unknown**
- ✓ Correlation to WAT params
  - Parametric
  - **Spatial** (special patterms)
  - Binning

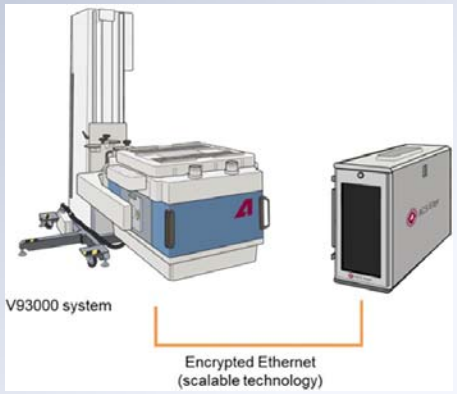
Multiple permutations over time

Automation + Machine Learning = Accelerated Benefits

Challenge: Maintenance required over time:

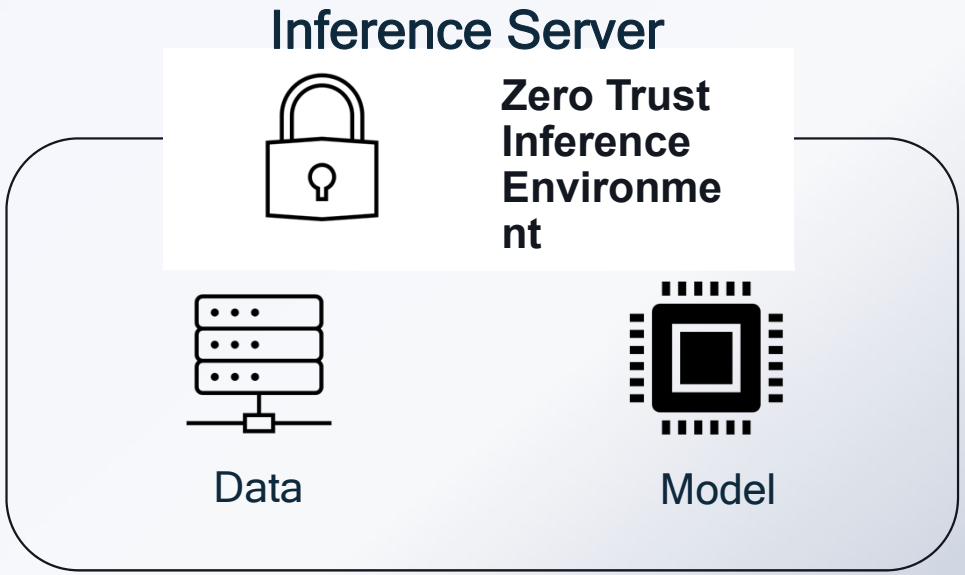
- Train models to include new wafer patterns over time
- Development of new Ink-off patterns to optimize yields

What's getting adopted: Online Infrastructure
ATE's Inference Server



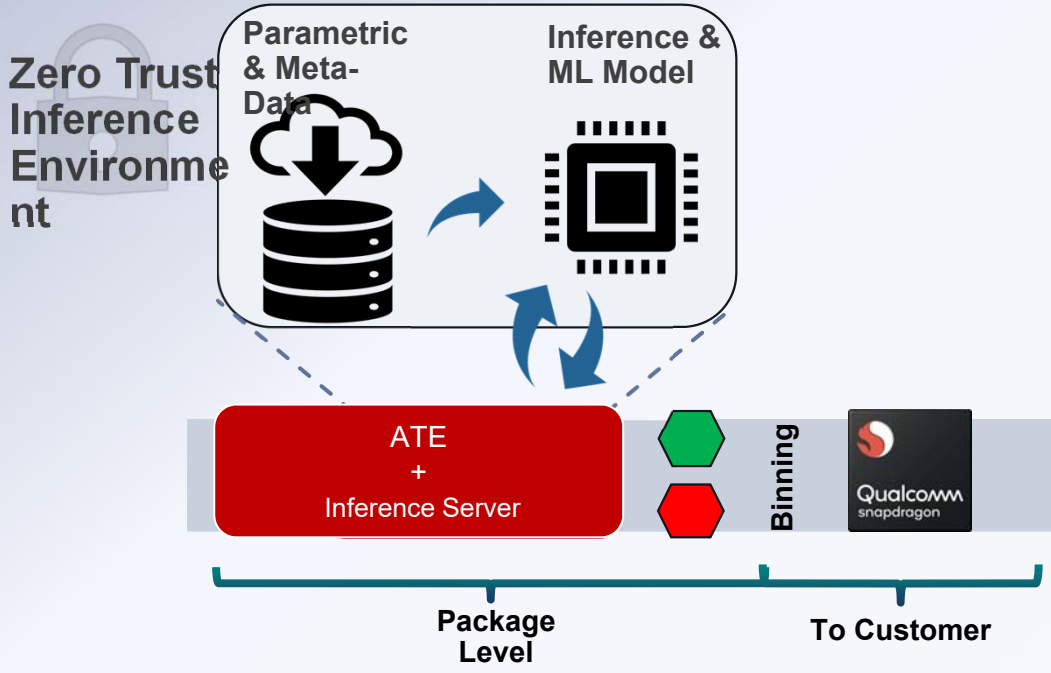
Benefits:
- ✓ On-the-Fly ML Scoring /Decision Making
- ✓ Zero Trust Environment approved
  - Secured ATE Communication (Encrypted)
- ✓ Minimum Latencies (uSec/mSec)
- ✓ Easy model integration with test program

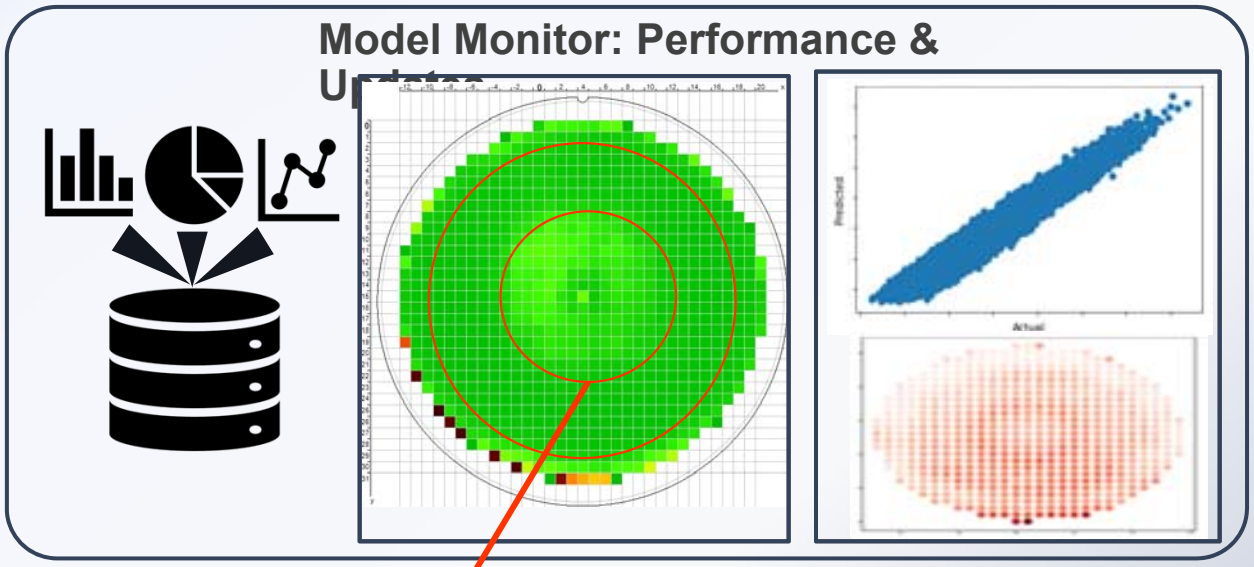
Limitations
- ✓ Limited compute power
- ✓ Must have HW available at FABs/OSATs

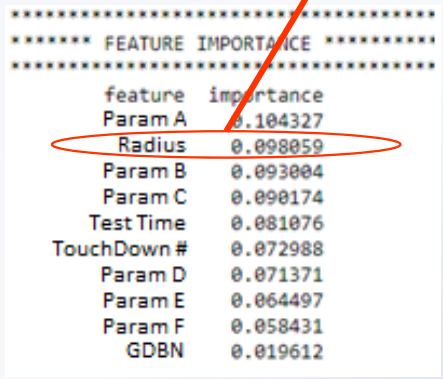


The Online Case: Parametric Predictions

How does it work?







Benefits:

- Param Test reduced by > 50%
- No Quality impact
- Extends beyond ATE APIs
- Can run multiple models in same project
- Identify performance matching ICs
- Negligible TT overhead

Limitations:

- Scalability of Inference HW over FAB /OSAT
- Limited adaptation over time

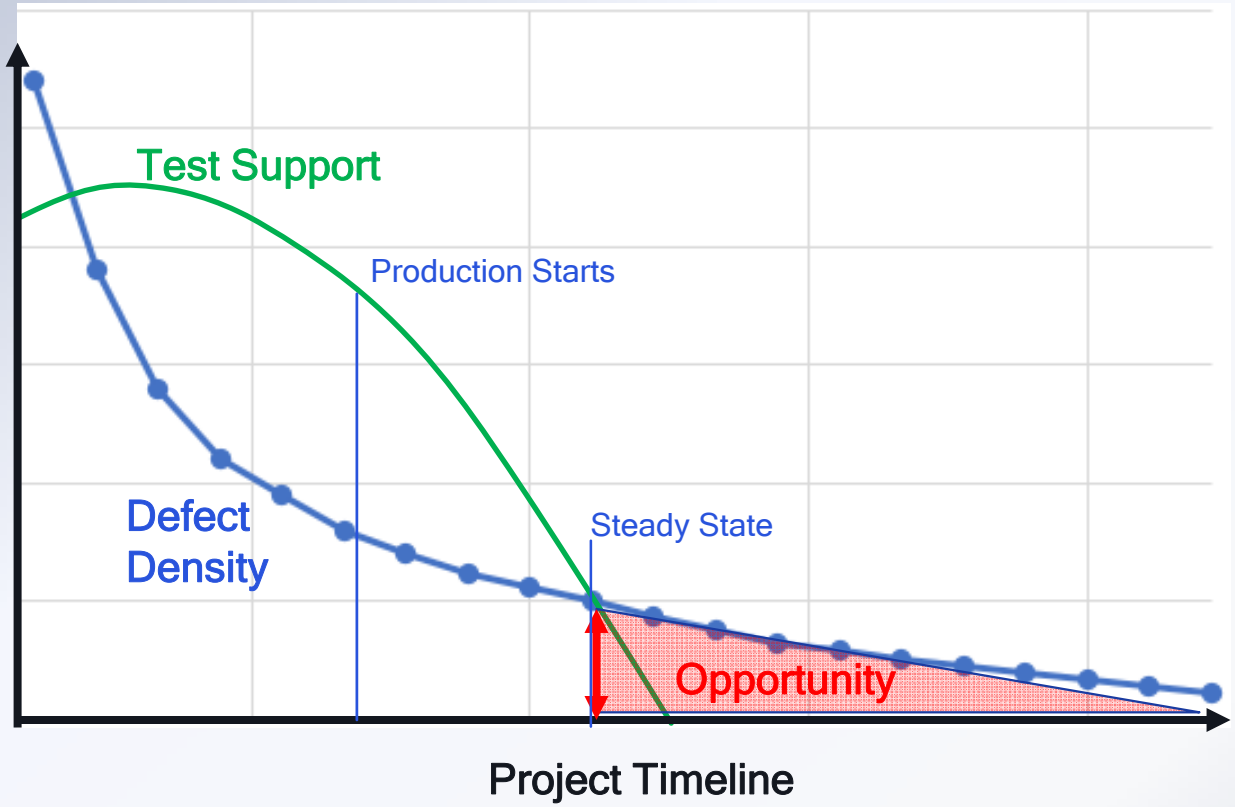
Offline Compute

Re-Train and Development of Improved ML model

The constant challenge: "Capable to adapt over time"

What we know:

- Process improves over time
- Test development support is limited during Steady State
- Chiplets, 2.5D or 3D may extend the tail end of the curve



Variance contributors

- ❑ **Cross Operations**
  - Fabrication
  - Probing
  - Package & Assembly
  - Package Test
  - Multiple SATs
  - Multiple Test Cells
- ❑ **Power/Thermal**
  - Process Monitors
  - Thermal Sensors
  - Wafer location aware
  - Defectivity aware
  - Setup aware
- ❑ **Process**
  - Defect Density
  - Binning trends
  - Yield Trends
  - Inter-chip defects/performance
  - Fablot Condition
- ❑ **Defect Detection**
  - Structural
  - Functional
  - Memory
  - Analog
  - RF

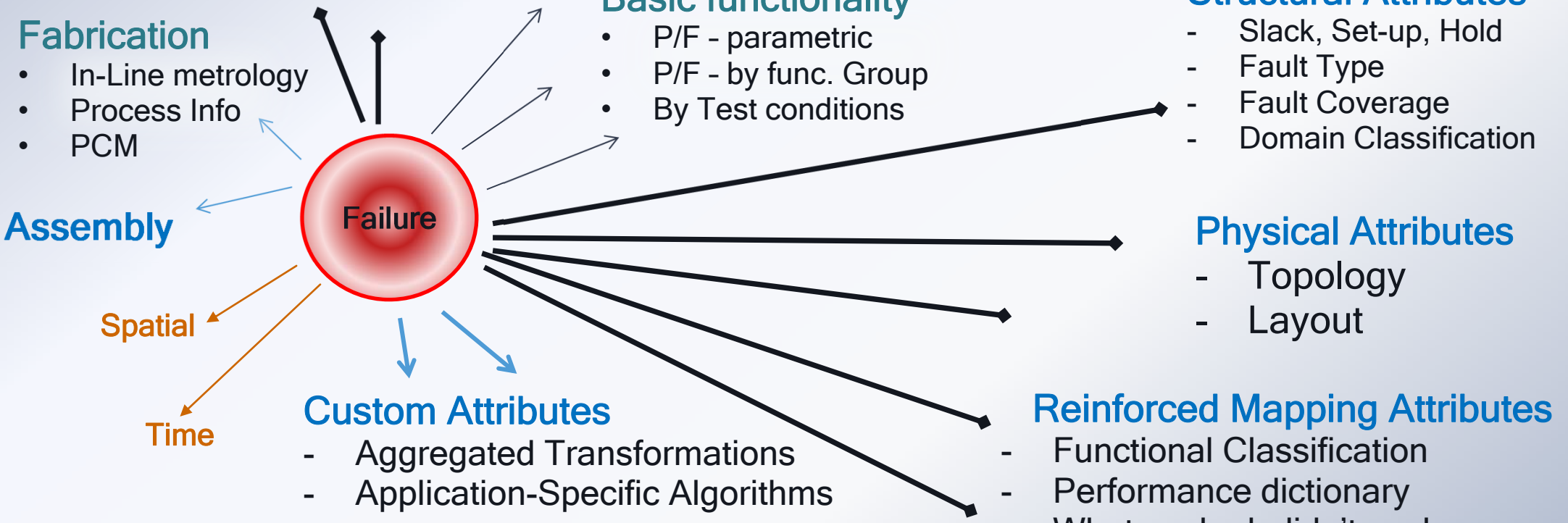
How to enable adaptability in our ML models?

Capture Variances with Higher Dimension Datasets

Collaboration across all disciplines → Strong Failure Signatures

Aggregated Reactive Attributes
- Failure Analysis
- Customer Returns
- Quality Excursions

Enhanced Test Data at all Test Operations
- Common Test Attributes across Wafer, SOC & Chiplet
- Test Attributes of both Good & Bad Device



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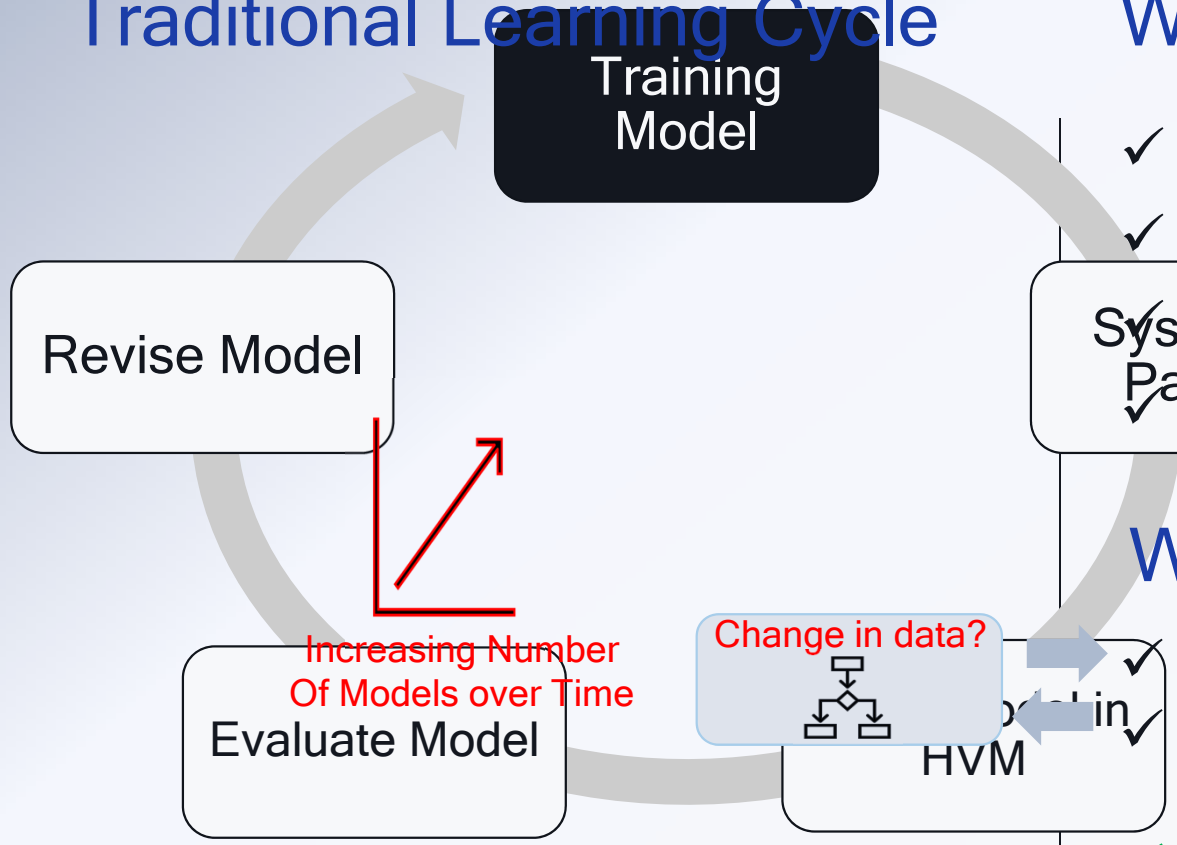
Today's Strategy – tomorrow's opportunity

Traditional Learning Cycle



What we do TODAY:

- ✓ Use of supervised learning to create models
- ✓ Use of unsupervised learning to explore data
- ✓ Heavy reliance in OFFLINE Infrastructure
- ✓ New models to replace old models over time

What we need to do TOMORROW:

- ✓ Include Higher Dimension Data Sets
- ✓ Develop hybrid models to adapt over time
  - Supervised + Unsupervised
- ✓ Adaptable models by taking advantage of
  - Automation,
  - Online & Offline compute HW

In the Not-So-Distant Future

Dimensionality

Adaptability
Hybrid Learning

Application
Environment

Existing Data Sets
(Baseline Features)

Un-Supervised
Learning

OFF-LINE
TEST

Higher Dimension Dataset
(Exploratory Features)

Supervised
Learning

ON-LINE
TEST

In Conclusion:

WHAT IS an extension of today's methodologies:

- Increased adoption of Automation + ML capabilities on Test Engineering
  - Accelerate learnings w/process, package, etc.
- Reuse of sensors (+ New DFT) to analyze the impact of new package, process, design, d2d I/F, etc.
- Reuse of traditional SOC ML techniques applied to 2.5D, 3D & Chiplets products.
- Parallel paths for Supervised (Fast Execution) and Unsupervised (Fast Discovery) on-the-fly models

WHAT WILL be the next generation methodologies:

- Development of application specific sensors on HW from initial analysis / debug findings.
  - EDA + ATE → Connecting Pre-silicon (planning) with Post-silicon (actuals) environments
- Chiplets, 2.5D & 3D will require new features to capture defect variances and adaptation over time
  - Data Vendors → Minimum to no delay data transport time across test insertions
- ML HW test cells to offer a "Smart" cell environment
  - ATE → Enable continuous learning and adapting capabilities ON-THE-FLY w/o impacting throughput
- Implementation of Hybrid Models to speed up exposure of new defects / performance degradation
  - Across several TBs of data / day

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