

Road to Chiplets: Data & Test

November 9 - 11, 2021



PDF/SOLUTIONS





Leveraging semiconductor lifecycle data to drive closed-loop and cost-efficient chiplet quality testing Kimon Michaels, Exec. VP

November 11, 2021

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PDF Solutions: Predictive Power for Semiconductor Manufacturing & Test and Electronic Systems

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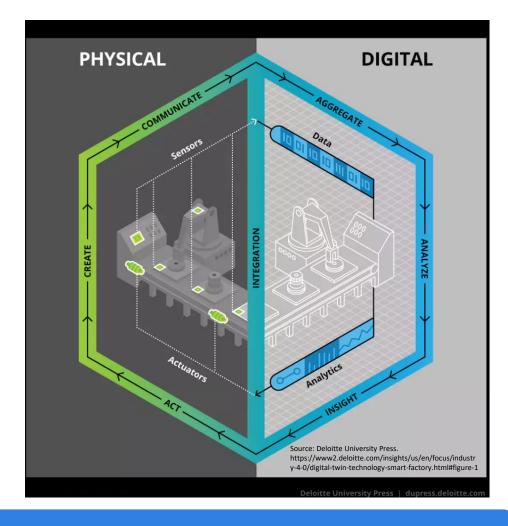
Offices and Support Centers Worldwide



Semi and Electronics Adopting Smart Manufacturing

Digitization drives the realization of Industry 4.0

- Sensors e.g. FDC or cell controllers
- Integration common platform to access data
- Advanced AI/ML analytics at the edge for yield prediction, advanced outlier detection/screening etc.
- Semantic data models to enable digital twins
- Online Control for closed-loop smart mfg. solutions
- Site-to-site connectivity integrating data across the entire supply chain



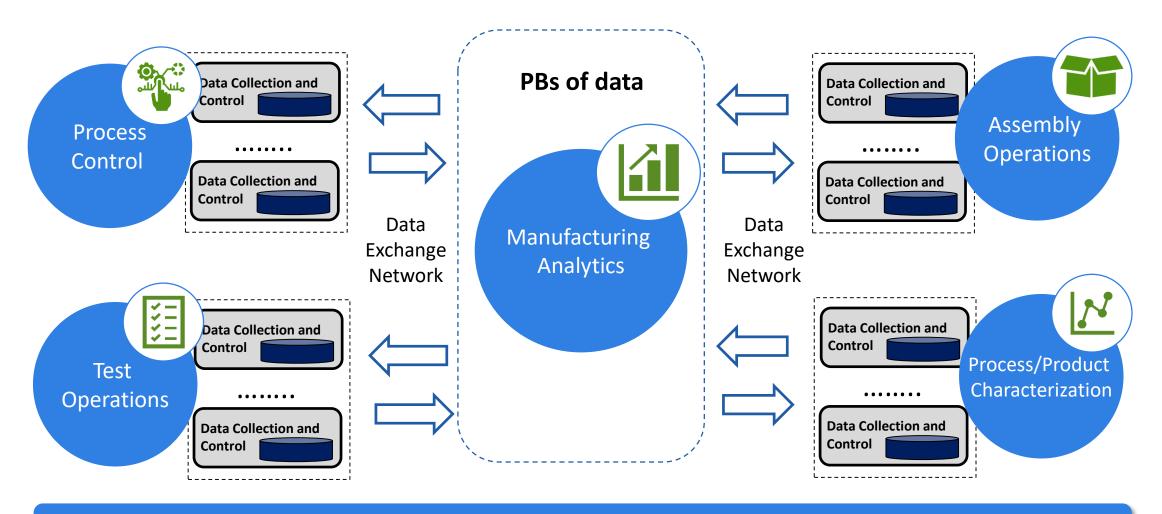
Industry 4.0 is driving digital transformation spanning the Silicon Life Cycle

Leveraging Data Across the Silicon Product Lifecycle

Data Feed Backward: Performance & Variability Optimization | Quality & Reliability Improvement Data Feed Forward: Drift & Excursion Monitoring | Drilldown & Diagnostics **Remote Update and Tool control / Dynamic Decision-Making / Flow Optimization** Instrumentation **Monitoring** WAT, WS Assembly, FT **System** 3D Assy & Design Wafer Mfg **Level Test** In-Field Monitor Test Simulation Wafersort Performance and Performance and Assy and Wafer Fab In-field **Final Test** Reliability data Traceability data Data **Manufacturing** Initial monitor data monitor data data (as avail.) Assy and Traceability All data stored in a semantic data model, ready for immediate analysis **Automated Alerts**, Support for >50 semi data types from the entire product **ML-driven Analytics Actions and** lifecycle for true end-to-end analytics (no data silos) **Supporting Reports**

A semantic data model is essential to support heterogeneous packaging & test

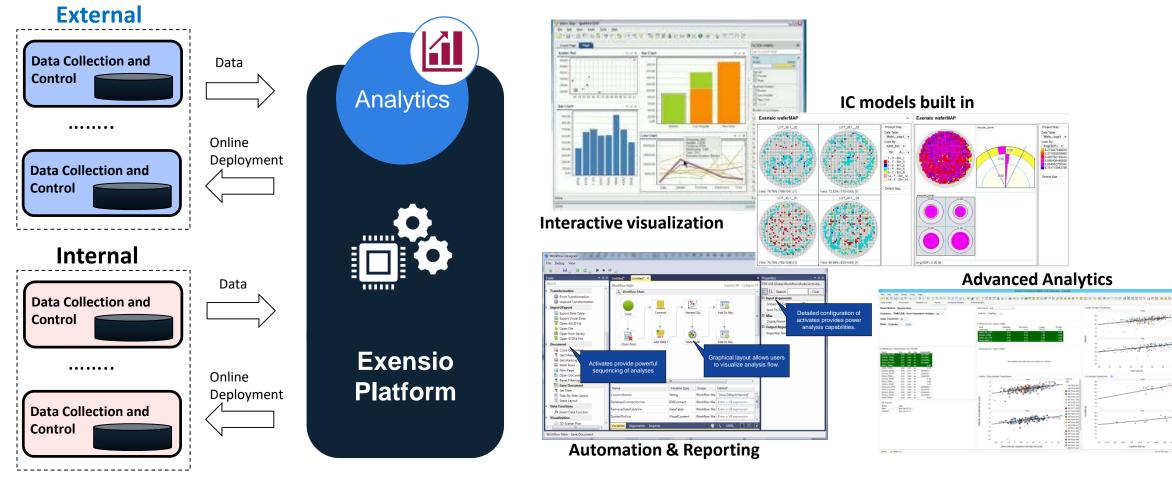
Data Exchange Network to Share Data Across the Silicon Lifecycle



Enabling Data Access for Heterogeneous Test and Packaging



Exensio Platform: Integrating FE & BE Data for Mfg & Test



Powerful signature analysis and diagnostics

Predictive power for the analysis of advanced ICs and electronic systems

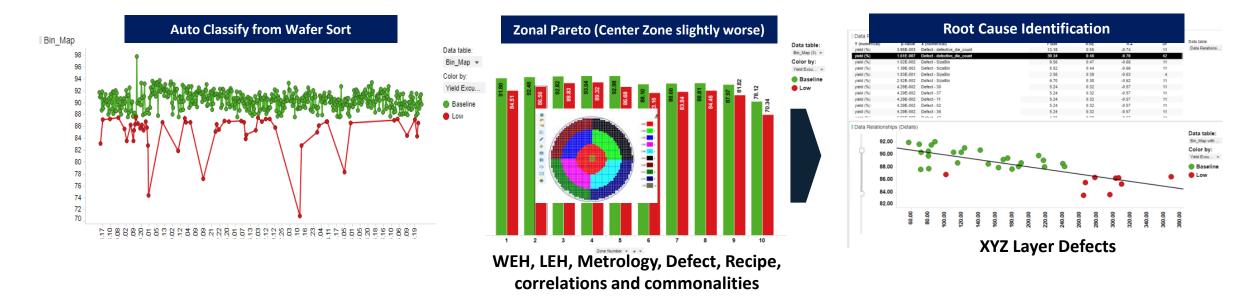


The Need for a "Single Source of Truth" for all Product Data

- Allows companies to integrate their offline AND online systems
 - Use the same data for analytics and actions for test and overall quality assurance
- Enables broader and faster implementation of online actions
 - No waiting for "clean and aligned" data to arrive
- Facilitates "Womb-to-Tomb" product traceability
 - Single die traceability from the fab to test operations to in-field
- Drives creation of closed loop product lifecycle optimization
 - Automated root cause analysis + proactive/predictive OCAP

Start Analysis Early to Catch Problems Sooner

 Identify root cause of excursions faster with auto-analysis and drill down on fab manufacturing data



Automated analysis reduces yield variability and removes human factor

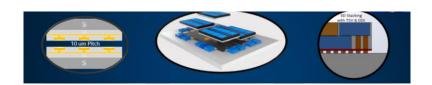


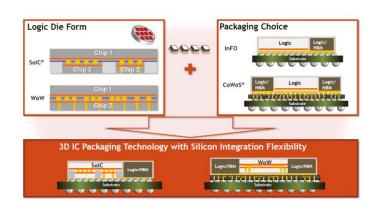
Heterogeneous Integration is a Traceability Challenge

According to an example from AMD*, when comparing a 32-core monolithic IC to 4x8-core chiplet, the chiplet area penalty is ~10%, but the cost savings are ~40%

But what happens if you put 4 good chiplets into a heterogeneous, integrated package, and it doesn't work?



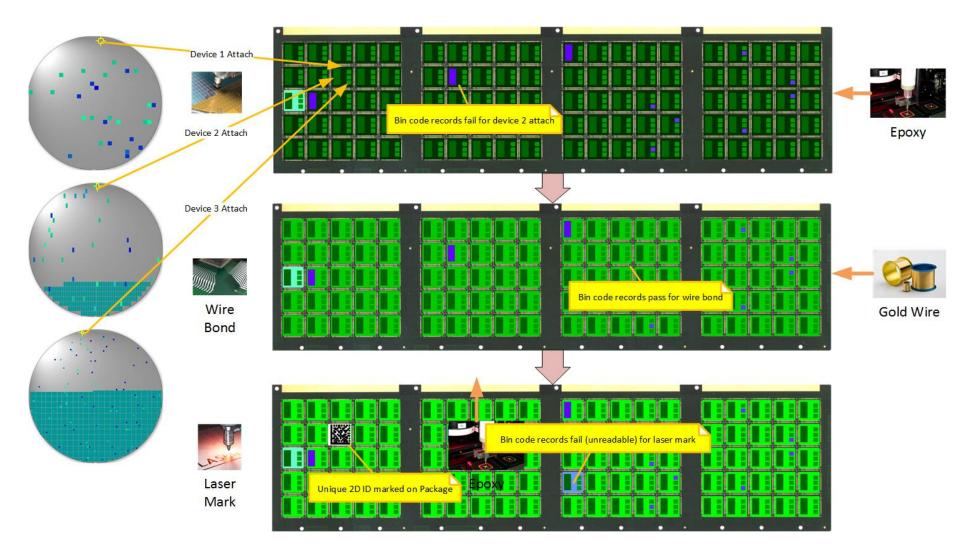




^{*} https://www.nextplatform.com/2021/06/09/amd-on-why-chiplets-and-why-now/



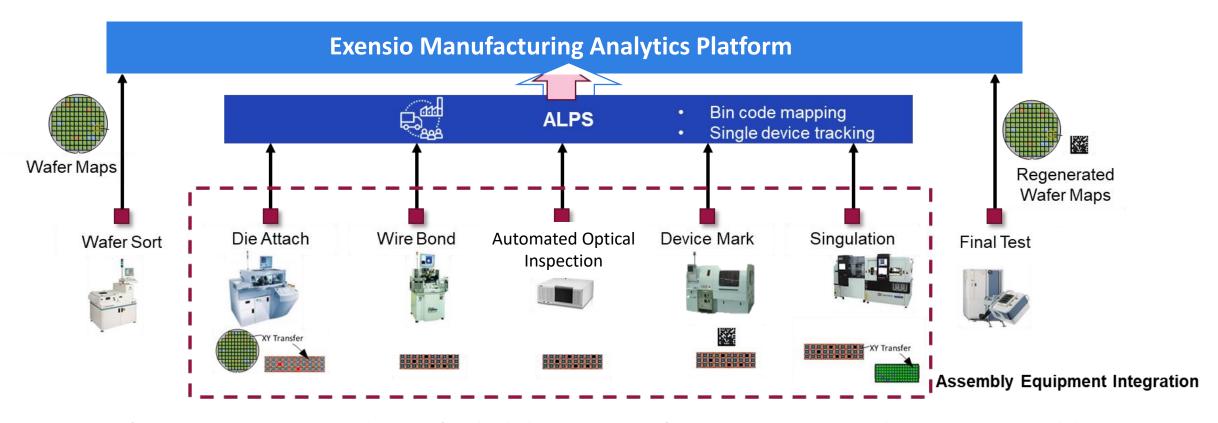
SEMI E142 Standard* for Single Die Traceability & Consumables



https://store-us.semi.org/products/e14200-semi-e142-specification-for-substrate-mapping



Linking All Product Data Through Assembly Without ECIDs



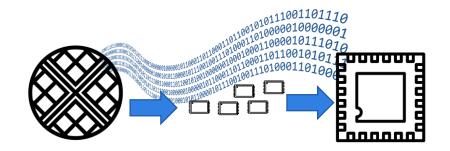
- Perform root cause analysis of reliability and performance issues related to assembly
- Essential for regulated market segments and high value consumer segments

Traceability of all components AND materials of a heterogeneous package

Additional Visibility is Needed for Chiplet-Based Systems

Leveraging front-end characterization

- Full core characterization for KGD determination
- Chiplet performance matching (slow/fast die challenge)



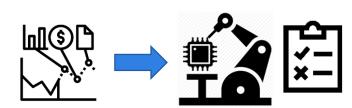
Lifetime diagnosis (via on-die sensors and monitors)

 Wafer sort chiplet screening for marginality and latent defects (reliability risks)



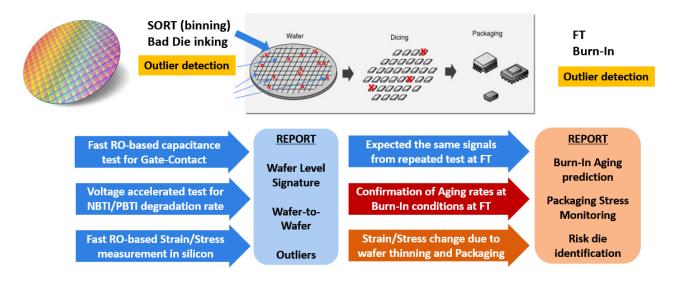
Optimizing cost and quality (predictive analytics)

- Test escapes elimination based on scan data diagnostics
- Burn-in optimization
- Full assembly process traceability

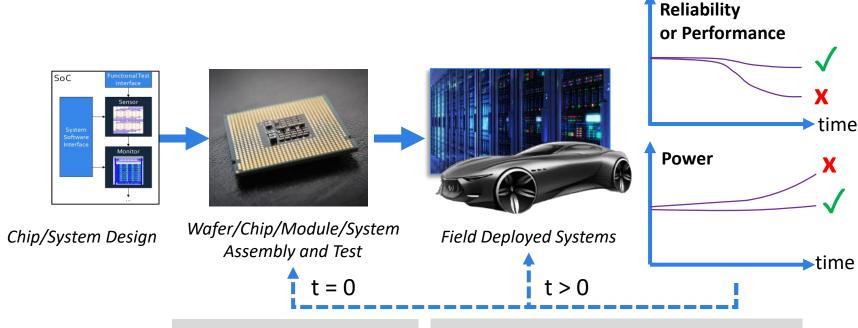


Utilize Front-End Data to Solve Back-End Problems

- ML models built on integrated FE and BE data quantify the relationship between upstream data and final yield
- Scribeline characterization can drive increased visibility and cost reduction
 - Optimize test operations for quality and efficiency
 - Identify scrap material sooner to eliminate wasted BE test



Leverage In-die Sensing for Actionable Insights into Heterogeneous Devices



Test Optimization

- Optimized test flows
- Higher quality
- Faster bring up

Mission-mode optimization

- Increased reliability
- Better Power/Perf. vs. Reliability
- Mission mode failure prediction (e.g., due to delamination, corrosion or cracking)

In Field Monitoring

Fast issue diagnosis and solution

- Burn-in fails
- RMA containment
- End-to-end Analytics for root cause understanding and failure prediction

Improved Quality and Reliability

- Better screening at t=0
- Meet aggressive SLA commitments

Performance Optimization

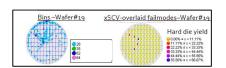
- Process centering
- Power (MWh)
- Variability (bin)



Holistic Product Data Can Provide "Predictive Power"

- Product data is collected to answer product engineering questions
 - Do I have enough product yield to meet my contractual obligations?
- Are you leveraging your product data to achieve Predictive Power?
 - Machine learning enables you to model alternative product test flows very early in the NPI phase when the entire product team is still intact
 - Achieve maximum optimization of yield/quality/reliability based on the target end market for every product

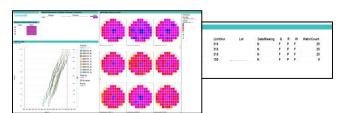
Data + Infrastructure + ML Analytics = Predictive Power



Characterization-to-WS (fail mode analysis)

WS-Scribe-based assisted pattern classification (closed loop)

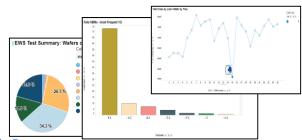
Scribeline assisted pattern classification (ACP)



- Char Data
- WS Data
- Fab Data

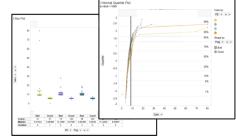
Analysis Infrastructure

- Lot disposition
- FDC Trace Analysis

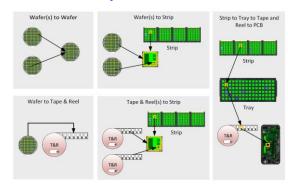


WS historical & daily data monitor

WS and tool commonality



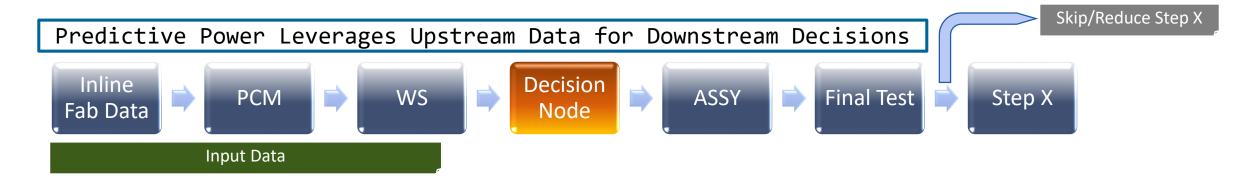
E142 traceability





Applying Predictive Power To Improve Quality & Cost

 Using upstream data, ML analytics can be used to predict if certain downstream steps can be fully or partially skipped



Failure Bin A Prediction	Failure Bin B Prediction	Combined Prediction	Die Population Passed	ACTION
PASS	PASS	BOTH_PASS	30%-50%	Completely Skip
FAIL	PASS	FAIL_BIN_A_ONLY	10%-20%	Partial Testing
PASS	FAIL	FAIL_BIN_B_ONLY	10%-20%	Partial Testing
FAIL	FAIL	BOTH_FAIL	10%-50%	Complete Testing

Value Assessment:
\$1.2M - \$1.7M test
savings annually on
just one product with
no quality impact



Summary

- A comprehensive semantic data model and data infrastructure is needed to leverage product data for heterogeneously packaged devices
- Complete end-to-end data can enable Predictive Power to achieve:
 - Reduced variability in manufacturing, more KGD
 - In-die characterization and sensing to improve "in field" prediction of reliability
 - Single die/chiplet traceability for rapid root cause analysis and automated correction
 - Creation of multiple test populations to reduce test costs with no impact on quality

Heterogeneous integration requires an inclusive data approach from manufacturing to test/assembly/packaging to in-field



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— **Risto Puhakka**, President VLSIresearch

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