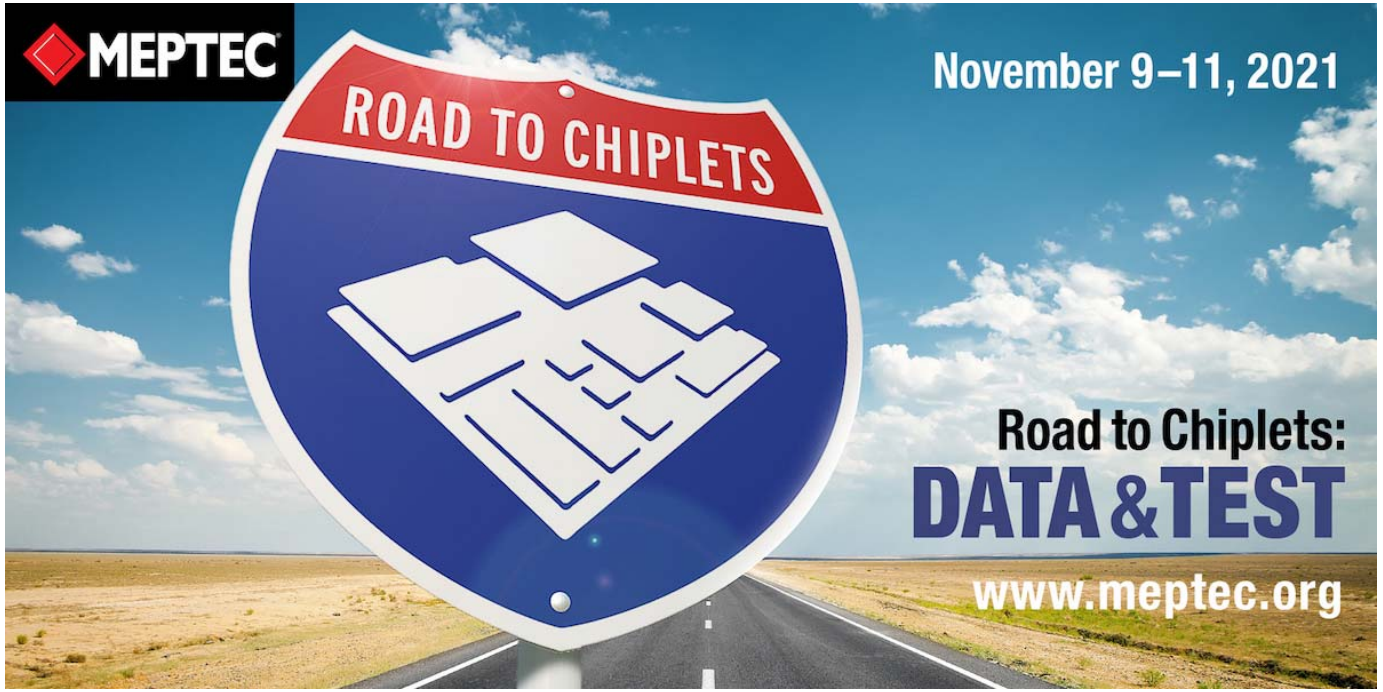


Road to Chiplets: Data & Test

November 9 - 11, 2021

MEPTEC
THE NEXT GENERATION

www.meptec.org

Design of Heterogeneous Integrated Circuits Testing Considerations

Jawad Nasrullah

Palo Alto Electron Inc

Nov 09, 2021

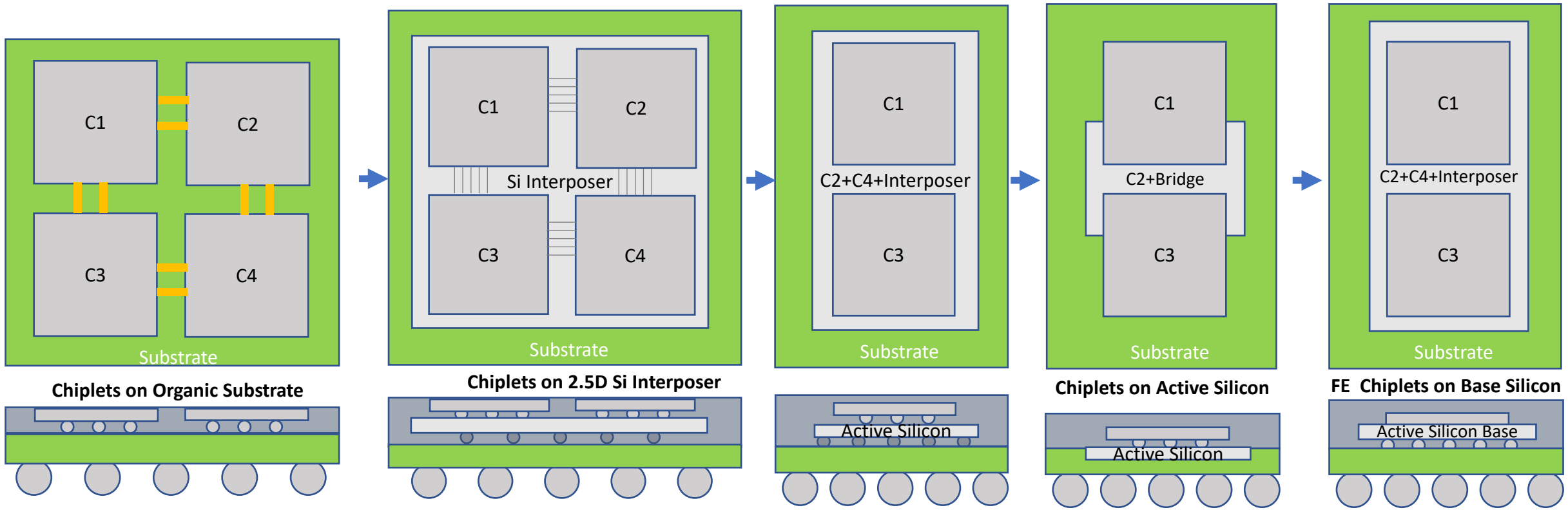
jawad@paloaltoelectron.com

Outline

1. Chiplet Integration
   - Heterogeneous Integrated Circuits with Chiplets
   - Chips vs Chiplets
2. Testing of Heterogeneous ICs
   - Chiplet Q&R Background
   - Design and Manufacturing Steps
   - Testing of Heterogeneous Chips
   - System Level Test (Jawad's Definition=> SLT = Structural Final Test + Some basic Functionality Test)
   - Test
3. A Chiplet BIST Example
   - zGlue OmniChip and BIST
   - Fabric Chiplet Testing Scheme
4. SUMMARY

Chiplet Integration

Integrated Circuits With Chiplets

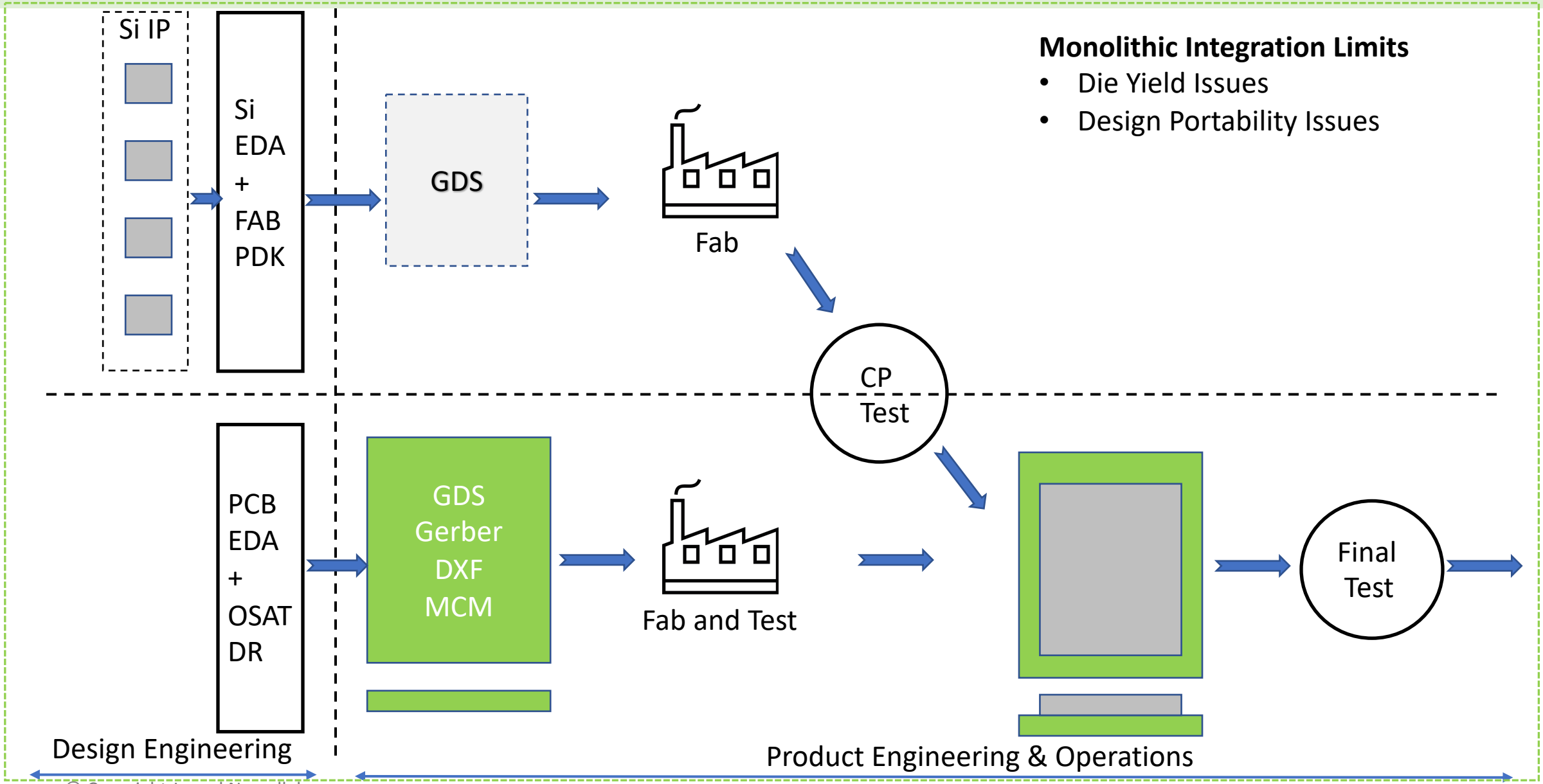


Chiplet on Organic	2.5D Chiplets	Active Interposer	Si Bridges	FE Chiplets
CP Test (Chiplets)	CP Test (Chiplets+Interposer)	CP Test (Chiplets+Interposer)	CP Test (Chiplets+Bridge)	CP Test (Chiplets+Base Die)
E-Test (Substrate)	E-Test (Substrate)	E-Test (Substrate)	E-Test (Substrate)	E-Test (Substrate)
Package/Final Test	Package/Final Test	Package/Final Test	Package/Final Test	Package/Final Test

Chips vs Chiplets

	Chips	Si Hard/Soft IP	Chiplets
State	Physical Goods	IP	Physical Goods
Trading	Buy/Sell with Warranty	Buy/Sell with Warranty	Buy/Sell with Warranty
Warranty	Warranty for DPPM	N/A	Warranty for DPPM
2L Assembly	SMT Capable	N/A	SMT or Wire-bond
Packing	Tape & Reel	N/A	Tape & Reel or Wafer Sale
Testing	Testable by Manufacturer. Some have JTAG boundary scan.	N/A	Testable by Customer. Need boundary scan at least.

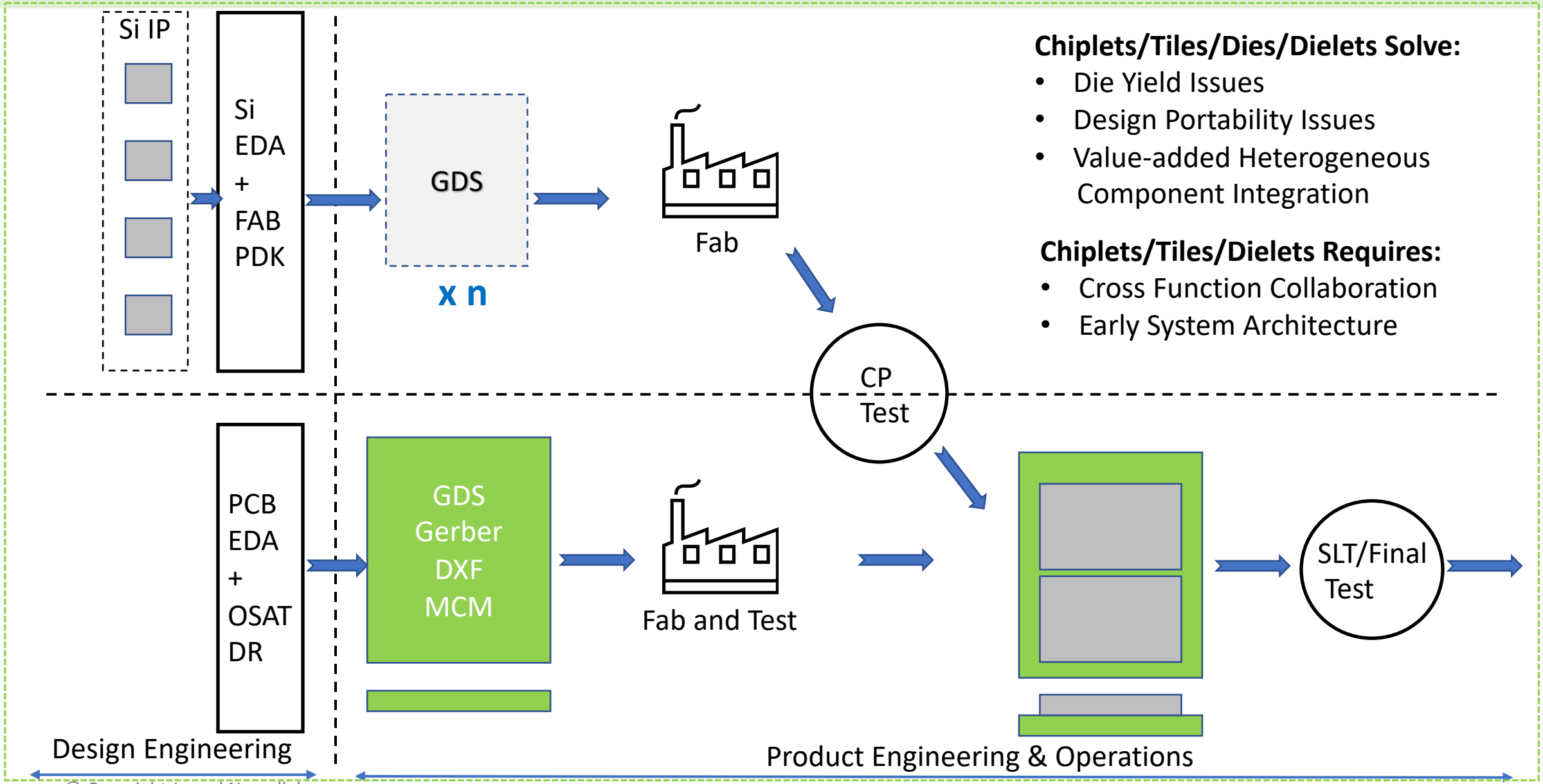
Single Chip Integrated Circuits (LEGACY)



Monolithic Integration Limits

- Die Yield Issues
- Design Portability Issues

Multi Chiplet Integrated Circuits (NEW)



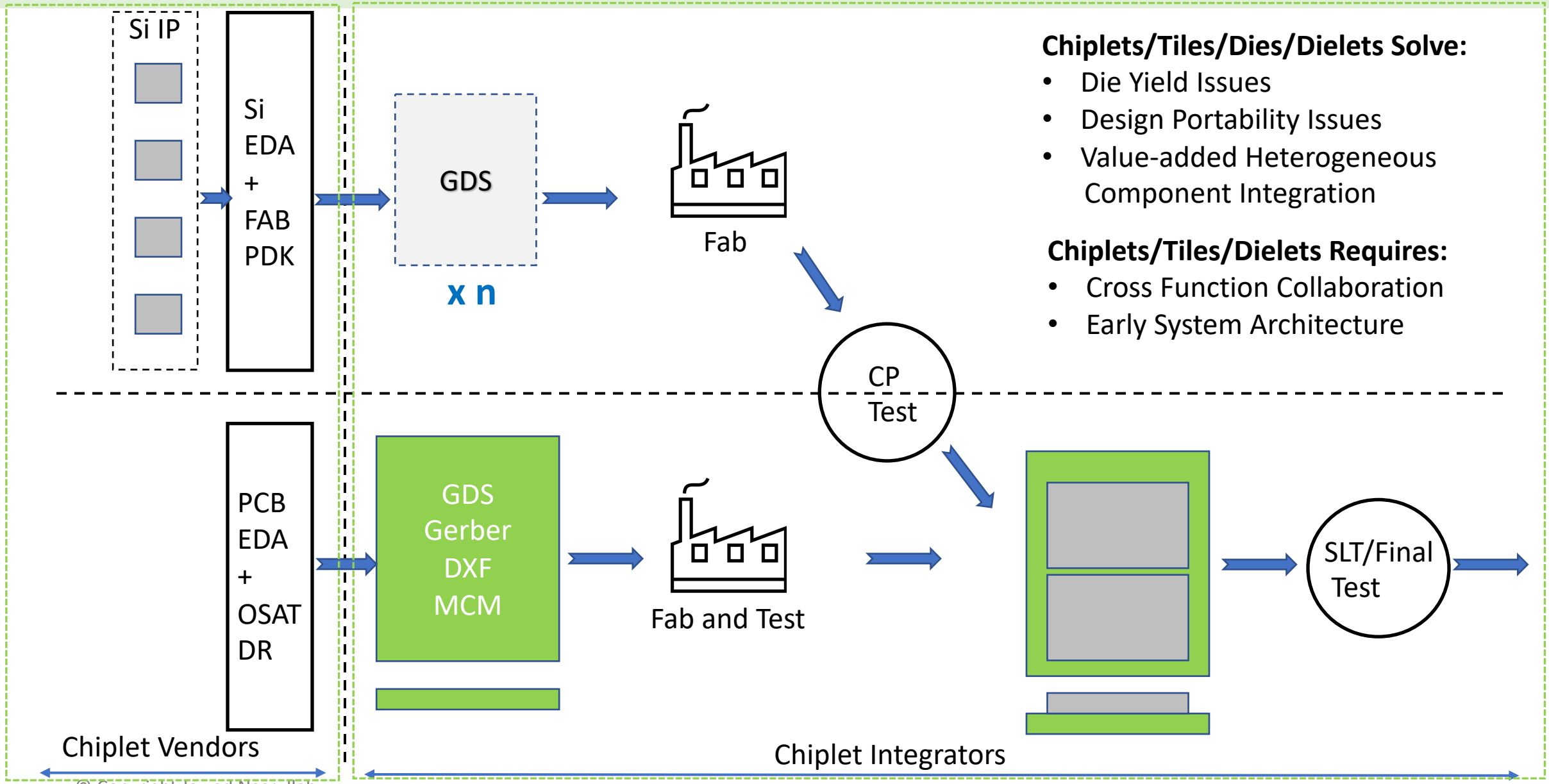
Chiplets/Tiles/Dies/Dielets Solve:

- Die Yield Issues
- Design Portability Issues
- Value-added Heterogeneous Component Integration

Chiplets/Tiles/Dielets Requires:

- Cross Function Collaboration
- Early System Architecture

Multi Chiplet Integrated Circuits (UPCOMING)



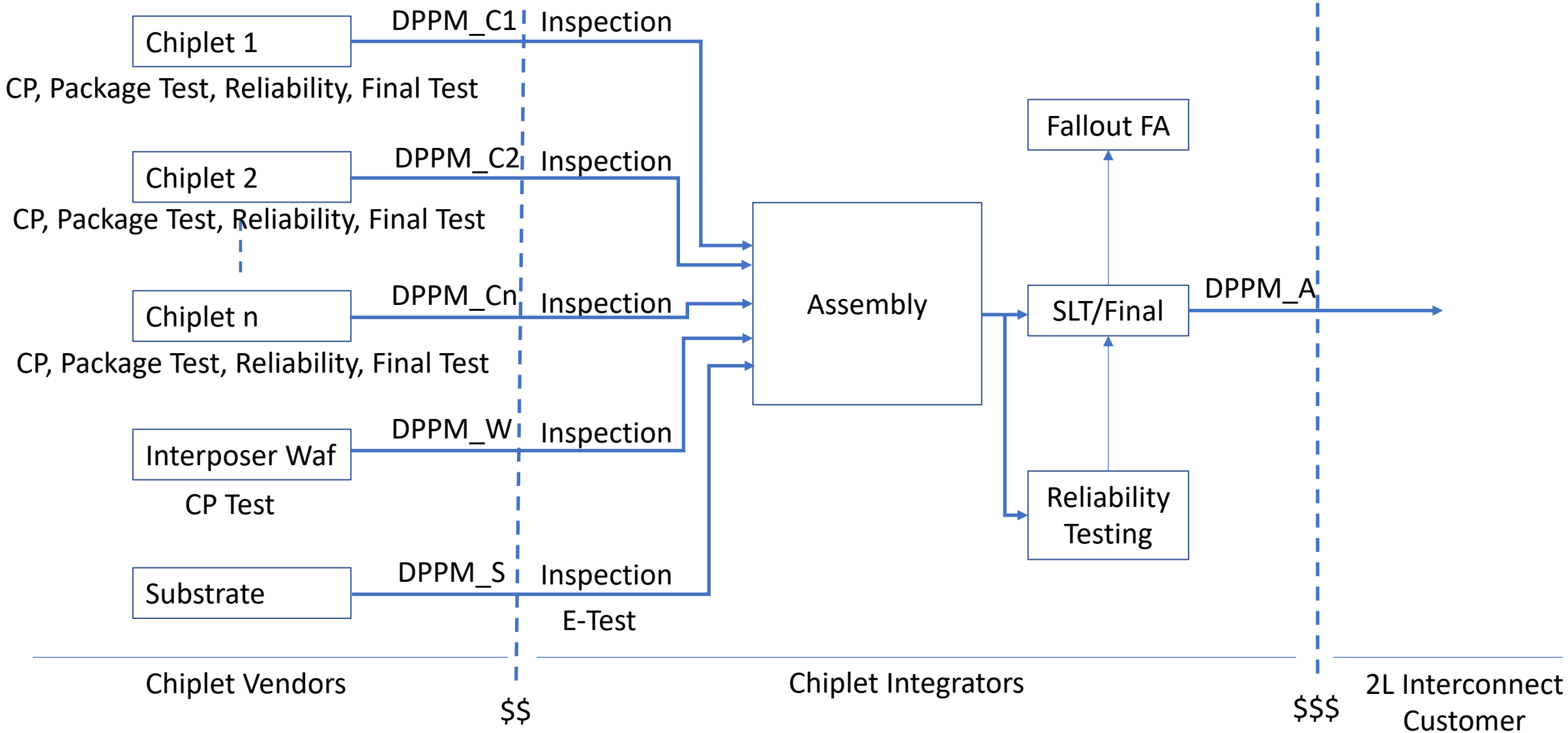
Chiplets/Tiles/Dies/Dielets Solve:

- Die Yield Issues
- Design Portability Issues
- Value-added Heterogeneous Component Integration

Chiplets/Tiles/Dielets Requires:

- Cross Function Collaboration
- Early System Architecture

Chiplet Integration Operations Flow



Testing of Heterogeneous ICs

Chiplet Quality and Reliability

Quality = Performance Against Specification

Wafer Probe for Chips, Chiplets, Interposers
E-Test for Substrates
System Level Test (SLT) for Package Assemblies

Need to have the ability to observe and debug failures

- Production Quality Tests Look for Defects in
  -Incoming material
  -Manufacturing Yield
- Systematic Failures should be addressed separately
- Chiplet A+B Failures should be addressed in the design and qualification phase
- SLT includes, a) functionality and communication, b) power, clocks, resets, configs, c) RF performance

Chiplet Quality and Reliability

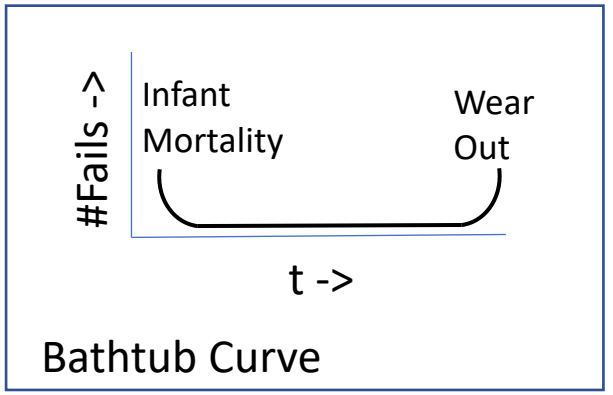
Quality = Performance Against Specification

Wafer Probe for Chips, Chiplets, Interposers
E-Test for Substrates
System Level Test (SLT) for Package Assemblies

Need to have the ability to observe and debug failures

Reliability = Quality Over Time (given various operating and environmental conditions)

Acceleration Tests:
PreCon/Autoclave= f(RH, P, T) environmental pre-conditioning
P/TC/TS = f(T, dT/dt), mechanical/solder failures due to Temp Cycle and Shock
THB, u/bHAST = f(V, T, RH) , corrosion
HTS = f(T, t), high temperature storage life
HTOL = f(V, T), looks for wear Out of wires and dielectrics
Burn-in (ELF) = f(V, T), looks for Infant Mortality of Silicon
2nd Level Interconnect Testing
⋮
ESD: HBM, CDM Human and Manufacturing Equipment Electrostatic Discharge
LU Latchup



Design and Manufacturing Steps—Chips / Chiplets

DESIGN STEPS

1- Architecture

2- Design
- IO Planning
- RTL Design and Verification
- Schematic Capture
- DFT/BIST

3- Chip Layout / Routing / Package Layout

4- Verification
- Functional/Formal
- Electrical
- Thermal/Structural

5- Send to Manufacturing

MANUFACTURING STEPS

1- Wafer Fab, Contact Probe

2- Substrate Fab, e-test

3- uBump/Assembly/CSP/BGA

4- Packaged Part Test

5- ESD and Latchup Tests (sampling)

6- Reliability Tests (sampling)

7- Infant Mortality Burn-in

8- Final Test

Design and Manufacturing Steps—Chiplet Integration

DESIGN STEPS

1- Architecture, Chiplet selection/design, Package Technology Selection

2- Design
- IO Planning
- RTL Design and ESL Verification
- Schematic Capture/Netlist Gen
- Component Placement

3- Substrate/Interposer Routing and Layout

4- Verification
- Thermal
- Functional
- Electrical

5- Send to Manufacturing

MANUFACTURING STEPS

1- Interposer Fab, Contact Probe

2- Substrate Fab, e-test

3- Chiplet Assembly/Packaging

4- Package Final / System Level Test

5- ESD and Latchup Tests

6- Reliability Tests

7- Infant Mortality Burn-in?

Testing of Heterogeneous Chips

Contact Probe Test For Chiplets

- One Chip CP Test
- Multi Chiplet CP Tests

- Test NRE: Probe Cards, Test Development
- Unit Cost = Die Test Time per Chiplet x #Chiplets

System Level Test After Packaging

- Packaging Quality Test (Open/Short)
- IDDQs
- FW Loading
- System Level Function Test
- RF Test

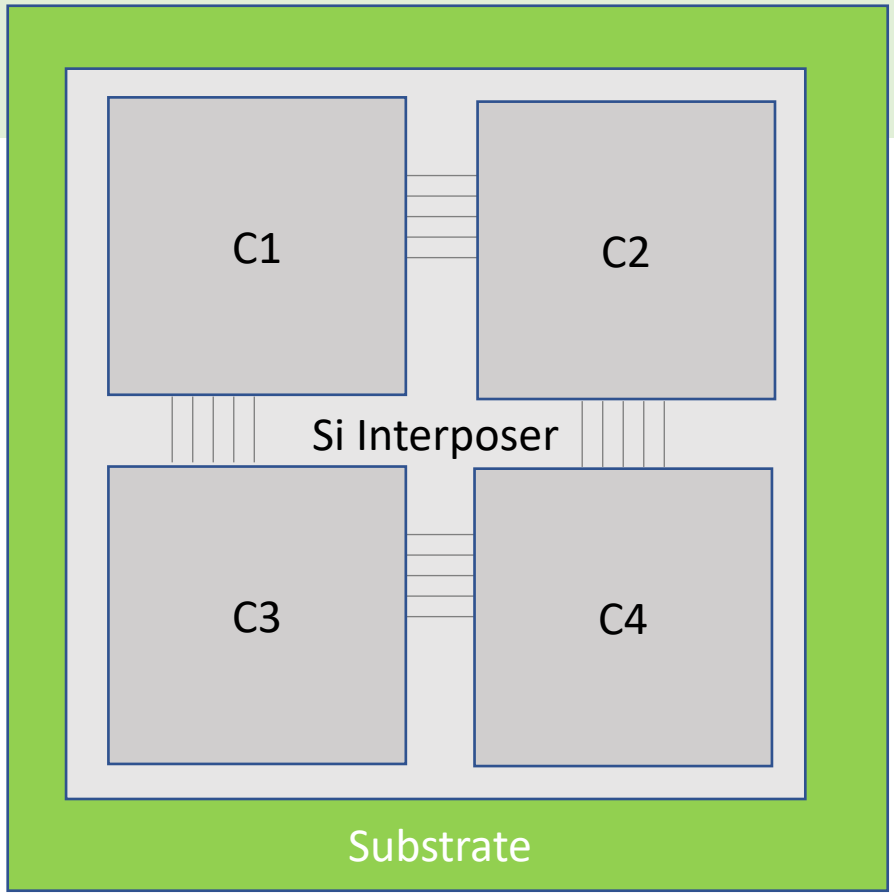
- Test NRE: SLT Test Boards, Test Equipment
- Unit Cost = Test Time for structure check and functional check

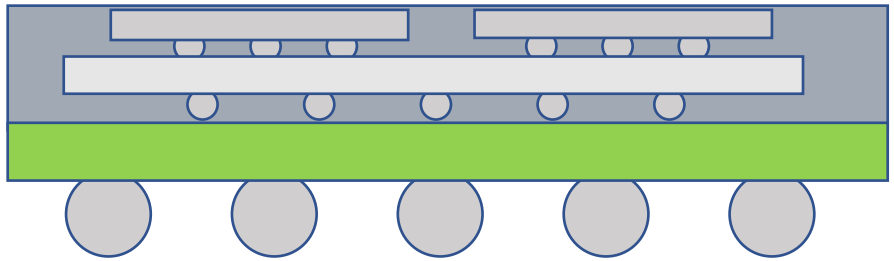
Reliability Tests

- Solderability/Reflows
- Thermal Cycle
- Environmental
- ESD/LU
- HTOL
- ELF Burn-in

- Test NRE: Test Boards, Sample Tests

Testing of Heterogeneous Chips



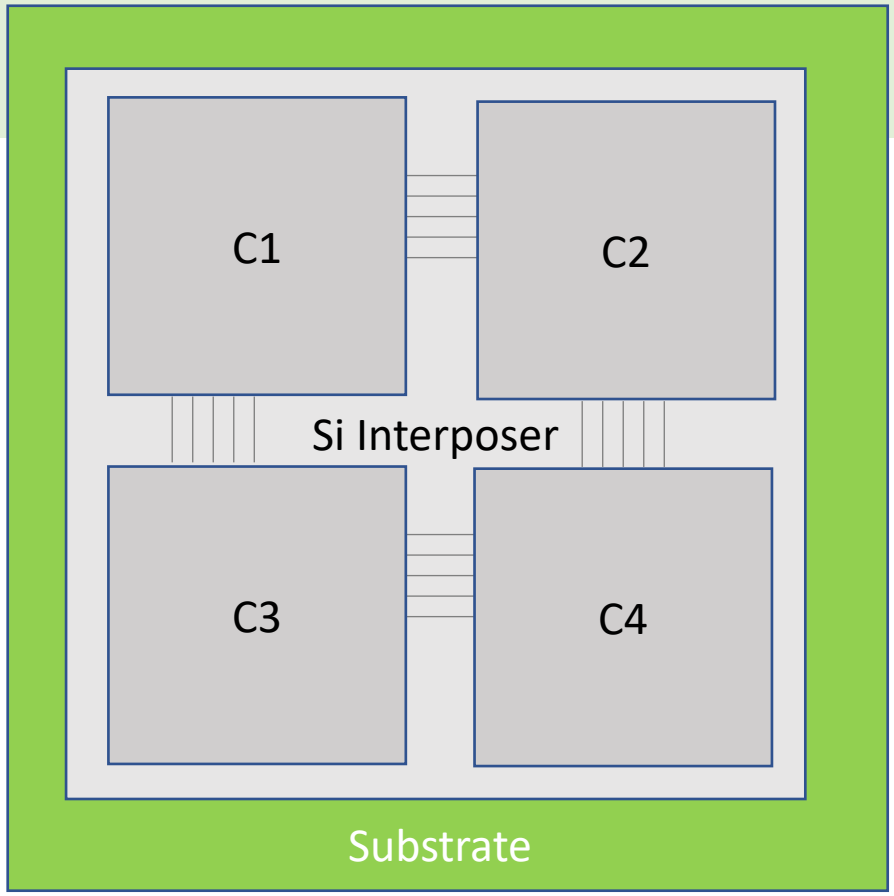


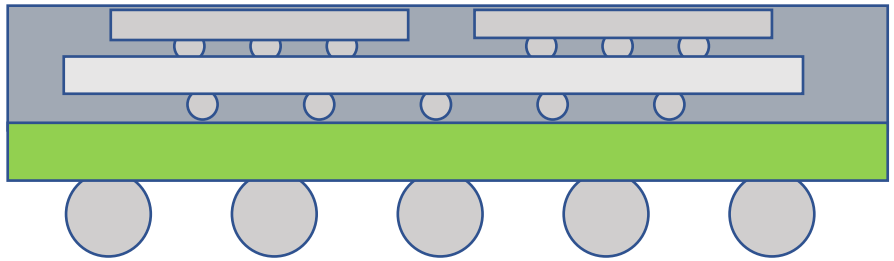
DFT & Verification:
- Need ESL (transaction level) and IBIS Models for all Chiplets
- Need Mechanical Models for all Chiplets for Thermal/Mech Simulations
- Simple JTAG in each Chiplet

Incoming Material:
- Visual Inspection
- Quality of Chiplets to be guaranteed by the Vendor
- E-test for substrate
- CP test for Si Interposer

After Assembly:
- Inspection (e.g. x-rays)
- System level testing to verify assembly process (JTAG needed)
- Reliability testing

Yield Estimation Example





Incoming DPMin Chiplet C1-C4= DPM_C < 100
Number of Chiplets = N = 4
Incoming DPM in Si Interposer= DRM_W <100

Failed Assemblies due to incoming DPM
= N x DPM_C+ DPM_W
= 4 x 100 + 100 = 500 (99.95%)

Control of Incoming DPM_C is the key for Yield.

Assembly Yield numbers can be awesome.

System Level Test is the key to control outgoing DPM For Heterogeneous Chips.

Components of SLT/Final Test

1- Find Assembly Defects

- Open/Short (validate the connectivity)
- Open/Short Repair

2- Validate System IDDQs

- Check Power Down IDDQs on all Chiplets
- Validate all IDDQ combos

3- Validate Functionality

- Load/Run SLT FW
- Test Bootup, Pairwise communication
- Outside connectivity Loop Backs. Eye scans.
- Run a bare minimum system function/customer app
- Test Mechanicals and Thermal

4- Save Program/Repair/FW/Keys

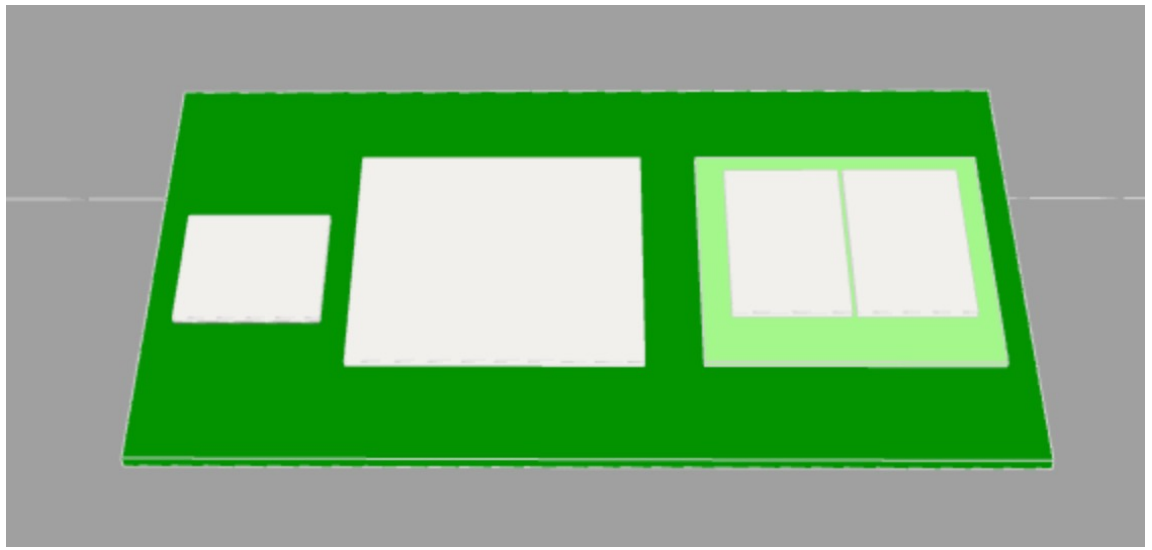
- Store data in the IC

Design For SLT/Final Test

EVT->DVT->PVT:
- Design for SLT in EVT Phase

Assembly Design:
- Design Open Short Testing BIST
- Simulate the system for open shorts. Identify sensitivities for Test Engineering.

System Design:
- Add JTAG to every component
- Add instrumentation circuits (Imon, Eyescan…)



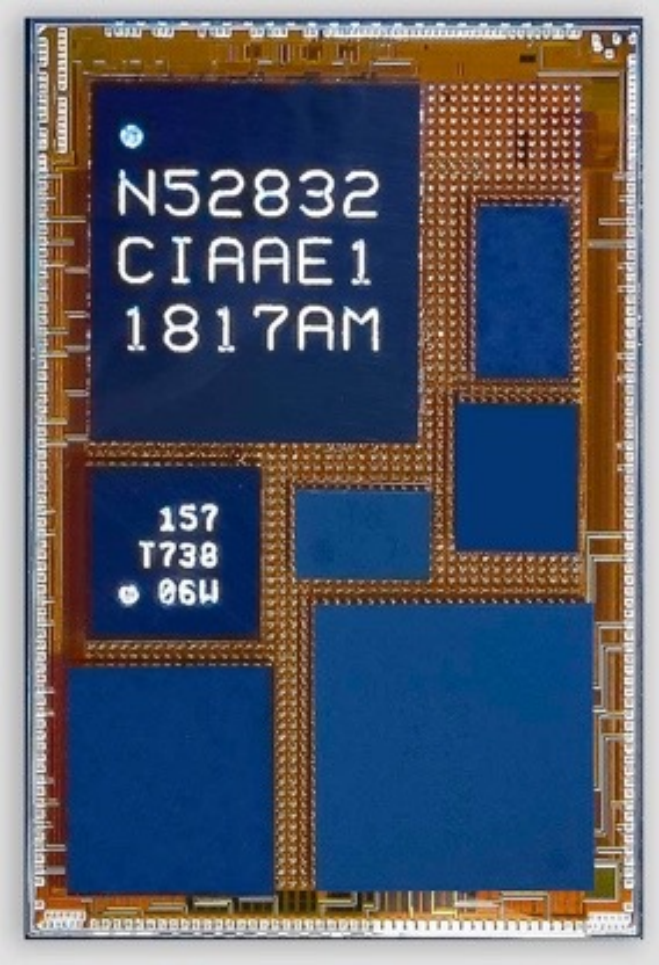
Develop Bench Test FW in EVT:
- Precursor to SLT FW and Automation
- Test Bootup, Pairwise communication
- Outside connectivity Loop Backs
- Run a bare minimum system function

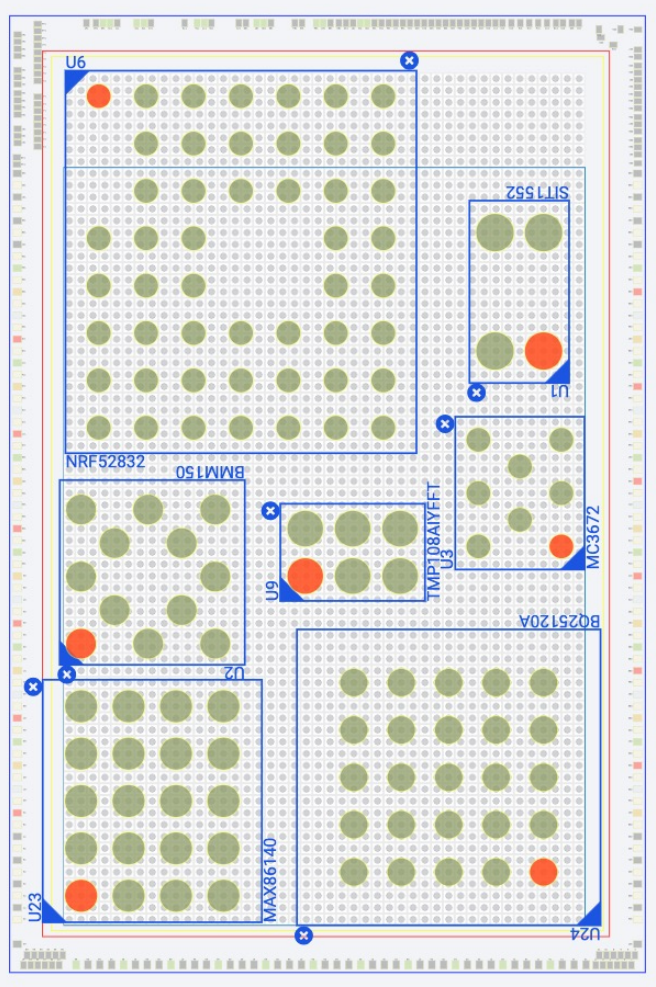
Power Delivery Network Design:
- Design for systematic Power Down and Power Up for Test Engineering

D2D and External IO:
- Design for pairwise chiplet test
- Design for external loopbacks (SerDes/RF)

A Chiplet BIST Example

An Example—zGlue OmniChip





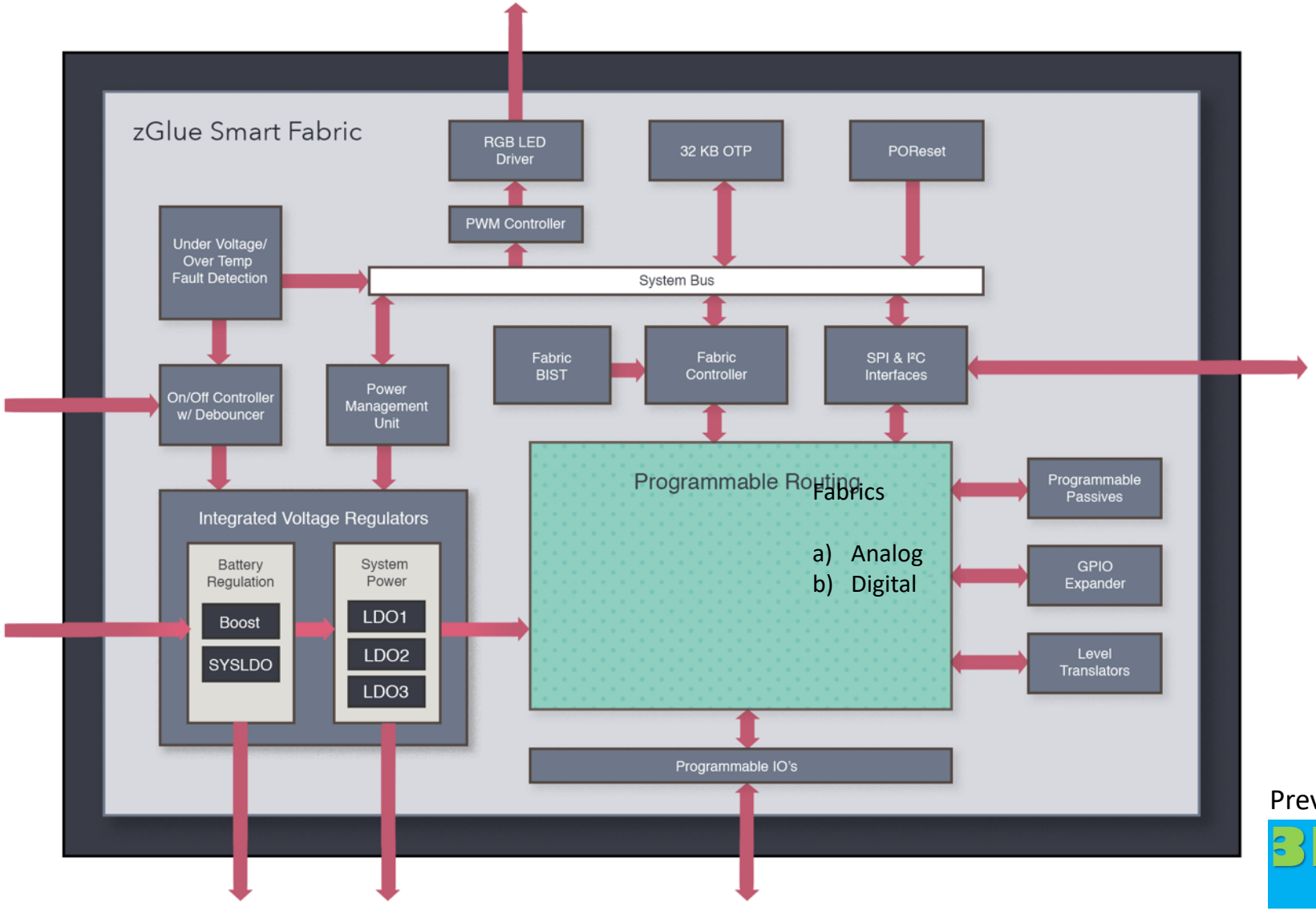
8 Chiplet Assembly

- 1x Fabric Chiplet 2500 Cu Pillar
- 7x CSP Chiplets
- F2F Assembly (CoWoS Style)

Previously Presented at

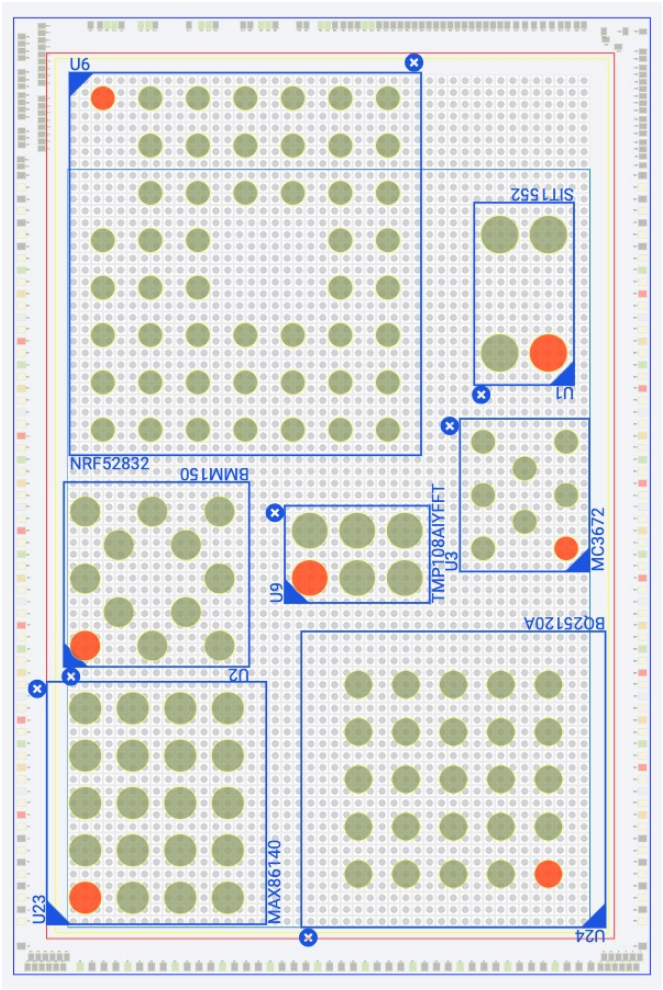
3DC-TEST
Nov 6-7, 2020

An Example—zGlue Smart Fabric Chiplet



Previously Presented at

Active Interposer Chiplet BIST Scheme



Built in Testability Functions with a matrix of Cu pillars

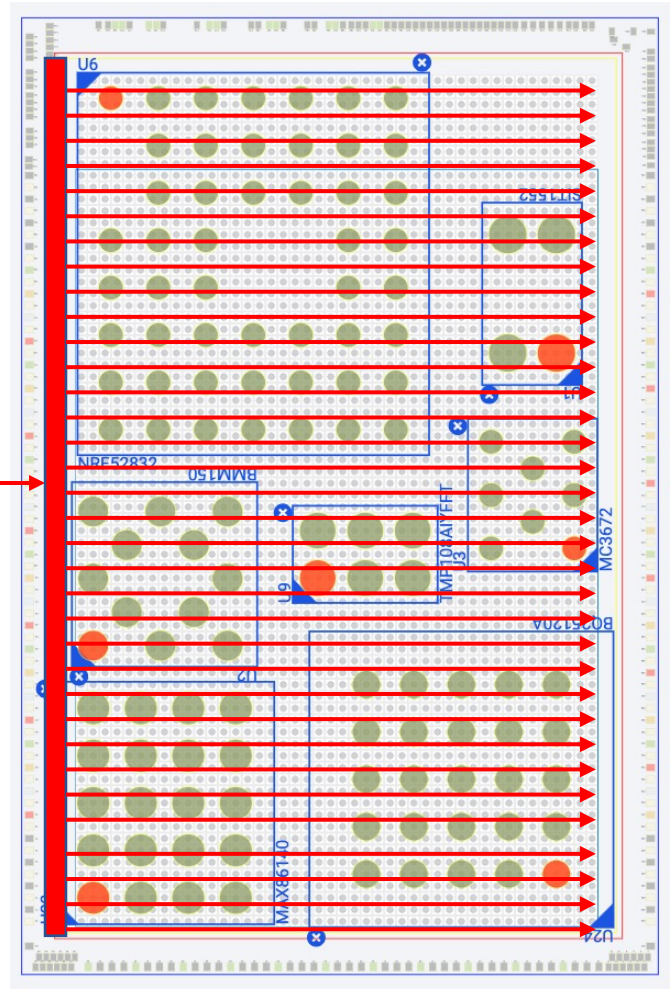
1. Open/Short
2. IDDQ
3. Connectivity
4. Programmable Probe
5. Kelvin
6. Pull up/pull down
7. Cap insert
8. Level Shift
9. Programmable IO
10. Chiplet VID

Support for 400um balls to <55um u-bump pitch

Previously Presented at

3DC-TEST
Nov 6-7, 2020

Active Interposer Chiplet BIST Scheme



Built in Testability Functions with a matrix of Cu pillars

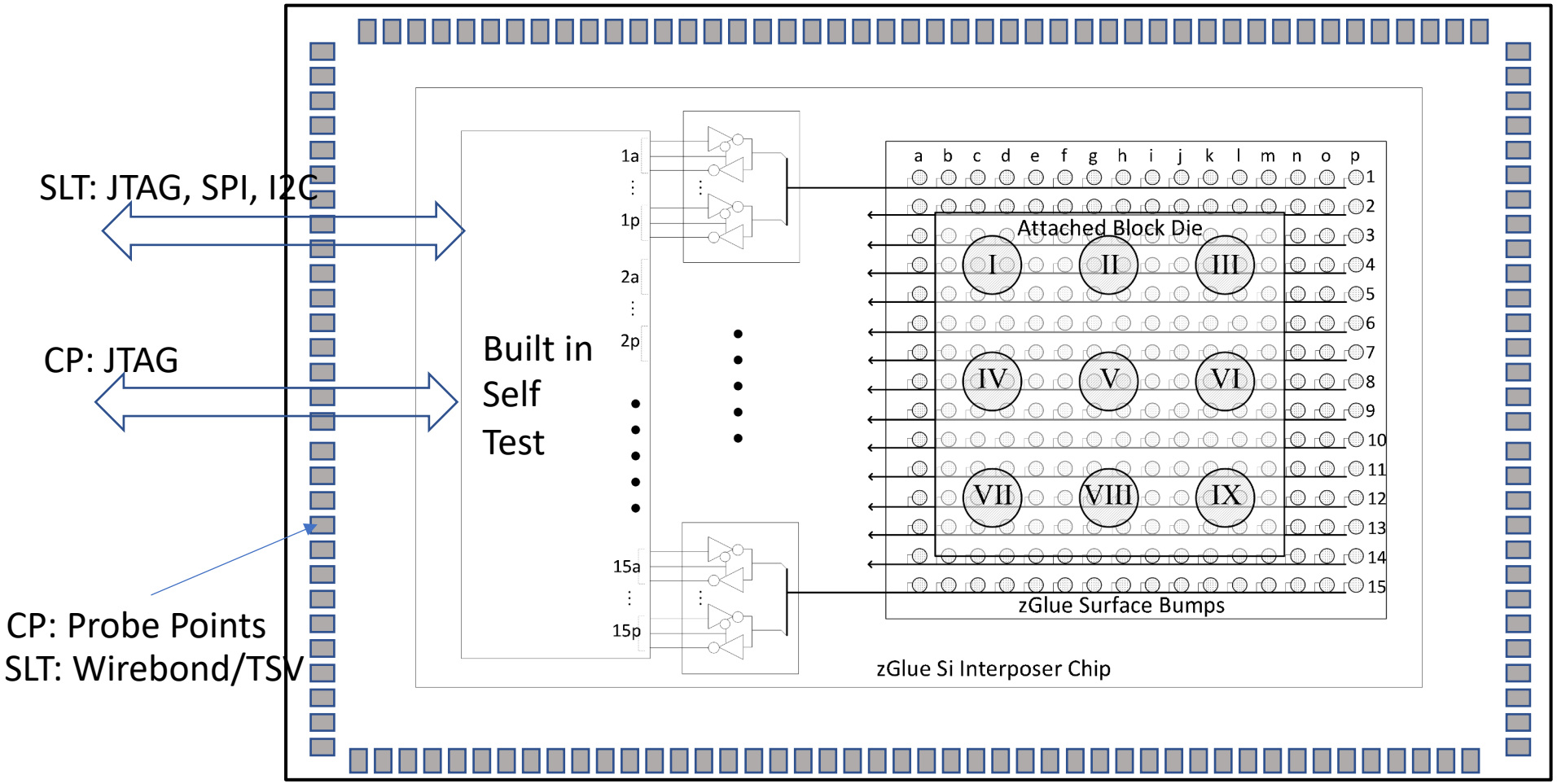
1. Open/Short
2. IDDQ
3. Connectivity
4. Programmable Probe
5. Kelvin
6. Pull up/pull down
7. Cap insert
8. Level Shift
9. Programmable IO
10. Chiplet VID

Support for 400um balls to <55um u-bump pitch

Previously Presented at

3DC-TEST
Nov 6-7, 2020

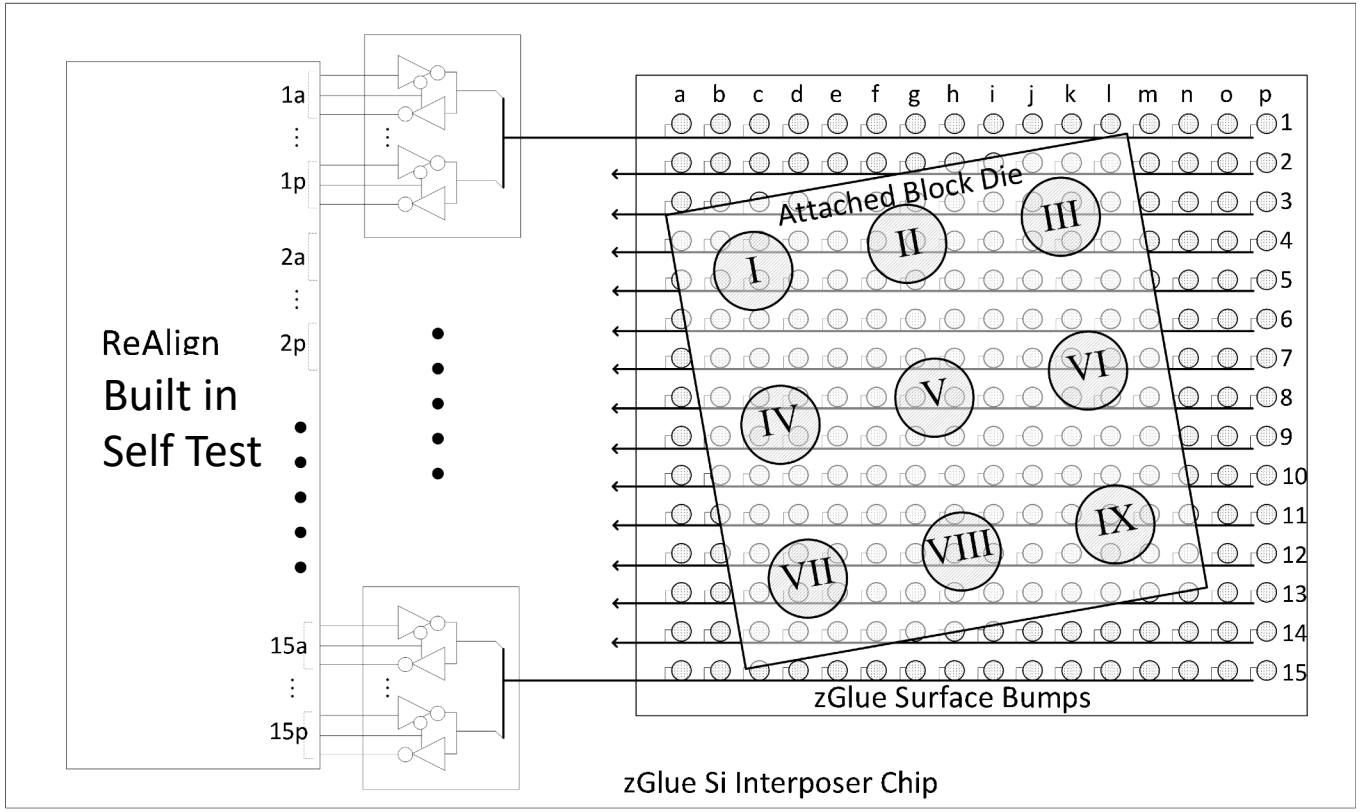
Active Interposer Chiplet BIST Scheme

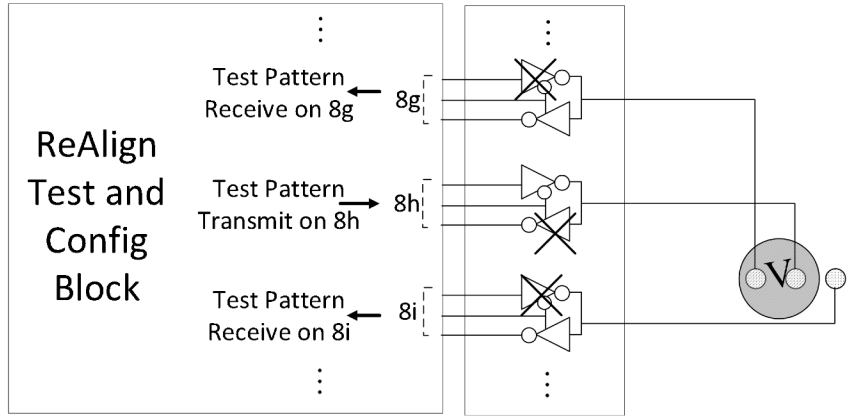


Previously Presented at

3DC-TEST
Nov 6-7, 2020

Active Interposer Chiplet BIST Scheme





Previously Presented at

3DC-TEST
Nov 6-7, 2020

Summary

1. Chiplets
   - Proper Test Planning is key for Chiplet based product
   - Test Plan is easier when Chiplets are being developed in-house
   - Third Party Chiplet Vendors will need to provide graybox models.

2. Testing of Heterogeneous ICs
   - Components need to be tested individually before assembly. KGD is a challenge. Proper chiplet design with BIST and Design for SLT is key.
   - Product goal should be to eliminate all pairwise design flaws at bench testing and only test for manufacturing quality.
   - Test cost can be controlled at levels comparable to monolithic solutions.
   - Work out ELF in Chiplets before assembly if possible.
   - 1149 is a great option for chiplets.

3. Chiplet BIST
   - Self test designed to assist SLT helps reduce test time.
   - Visibility of signals at debug IO reduces need for complicated FA.

Thank You

Thank you sponsors!

Amkor's Differentiators

Technology

Advanced Packaging Leadership
Engineering Services
Broad Portfolio

Quality

QualityFIRST Culture
Execution
Automation

Service

Design & Test Through Drop Ship
Manufacturing Footprint
Local Sales & Support

Global Companies Rate Advantest THE BEST ATE Company 2021

Advantest receives highest ratings from customers in annual VLSIresearch Customer Satisfaction Survey for 2 consecutive years.

Global customers name Advantest THE BEST supplier of test equipment in 2020 and 2021, with highest ratings in categories of:

Technical Leadership – Partnership – Trust – Recommended Supplier – Field Service

"Year-after-year the company has delivered on its promise of technological excellence and it remains clear that Advantest keeps their customers' successes central to their strategy. Congratulations on celebrating 33 years of recognition for outstanding customer satisfaction."

— **Risto Puhakka**, President VLSIresearch


SYNOPSYS®
Silicon to Software™

COPYRIGHT NOTICE

www.meptec.org

MEPTEC
THE NEXT GENERATION