

Road to Chiplets: Data & Test

November 9 - 11, 2021







Test Impacts of Chiplets in Packages

George Harris I VP, Global Test Services
November 2021

Agenda

- 1 Chiplets & End Markets
- Package Integration Technologies & Landscapes
- 3 Package Applications & Aspects
- 4 Impacts & Opportunities for Test & Data



Amkor Dielet & Chiplet Integration Market Apps



Automotive, Health, Industrial

ADAS, SiP/IVI, MEMS, Sensors, Performance, Safety



Communications

5G, RF & Mixed Signal, Handheld Devices, Mobile/Smartphones, Tablets, IoT, Satellite



Artificial Intelligence, Networking, Computing

Networking,
Data Center, Infrastructure,
PC/Laptop, Storage



Consumer

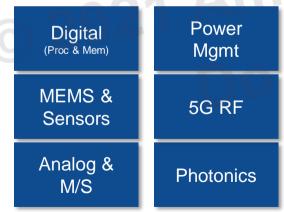
Connected Home, Set-top Box, Televisions, Visual Imaging, Wearables

Multi-die packages are ubiquitous!



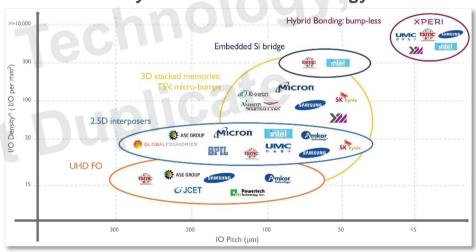
Technology Integration Processes

- ▶ SiP and module
- ▶ 3D & interconnect
- Wafer level fan-in & fan-out



Industry level push in all segments

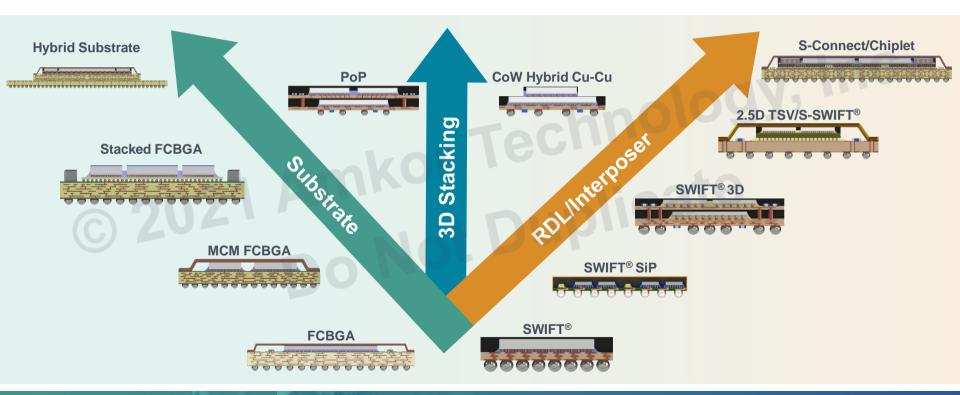
Mapping of High-End Packaging Players Based on Technology



Source: High-end Performance Packaging 3D/2.5D Integration 2020 report, Yole Développement, 2020

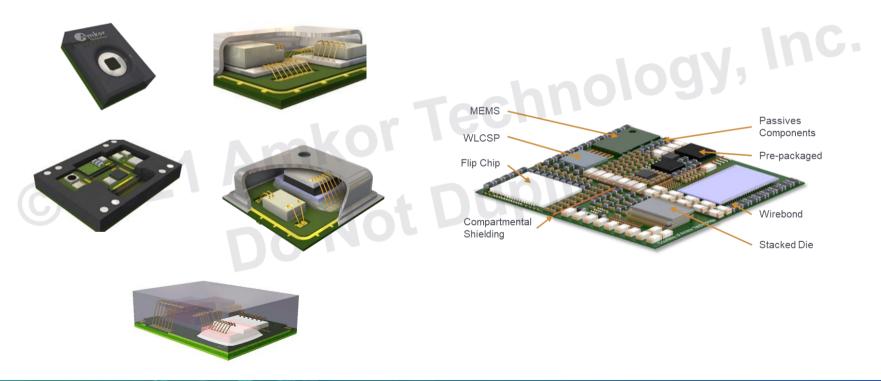


Amkor Multi-Die Package Technologies



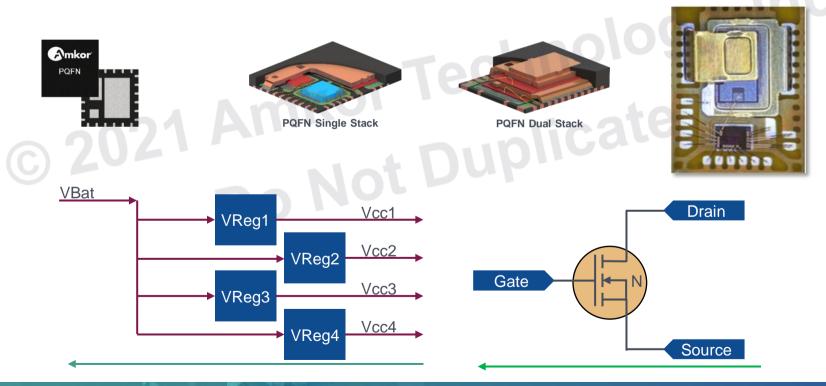


Amkor Multi-Die Package Assembly w/Sensors





Amkor Multi-Die Package Assembly for Power



Amkor Package Assembly for SiPs



1x SiP

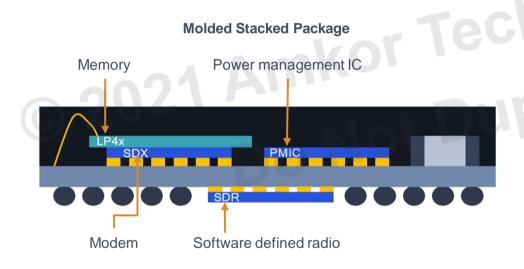


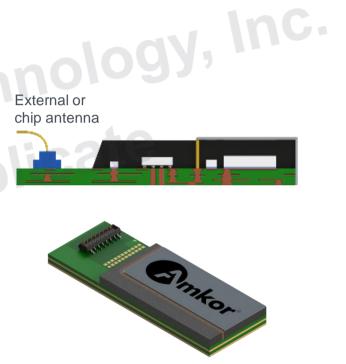
Source: IHS Markit

75% area reduction



Amkor Package Assembly



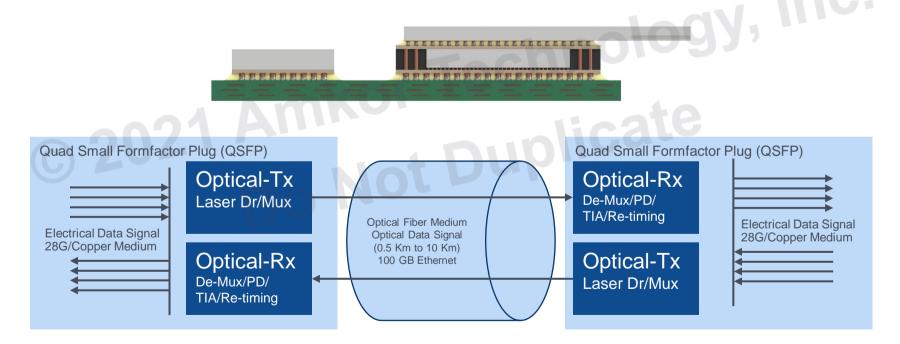


Embedded patch antenna



Amkor Package Assembly for Si Photonics

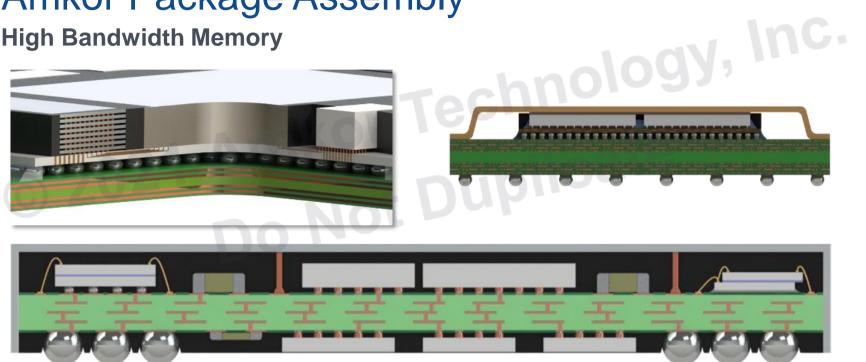
Enabling 100 to >400 Gbps data rates





Amkor Package Assembly

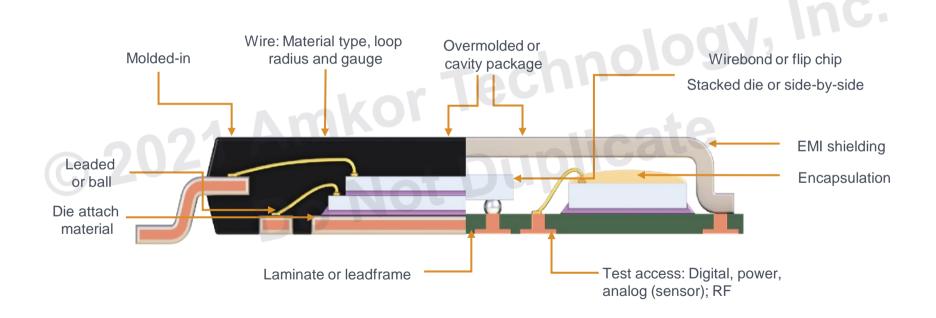
High Bandwidth Memory



As packaging complexities increase, new matching test methodologies must be architected

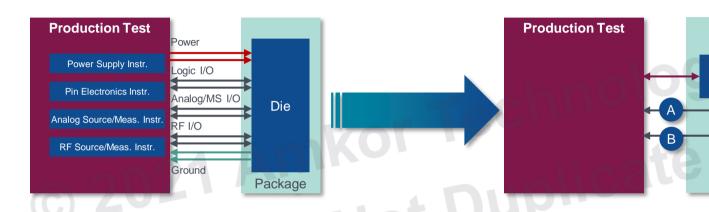


Amkor Package Assembly – Aspects & Test





Production Test Challenges



- No direct access
- Radiative access
- Digital system bus protocol

Die 2 interface physically

Die 1

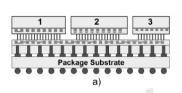
- A Not pinned out
- B Pinned out



Die 2

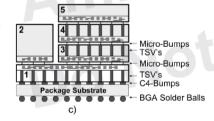
Package

High Density Digital Packages – TAPS



Stacked IC

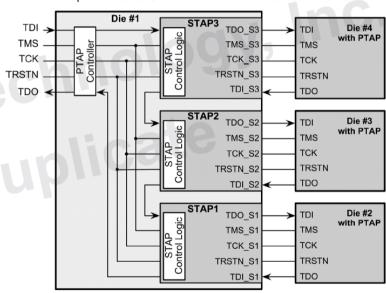
- a) 2.5
- b) 3D
- c) 5.5D



3D-IC stacks to a 2.5D-IC silicon interposer

P/S TAP: Primary & secondary test access port



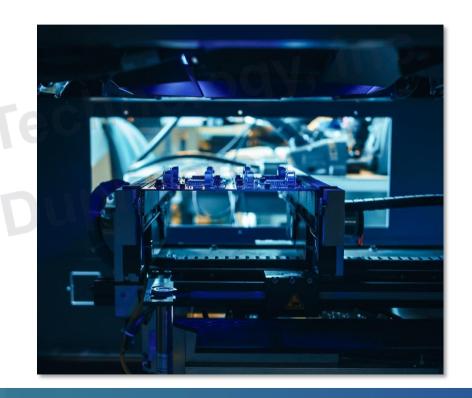


Source: "IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits," in IEEE Std 1838-2019, vol., no., pp.1-73, 13 March 2020, DOI: 10.1109/IEEESTD.2020.9036129.



Impact to Production Test Methodology

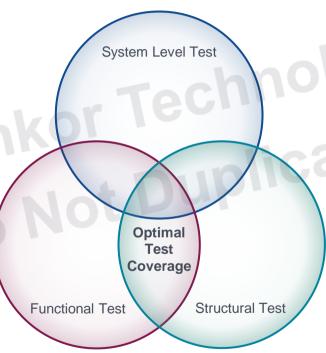
- Functional & structural test content
 - BIST, SBFT, scan IEEE 1149.x, 1500, 1687
- Digital test equipment may require protocol aware instrumentation
- ➤ Concurrency e.g., multi-site & within single DUT





System Level Production Test – Coverage

- ► High-speed serial interface, e.g., USB, PCIe, MIPI, UFS, Ethernet
- ► Test access port, serial, e.g., IEEE 1149.x, 1500, 1687, SPI/I²C...
- Contactless interface e.g., Wi-Fi, 5G NR RF, Zigbee...



DFx

- Mfg: Yield optimization, fault isolation
- Quality & reliability burn-in, stress
- ▶ Thermal design
- ► Test: High-speed serial, 5G RF, analog, digital content generation

Amkor has the equipment and engineers for these test challenges



System Level Test Equipment

Tester

- Power, signal, clock, protocol
- SLT Requirements –
 eased by FPGA based
 instrumentation &
 popularity

Handler

- Package size range
- Massively parallel
- High UPH In

Test Hardware

- Mimic end application
- Increased complexity
- Increased test coverage

TechWing



Hontech



Chroma



Advantest



Teradyne



Production Test – Impact to Test Flow

Example: Single chip production test flow

Altered Test Flow

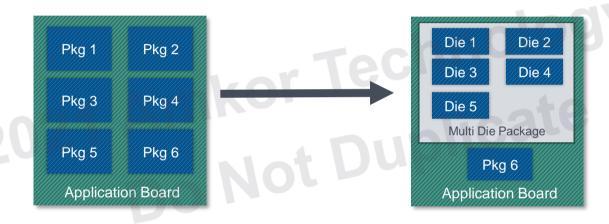


Example: Multi-chip cost optimized high level production test flow Post Test **KGD** SLT Pass **Test** Wafer Probe (OS boot, Multimedia, Lot Accept Result Packaging Communication) (WL Burn-in/Stress) Fail/Sample Final Test/Stress Burn-in (FA, Yield Opt.) (Reliability)

Test Content Re-distributed

Platform Level Test Quality

Test Data Enabled Advanced Manufacturing

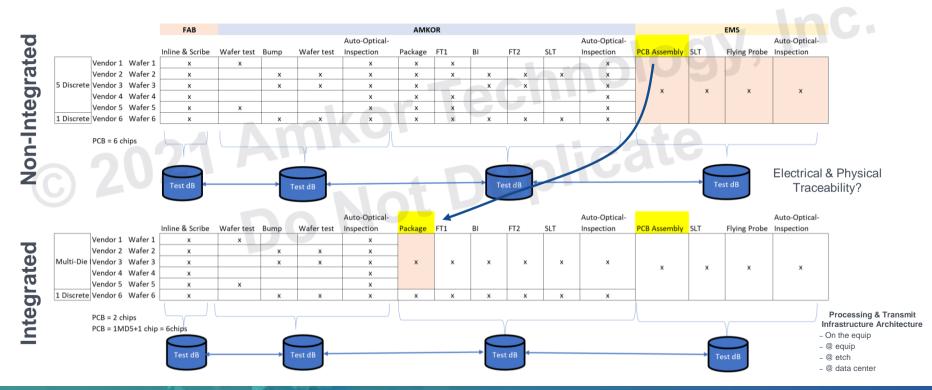


Non-Integrated

Integrated



Test Data Enabled Advanced Manufacturing





Amkor Test Services



24/7

Operation of fully networked test floors





2000+ Amkor, 300+ consigned



TESTED ANNUALLY

>6 Billion units
>6 Million wafers



Test Development

Software & hardware for probe, strip, final and system level test



Testing For Commercial, Industrial & Automotive Devices

Discrete, power, mixed-signal, memory, RF, MEMS and SiP devices

ACCURATE AND THOROUGH TEST SERVICES

Wafer probe, final test, strip test, film frame test, system level test, opens/shorts test, burn-in and complete end-of-line



Full End-of-Line Processing

Bake, scan, pack, ship and finished good services



Summary

- Dielet/Chiplet integration allows for scaling in the future
- Business continues to have cost and performance challenges
- ► Call to action advanced test methods
- Amkor is the industry leader in advanced packaging and production test solutions







Thank You

George Harris, george.harris@amkor.com

Learn more: https://amkor.com/test-services/

amkor.com









Thank you sponsors!

ADVANTEST®



SYNOPSYS®





Amkor's Differentiators





Technology

Advanced Packaging Leadership
Engineering Services
Broad Portfolio



Quality

QualityFIRST Culture Execution Automation



Service

Design & Test Through Drop Ship

Manufacturing Footprint

Local Sales & Support

Global Companies Rate Advantest THE BEST ATE Company 2021



Advantest receives highest ratings from customers in annual VLSIresearch Customer Satisfaction Survey for 2 consecutive years.

Global customers name Advantest THE BEST supplier of test equipment in 2020 and 2021, with highest ratings in categories of:

Technical Leadership – Partnership – Trust – Recommended Supplier – Field Service

"Year-after-year the company has delivered on its promise of technological excellence and it remains clear that Advantest keeps their customers' successes central to their strategy. Congratulations on celebrating 33 years of recognition for outstanding customer satisfaction."

— **Risto Puhakka**, President VLSIresearch

SYNOPSYS®

Silicon to Software™

COPYRIGHT NOTICE

This presentation in this publication was presented at the **Road to Chiplets: Data & Test** (November 9-11, 2021). The content reflects the opinion of the author(s) and their respective companies. The inclusion of presentations in this publication does not constitute an endorsement by MEPTEC or the sponsors.

There is no copyright protection claimed by this publication. However, each presentation is the work of the authors and their respective companies and may contain copyrighted material. As such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

www.meptec.org

