



Road to Chiplets: Data & Test

November 9 - 11, 2021



Road to Chiplets:
DATA&TEST

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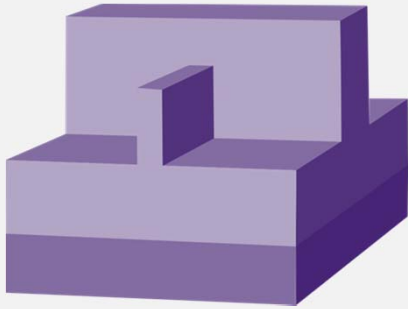
Using Data Analytics to Debug and Trace Multi-Chip Module (MCM) Test Failures During the Manufacturing Process for Reducing Overall Test and Manufacturing Costs

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Silicon Lifecycle Management (SLM)

November 2021

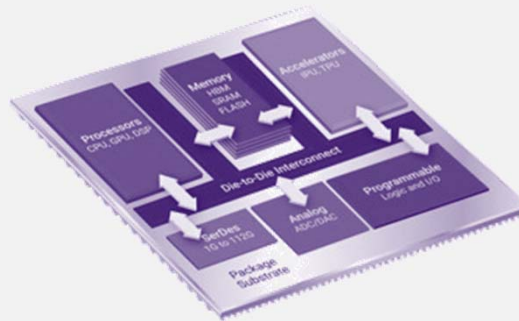
New Silicon & System Complexity Challenges

Scaling



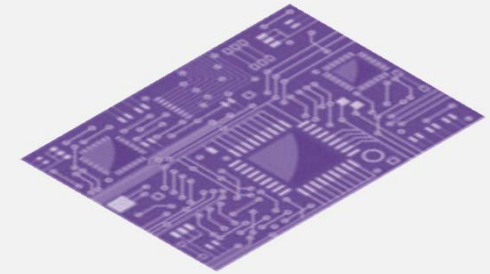
- Design size and complexity
- Transistor density
- Manufacturing variability

Packaging



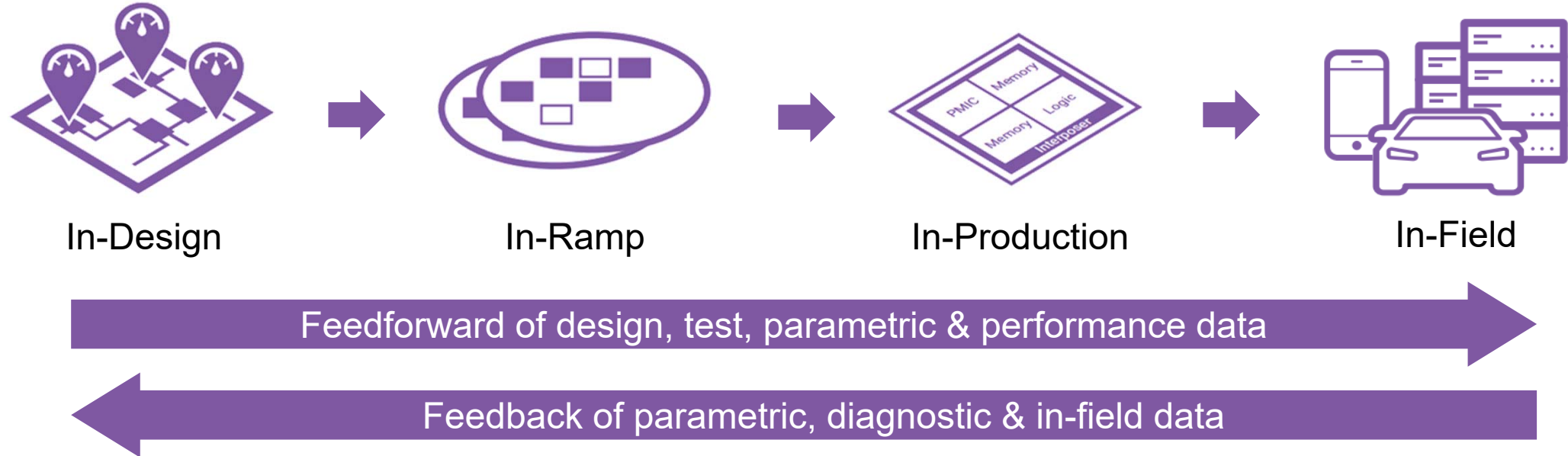
- Stacked die
- 2.5 & 3D Packaging
- Chiplets

System



- Data Aggregation & Security
- Ageing & Degradation
- Power & Computational throughput

SiliconMAX - Silicon Lifecycle Management (SLM) Platform



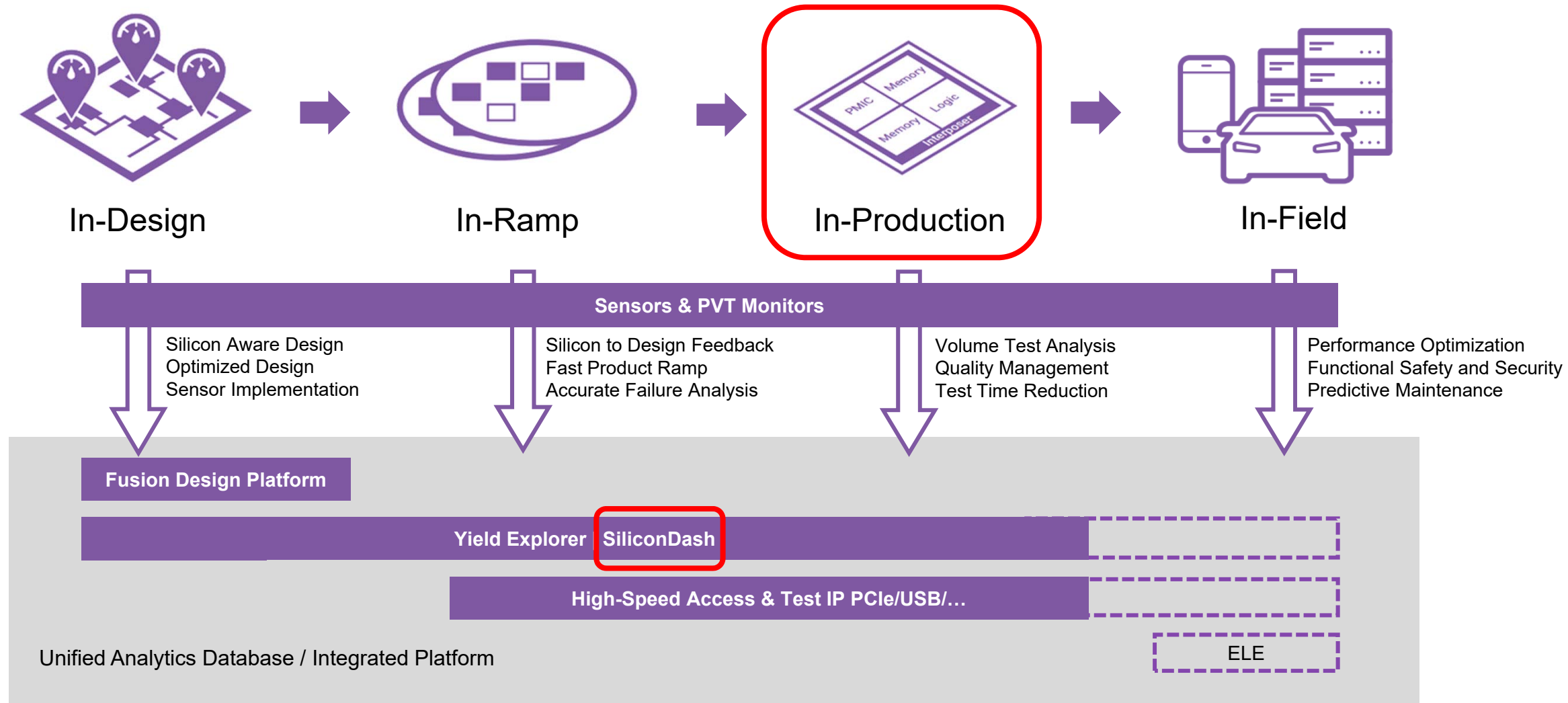
Actionable Insights Through Silicon Lifecycle Sensing and Analytics

Sensors
Data sources

Data
Unified database

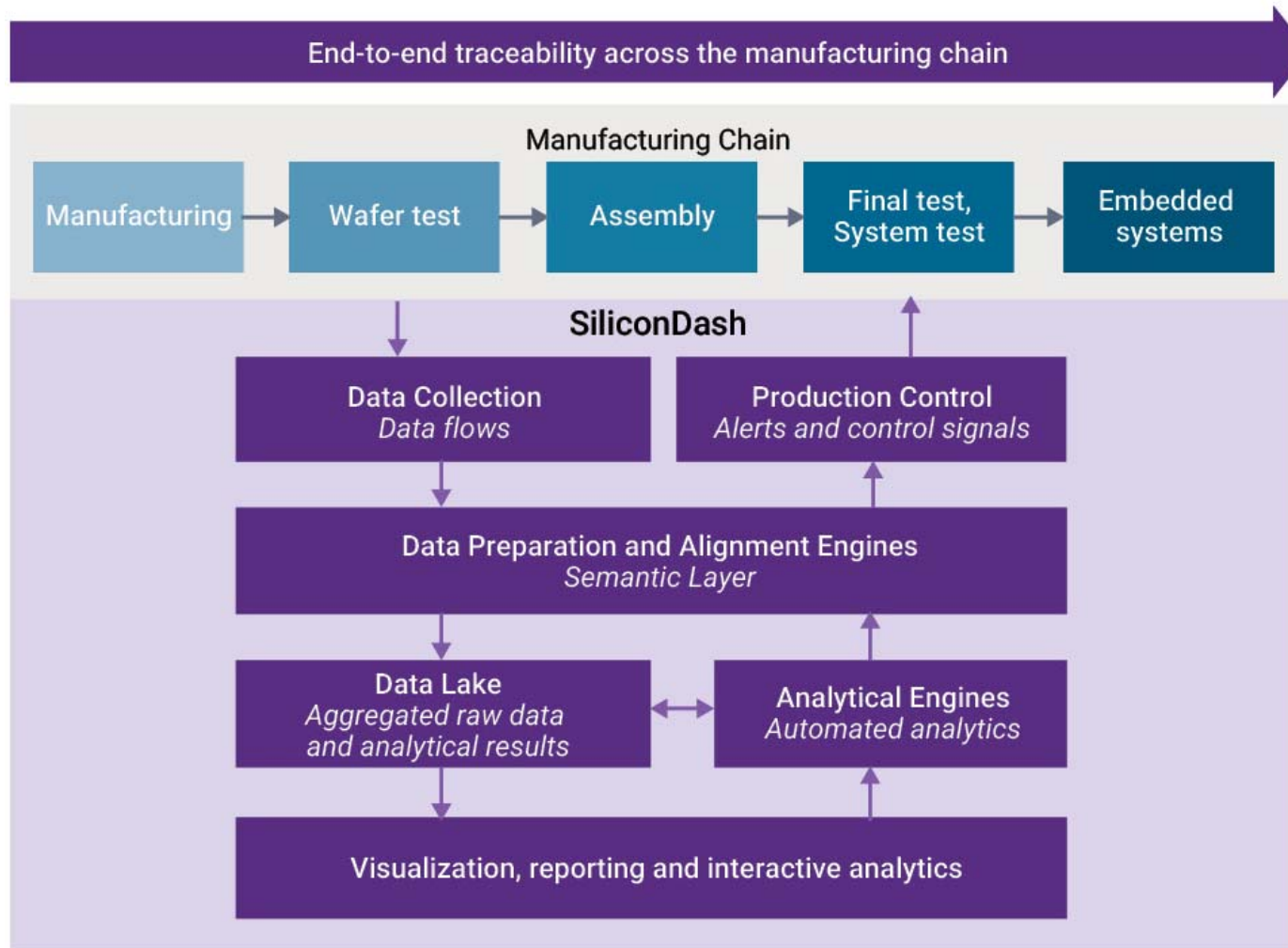
Analytics
Product optimization

SiliconMAX - Silicon Lifecycle Management (SLM) Platform



SiliconDash Overview

Next generation high-volume big data analytics solution for Fabless, IDMs, OSATs & Foundries



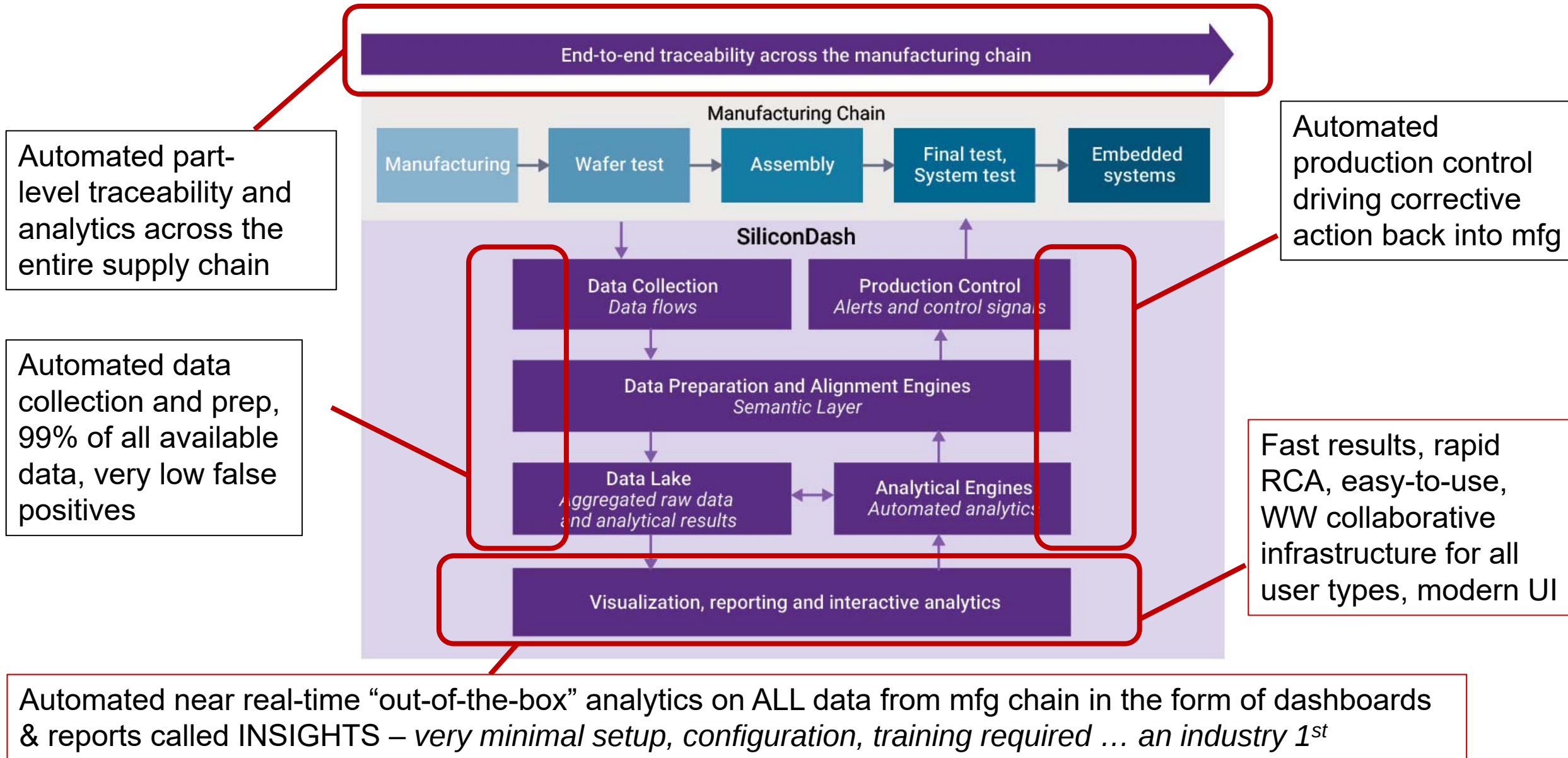
SiliconDash is:

- Automated Analytics
- Automated Reporting
- Automated Production Control

SiliconDash addresses:

- Quality Management
- Throughput Management
- Operations Management

SiliconDash Benefits



SiliconDash Insights

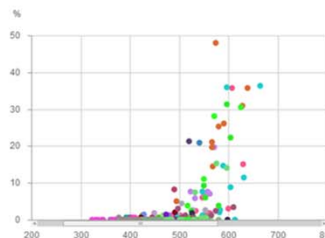
Automated near real-time analytics “out-of-the-box”

- Insights in the form of dashboards and reports on ALL incoming data from manufacturing chain
- Approximately 40 Insights available and consistently updating as new data streams in
- NO setup, configuration or training required ... *an industry 1st*

Small Sampling of Insights Provided within SiliconDash

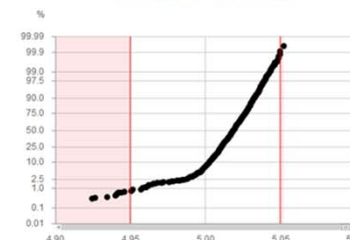
WAT – WS Correlation

WAT parameters that predict WS or FT binning



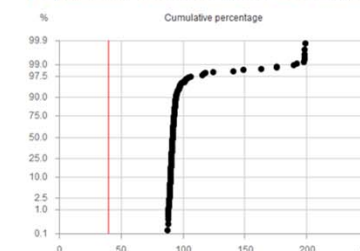
Distribution Tails

Parametric test results where the tail of the distribution is failing the test limit



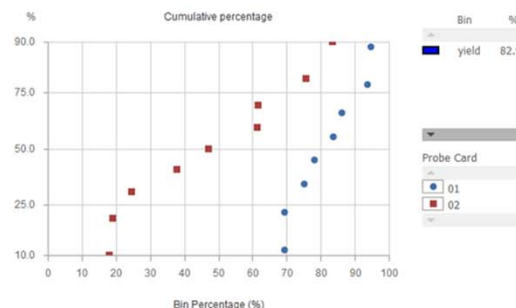
Wide Test Limits

Parametric test results where there are statistical outliers from the population but within the test limits



Test Equipment Dependency

Pass or failing bins that have a statistical dependency on the tester, probe card, test site, etc.



Consecutive Bin Fails

Stuck test sites that return the exact same failing bin for multiple consecutive results



Multi-Chip Modules (MCMs) / Chiplets Pose Unique Challenges

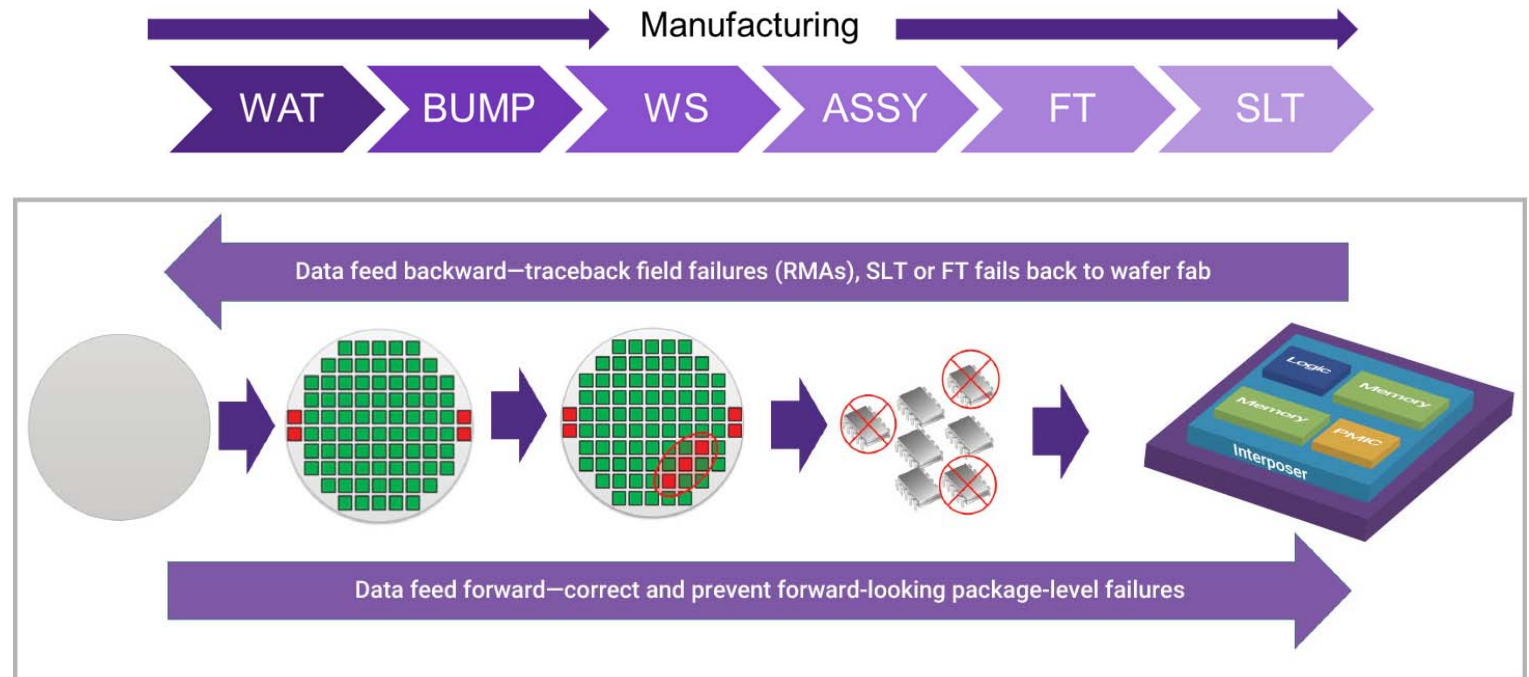
Goal is to find and correct issues as early as possible in the manufacturing chain

Challenges

- Only one failed die in an MCM causes the whole MCM to fail
- MCM packages are more costly to build and test vs single die packages
- Experiencing late stage systematic failures can be catastrophic if not resolved quickly

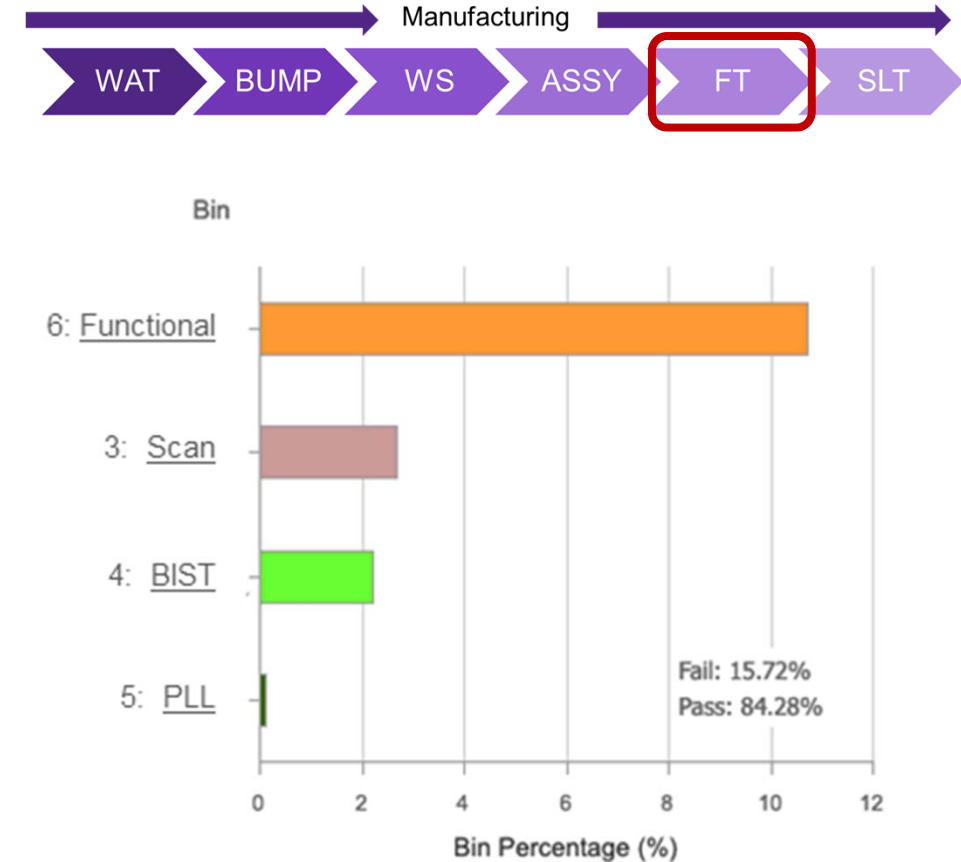
Requirements

- Electronic Chip ID (ECID) embedded within the die or a 2D barcode that is etched onto the substrate or marked onto the resin is required to do end-to-end traceability across the various manufacturing stages
- Ability to correlate tests across the various stages is critical to identifying sources of yield or quality issues
- Quality of each die within an MCM becomes critical



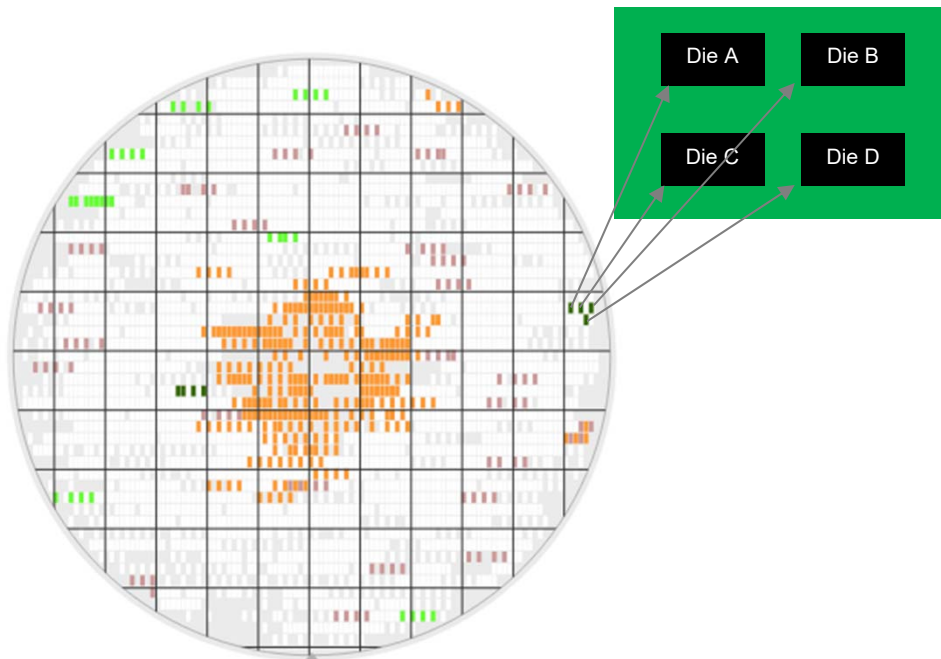
Customer Scenario

- Company was developing a 4-die MCM packaged product
- They were experiencing failures of their MCMs during Final Test (FT) which resulted in 84% yield
- The targeted yield requirement for this MCM product was not met
- Needed to debug and fix the problem ASAP as they were losing money and expending lots of cost on the failed MCMs
- From the failed bin analysis, it was evident that the majority of their FT failures were coming from Bin 6 which were the functional test failures



Geospatial Relationship

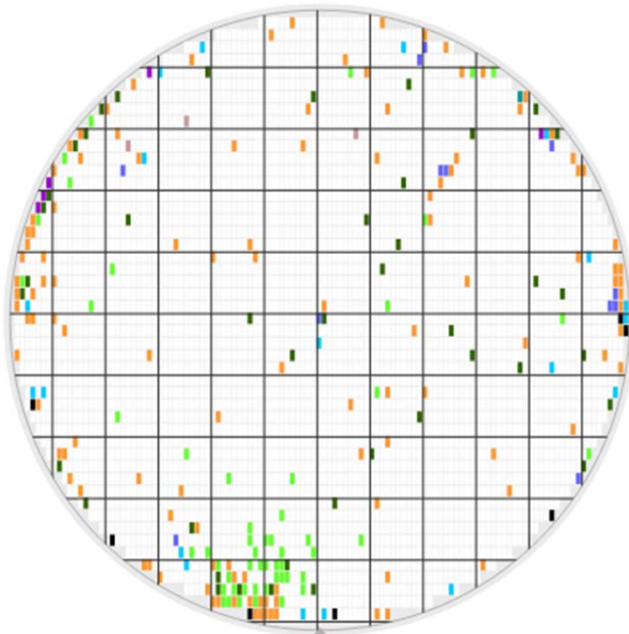
- ✓ Check if there is any geospatial relationship between these bin failure types and the location of where the dies originated from on their respected wafers before placed into their current MCM



- Dies from FT failed bin results are superimposed back onto a wafer map as shown here
 - ECID maps link the FT result back to the source die X/Y location
- Dies (**orange**) within the failed Bin 6 packages predominantly come from the center of the wafer map
- The surrounding dies are “**grey**” in color. This can mean any number of things but typically one of the following:
 - Not yet tested at the time that this analysis was performed
 - Used for a “different” product and not this particular 4-die MCM
 - Failed Wafer Sort testing, binned out and were no longer available
- Classic pattern of failure Clusters or Good Die Bad Neighborhood (GDBN) in and around the center of the wafer

Conclusion: Geospatial Relationship

- ✓ Double checking if it is Cluster or GDBN, let's take a closer look at how this particular wafer performed during Wafer Sort ... *expecting to see some center pattern of failed dies*



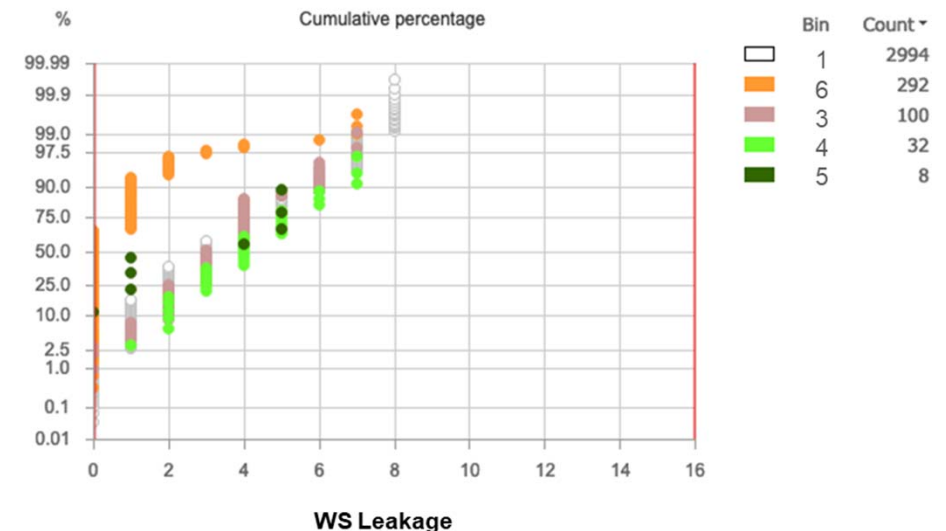
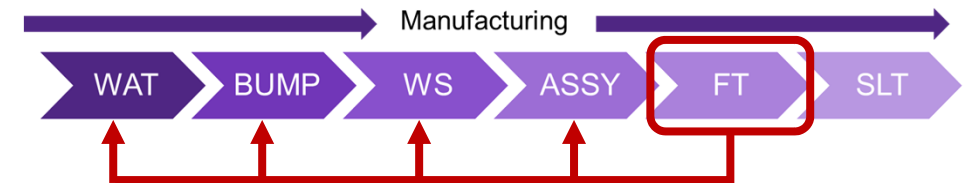
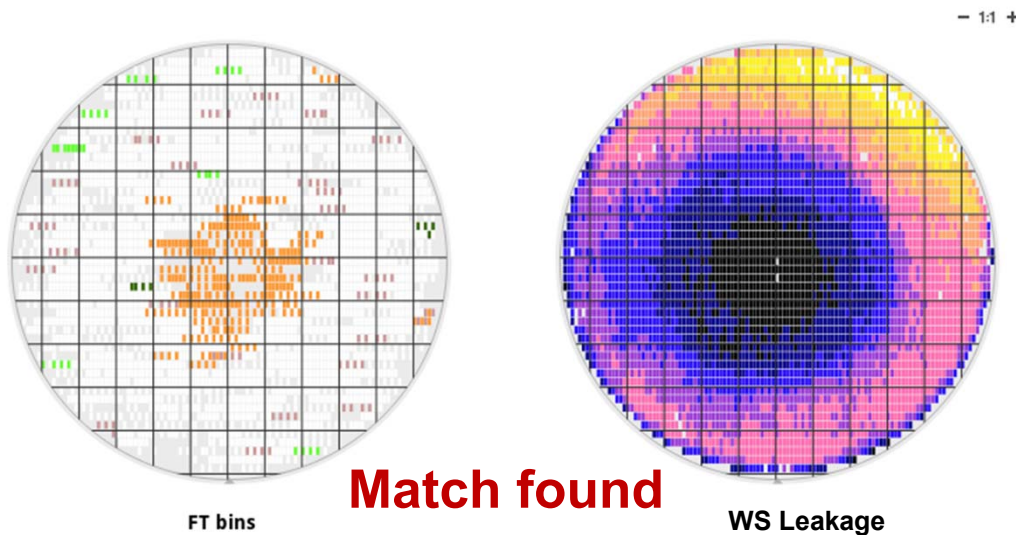
Composite view of all WS tests results performed on the dies within this wafer map



- **NO center pattern found ... assumption incorrect**
- Most of the dies in the center of the wafer passed all of their respective WS tests (denoted by the dies shaded in white)
 - These good dies at the center of the wafer did NOT fail WS
- This means one of two things occurred:
 - These corresponding good dies in white, that were also shown to be grey in the previous map containing the FT results, have NOT been tested yet if they belong to the same MCM product
 - Or they were put into a different product altogether that is not shown (note the previous map were the FT results of only this one MCM product)

Parametric Correlation

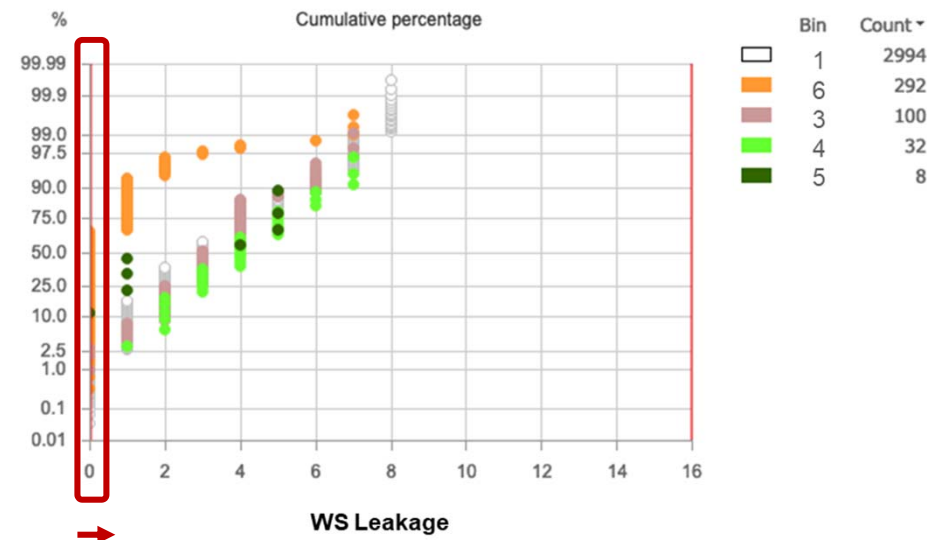
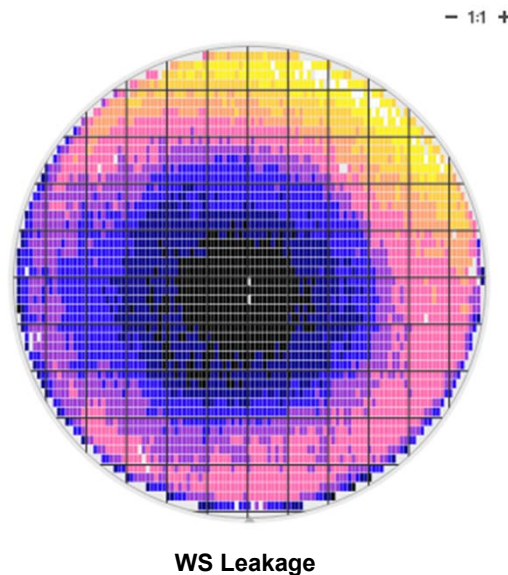
- ✓ Automatic push button correlation for feed backward analysis used to correlate the FT ECID module failed binning results against all available manufacturing test data
- ✓ Goal is to look for an upstream parameter that can predict this downstream issue at FT



- Tool found a leakage current test at WS that could predict the FT Bin 6 failures
- Plot reveals the failed dies at FT mostly measured at the lower spec limit of the current measurement

Conclusion

- With a single click, SiliconDash was able to identify an upstream parameter in the form of a leakage current test at WS that could predict these FT module bin failures
- The color scheme in the wafer map below is indicative of a “cold” (slower performing) center and radially increases in temperature (faster performing) as it goes outward towards the outer edge of the wafer
- Corrective action would be to raise the lower level limit to something greater than 0 mA to bin out those dies that have very low leakage and thus are performing too slow and are failing FT



Brainstorming – Future Considerations

- MCMs containing chiplets/dies of the same design that are randomly grouped together will be suboptimal
 - Weakest chiplet/die will determine the MCM's top performance and quality
- Concept: automated & intelligent grouping of chiplets/dies for assembly
 - Performance based: grouping fastest performing dies together, offer at a premium
 - Quality based: grouping most stable dies together (center of the histogram) for quality sensitive applications (automotive, datacenter, etc), offer at a premium
- SiliconDash does not offer this today but has the capabilities to do so
- Customers today, however, who have a biased process towards identifying dies that are optimal for power, performance, quality or reliability can provide their own scripting within SiliconDash to accomplish this

Thank You



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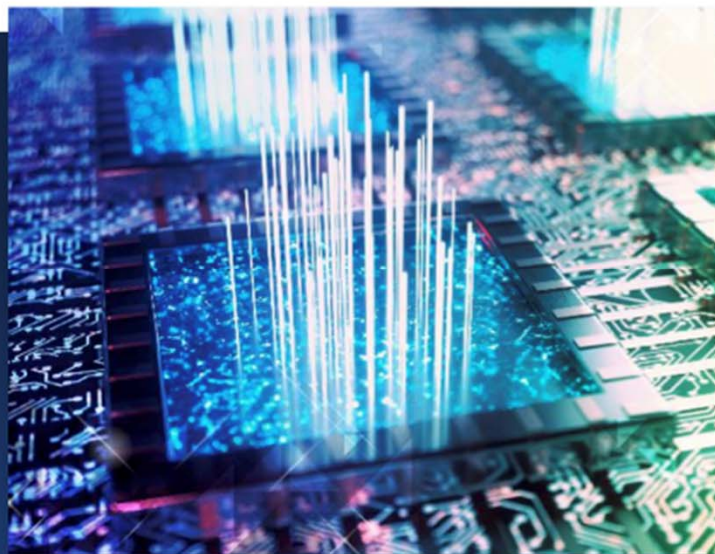
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