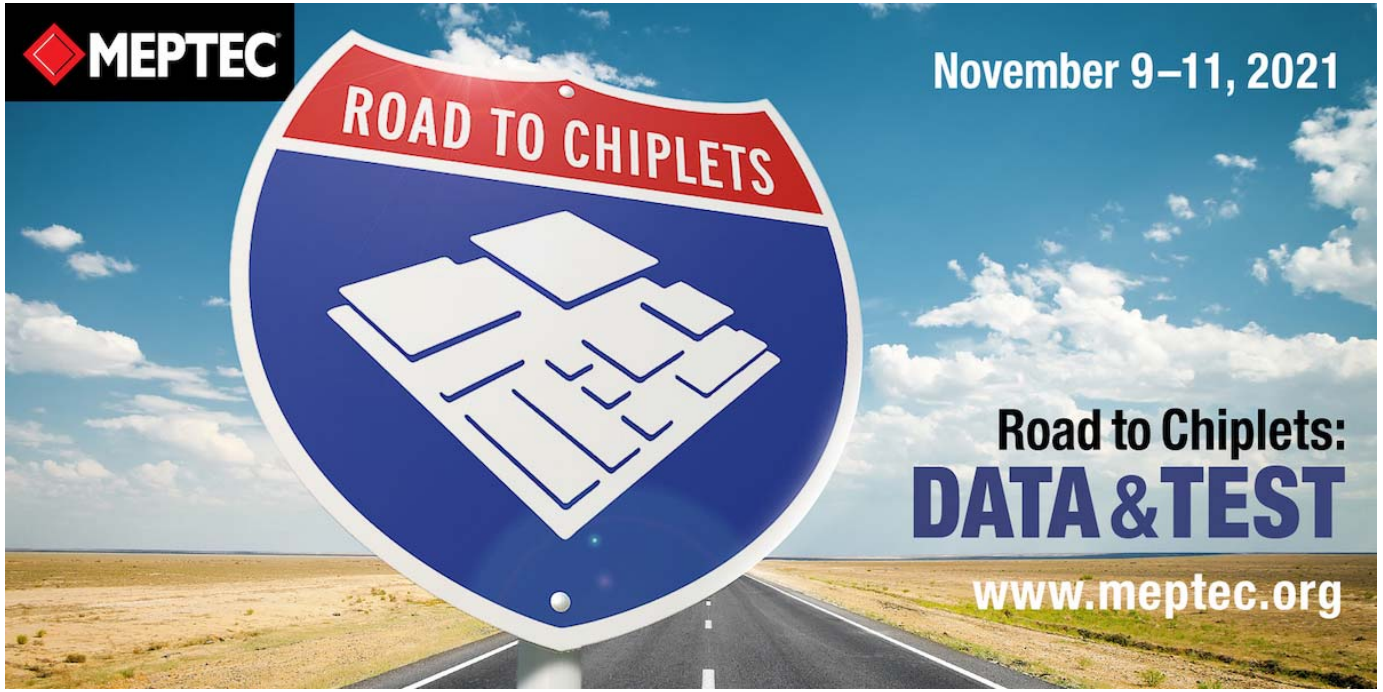

Road to Chiplets: Data & Test

November 9 - 11, 2021

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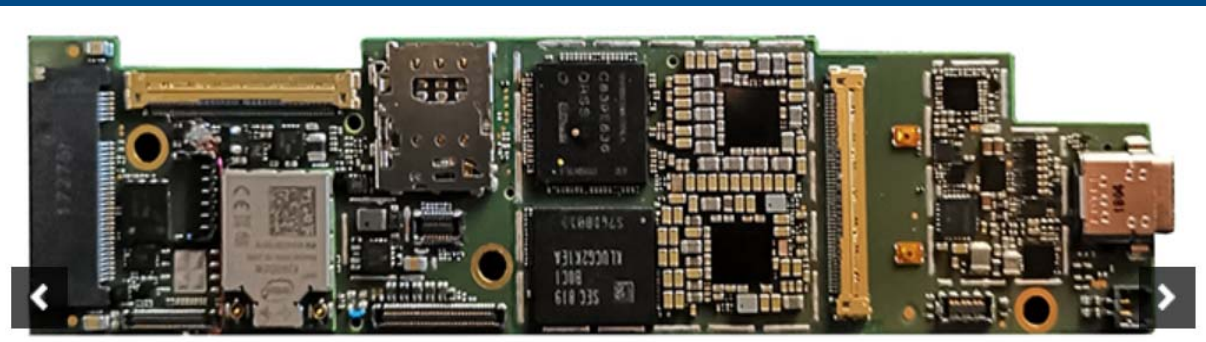
Dr. Sreejit Chakravarty, IEEE Fellow and Principal Engineer, Intel Corporation

Chip-lets Interconnect Test Challenges

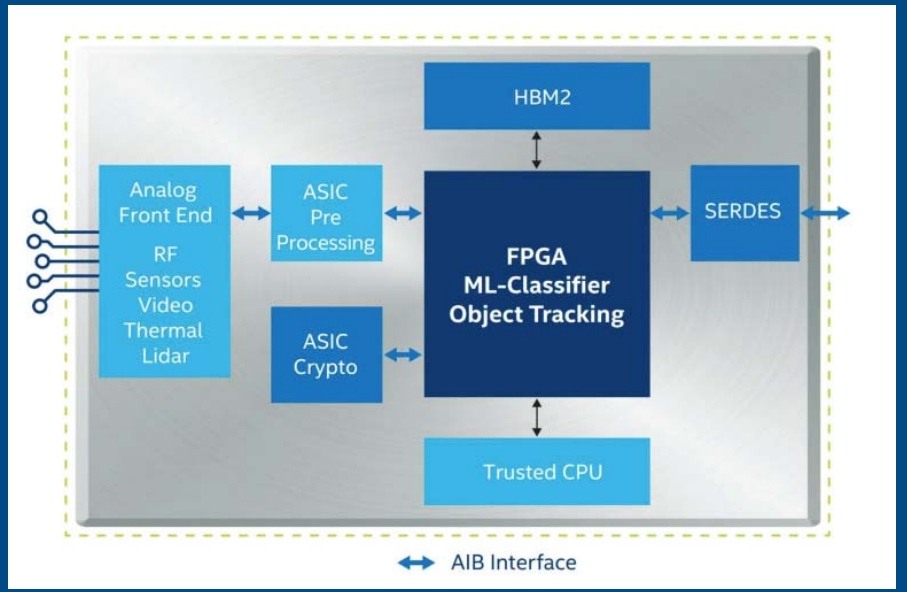
CHIPLET INTEGRATION EXAMPLES

- LAKEFIELD – Foveros
- 3D
- [Source: LKF-IntelNewsRoom]



At CES 2019, Intel Corporation previews a new client platform code-named "Lakefield." If features a hybrid CPU architecture with Intel's Foveros 3D packaging technology. Lakefield has five cores, combining a 10nm high-performance Sunny Cove core with four Intel Atom processor-based cores into a tiny motherboard for thin and light devices packed with performance, long battery life and connectivity. Intel displays how its technology is the foundation for the world's most important innovations and advances at CES 2019 from Jan. 8-11 in Las Vegas. (Credit: Intel Corporation)

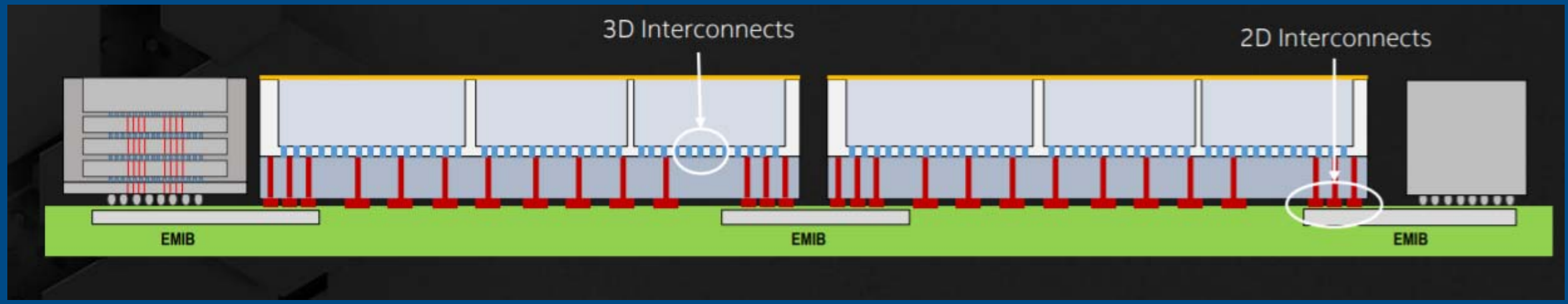
- Programmable Devices –AIB
- 2.5D
- [Source: AIB-WhitePaper]



Source [Mahajan Keynote]

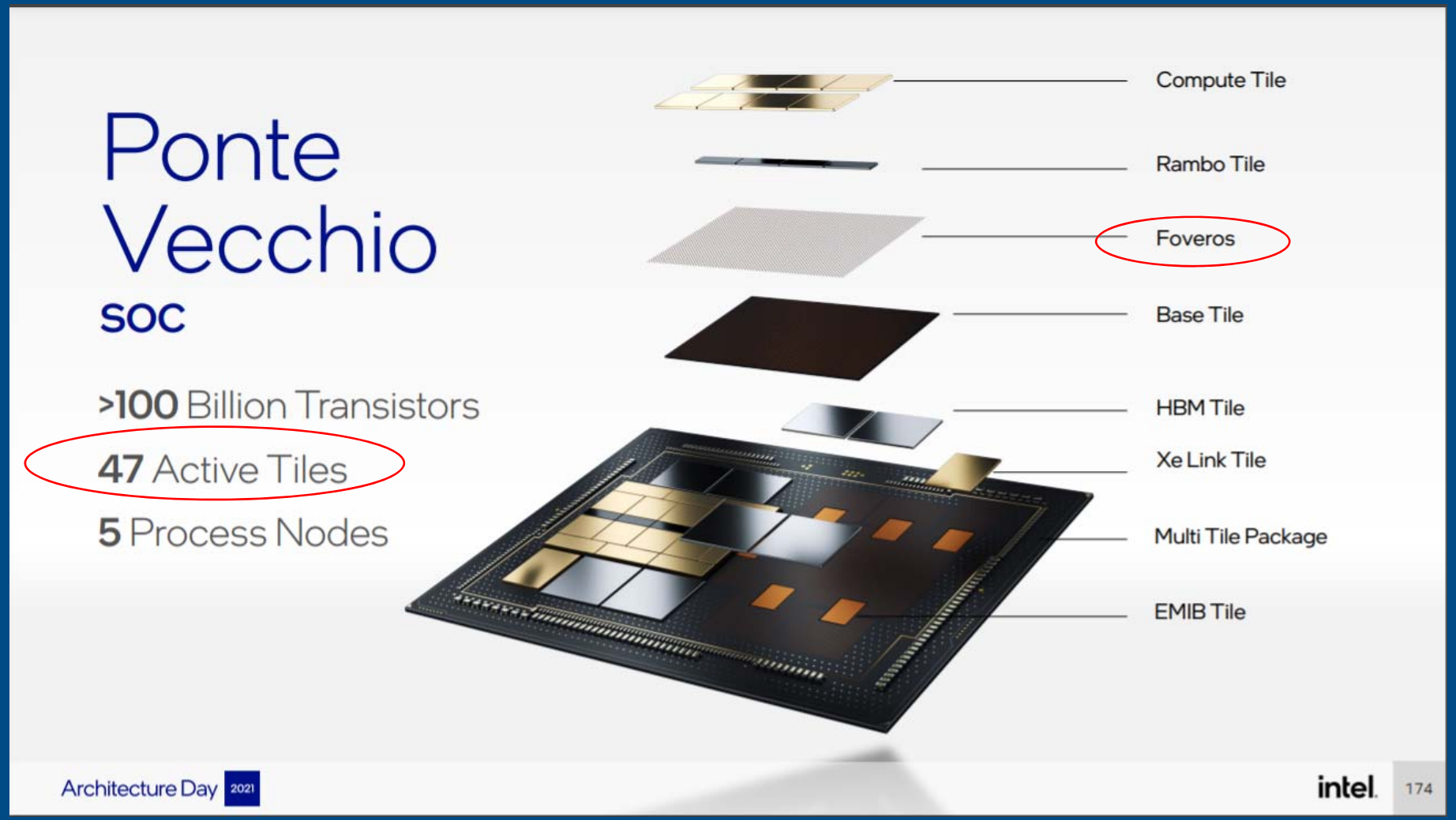
CHIPLET INTEGRATION EXAMPLE

- "Big Iron Compute" Products often combine 2.5D and 3D interconnect technology



SOURCE: IntelArchPressRelease_2021

BIG IRON COMPUTE ENGINEs



CHIP-LET INTERCONNECT

- Logic-on-logic die stacking
  - Face-to-Face micro-bump connections

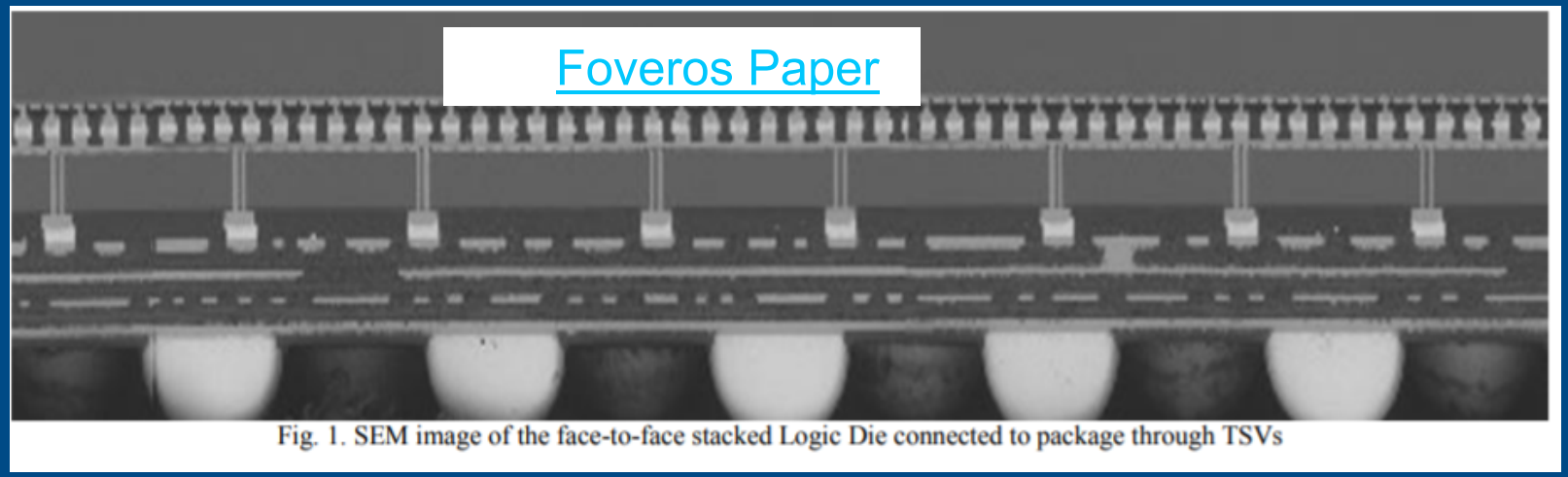
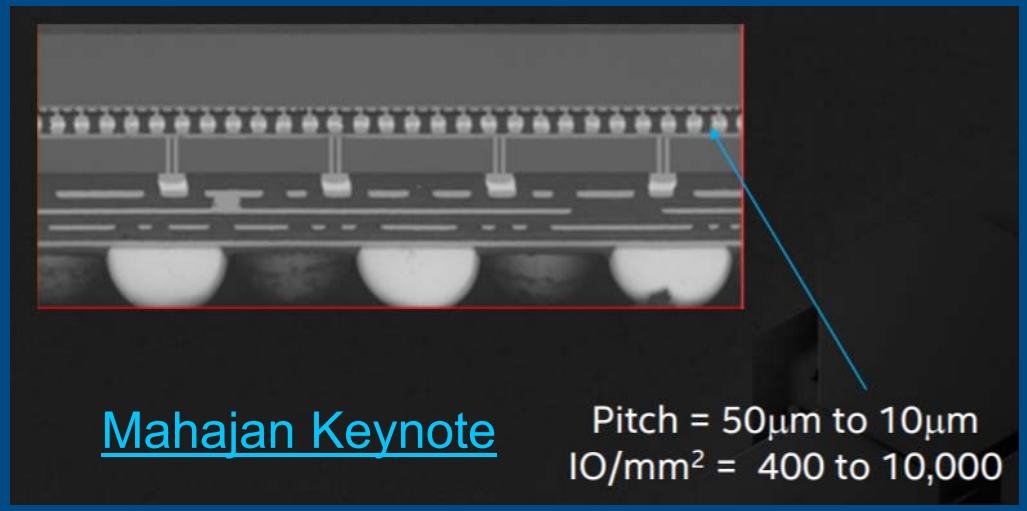
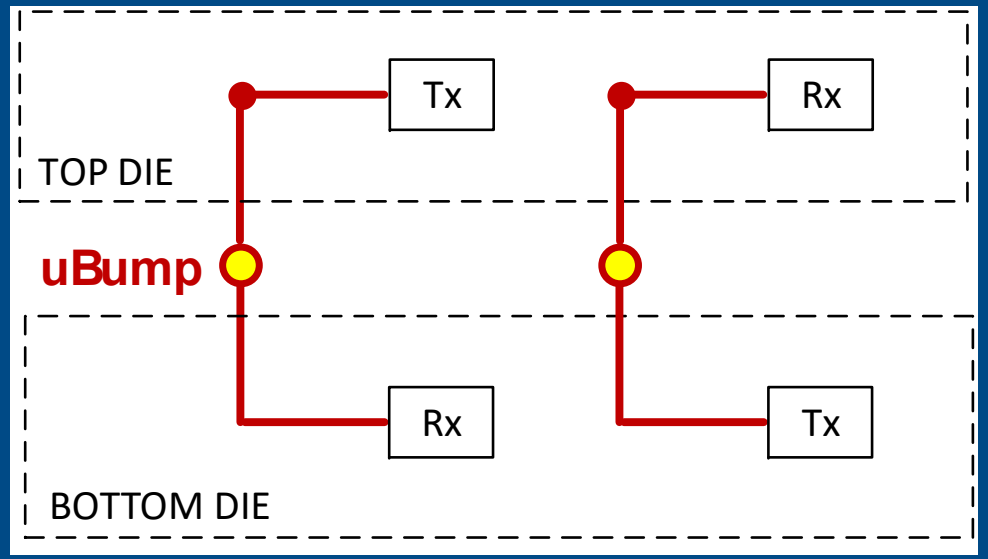


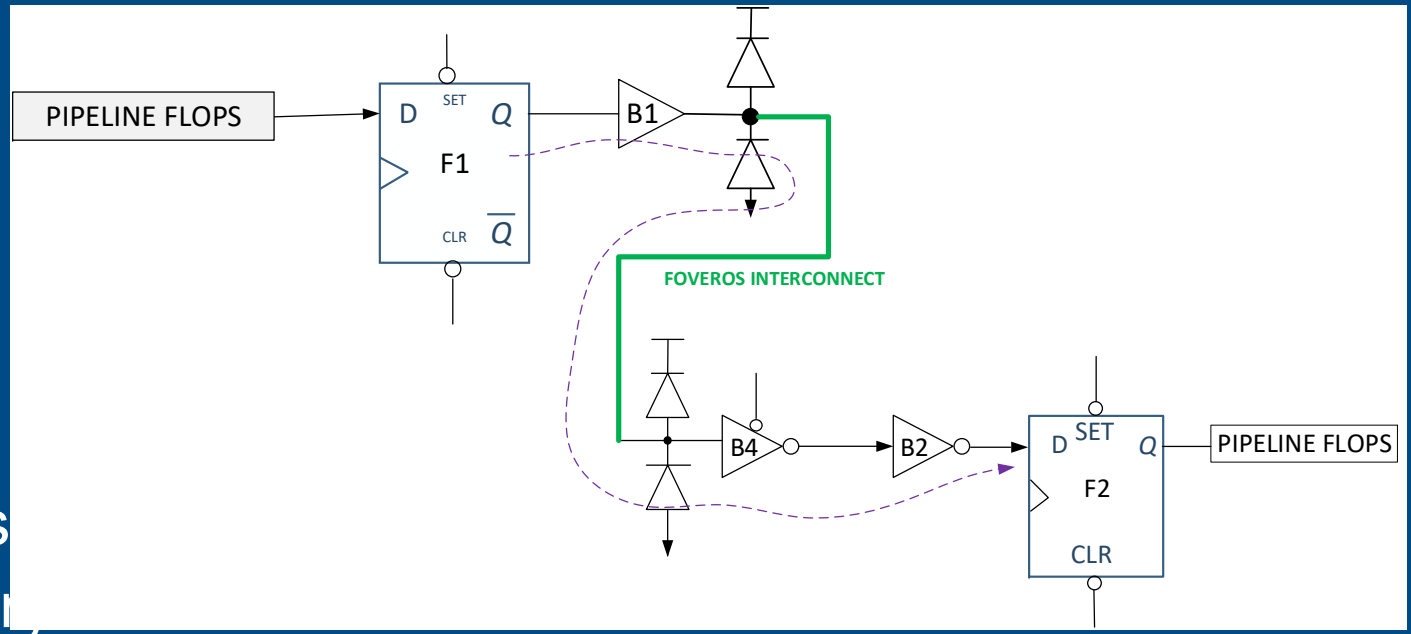
Fig. 1. SEM image of the face-to-face stacked Logic Die connected to package through TSVs





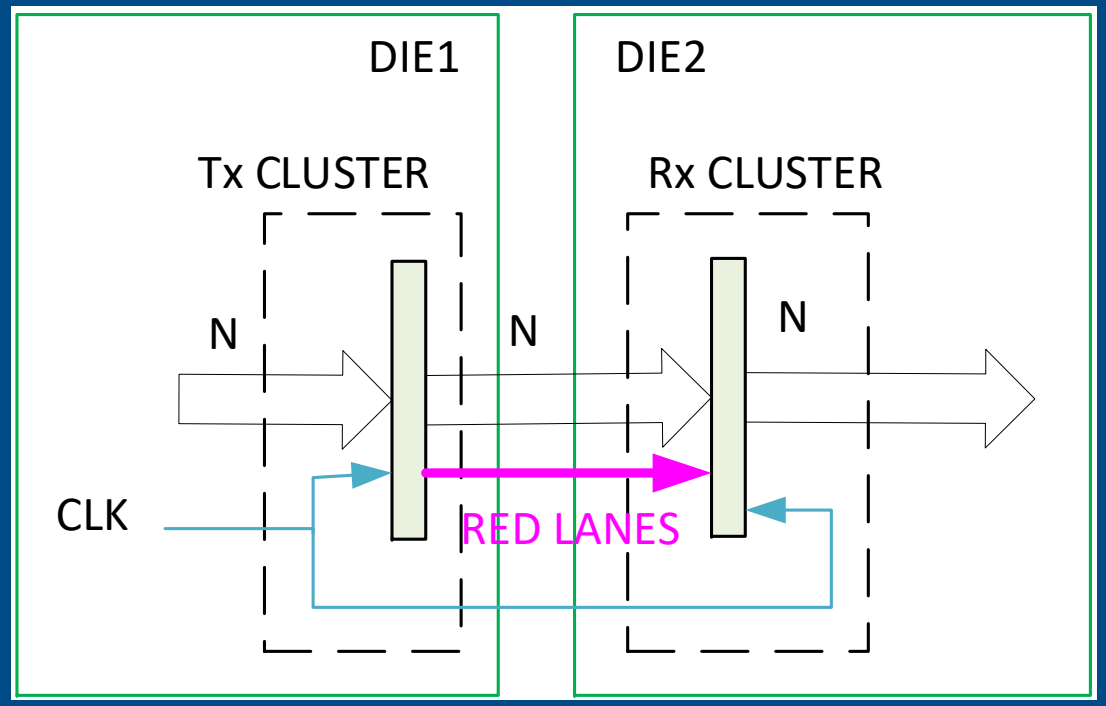
CHIP-LET INTERCONNECT TEST PROBLEM

- Simple Circuit. But ….
- Challenges
  - No touch test
  - Large numbers
  - High density
  - Complicated failure mechanis
  - High failure rate, yield recover and repair
  - Fault isolation and debug
  - ……

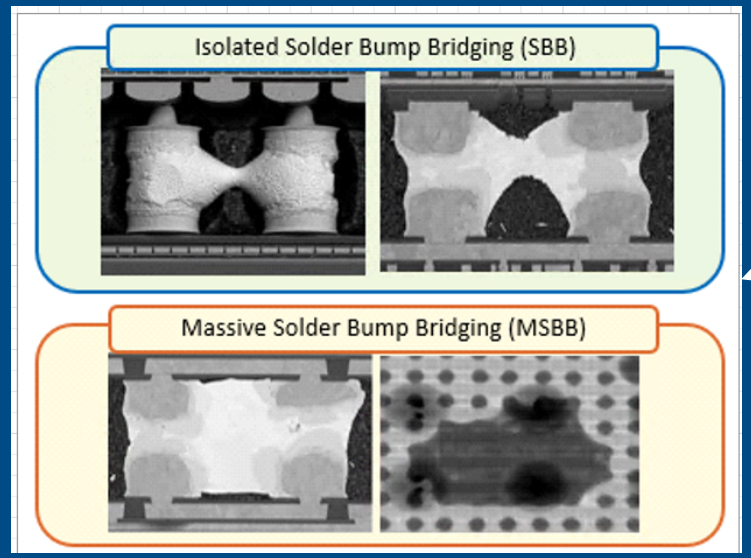


CHIP-LET INTERCONNECT CLUSTERING

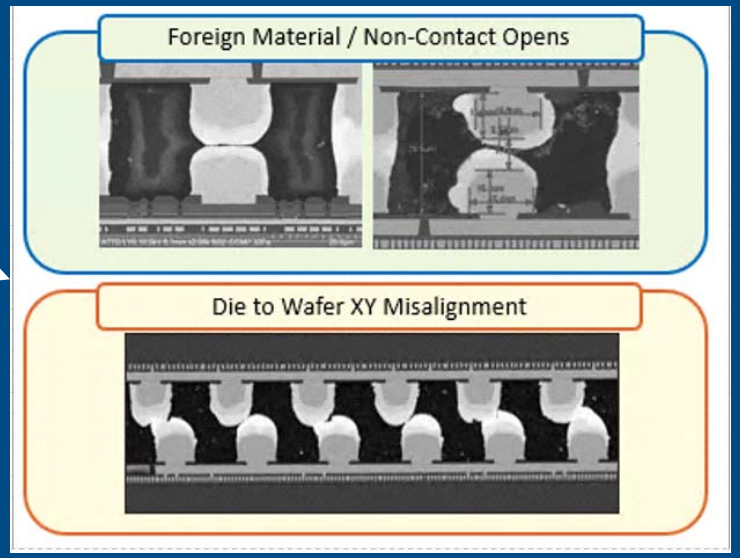
- Wide? Each interconnect uses many signals – 100s of them
- Wide busses divided into clusters
  - Constrained by clock distribution/timing closure
  - 36, 48 signals per cluster
- Common clock
- Repair Infrastructure
  - Redundant Lane
  - Repair Signature
  - Repair Muxes
  - Support for Clock Testing

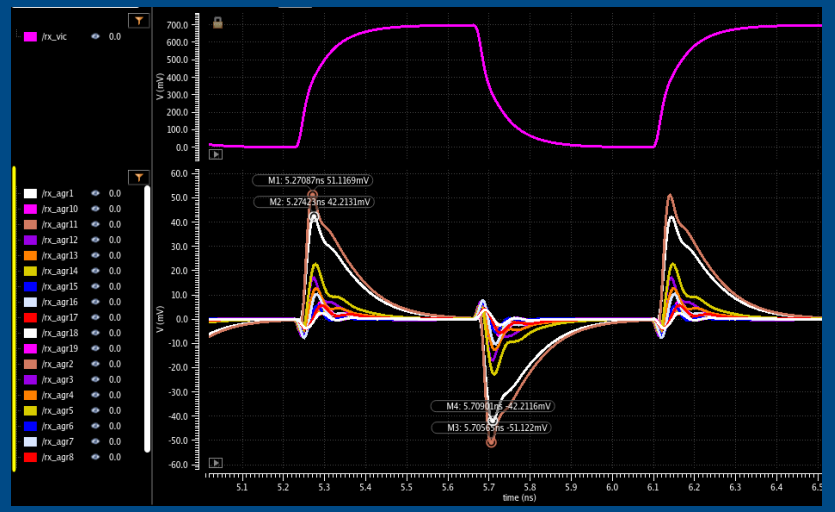


WHAT CAUSES INTERCONNECTS TO FAIL?



PHYSICAL: DEFECTS
[X-Ray]



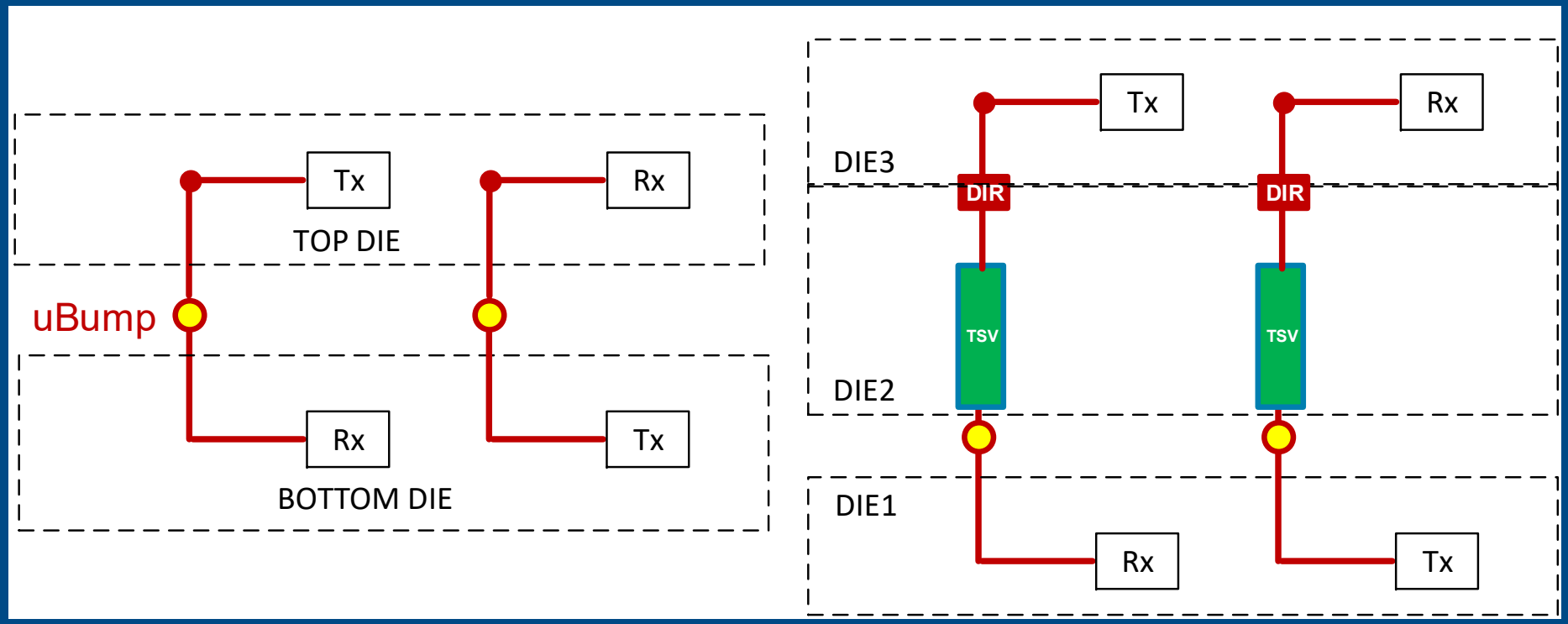


COUPLING
[Spice Simulation]

WHAT CAUSES INTERCONNECTS TO FAIL?

- Vcc/Vss shorts quite significant
  - Cannot be addressed during high volume manufacturing – Or, can it be?
  - Addressed through physical design rules
- Defects targetable during High Volume Manufacturing (HVM) Tests
  - ~1/3 Shorts between signal and Vcc/Vss
  - ~1/3 Shorts between 2-signal line
  - Slightly less than 1/3 multiple line shorts
  - ~5% opens
- Short between clock and signal
- Shorts across clusters
- Coupling Failures
- X-ray based defect locations
  - Cannot differentiate between hard/resistive shorts
  - Cannot identify coupling issues

EVOLUTION OF CHIP-LET INTERCONNECTS



TREND

- 2 die stacking to multi-die stacking
- µBump to combination of µBump + DIR + TSVs ++
- Die-Die versus Wafer Stacking

- Pitch: 50µm to < 10µm
- Signal Frequency: 2 to 3 Ghz
- Lane count: 500 to 75,000

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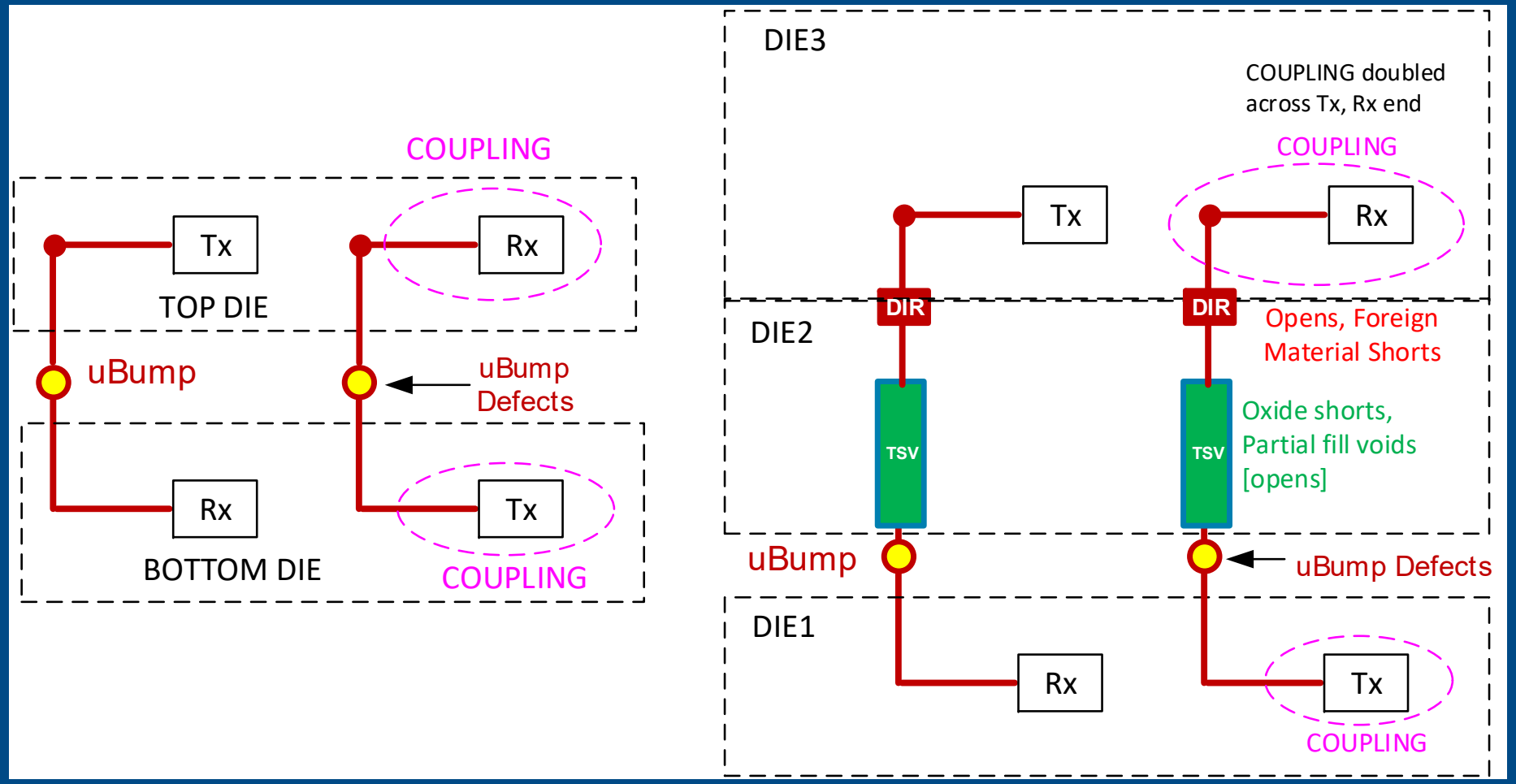
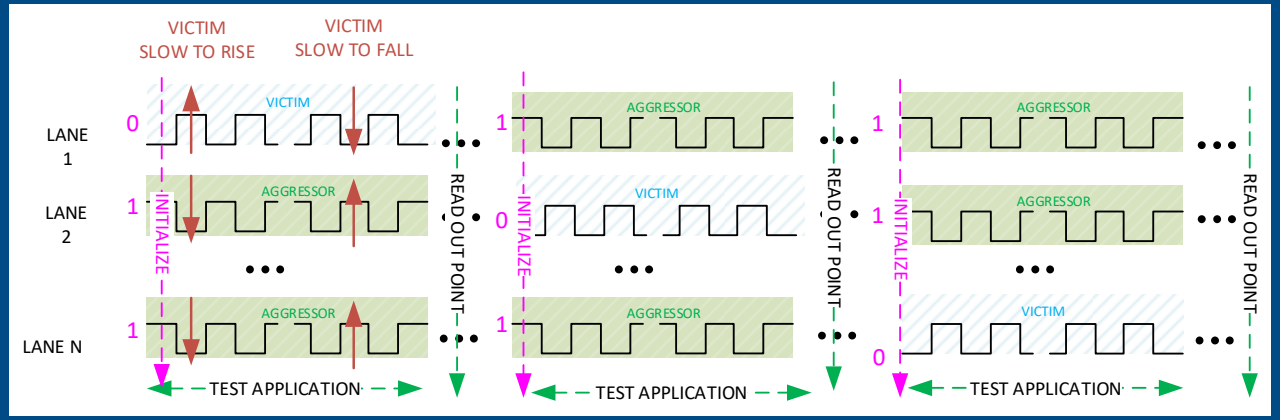
EVOLUTION OF CHIP_LET INTERCONNECT DEFECTS



TREND

INTERCONNECT TESTS

- LFSR Based tests have been the main stay of IO testing
- LFSR based tests will not be adequate
- More deterministic tests are needed



Pass/Fail Test Scorecard				
Defect		**speed**	**LFSR**	**DET STRESS**
Lane Open	Complete	slow		
	Partial	at-speed		
Lane to Power Short	Hard	slow		
	Resistive	at-speed		
Lanes Short	Hard	slow		
	Resistive	at-speed		
Lane to CLK	Hard	slow	??	??
	Resistive	at-speed	??	??
Coupling		at-speed	Unlikely	

ADDITIONAL INTERCONNECT TEST CONSIDERATIONS

- Single Data Rate, Double Data Rate
- Cluster level repair considerations
- On-die test and repair – analogous to Array test and repair
  - Recommended
- Slow and at-speed, non-destructive, diagnosis capability
  - Identify fault location – which die? interconnect?
- System Level Test
- Clocking
  - Single Data Rate, Double Data Rate
  - Inter-lane skew measurement
  - Clock duty cycle modification tests
  - Clock Repair
  - Synchronous, Asynchronous
- InField Test and Repair
  - Aging Related Failures
  - Increases availability

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INTEROPERABILITY AND STANDARDS

- DWR concept in IEEE 1838 standard is inadequately to address the wide interconnect test problem
- A new standard, supporting interconnect test problems highlighted, is required

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