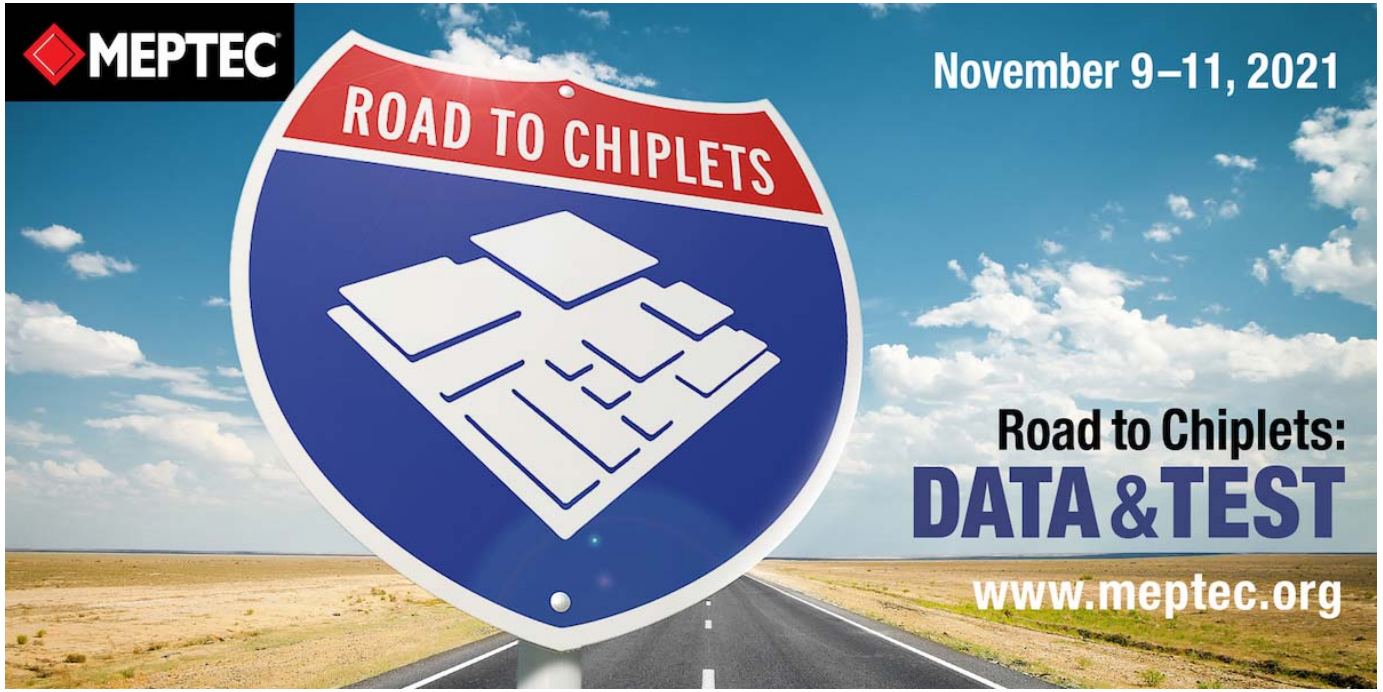

Road to Chiplets: Data & Test

November 9 - 11, 2021

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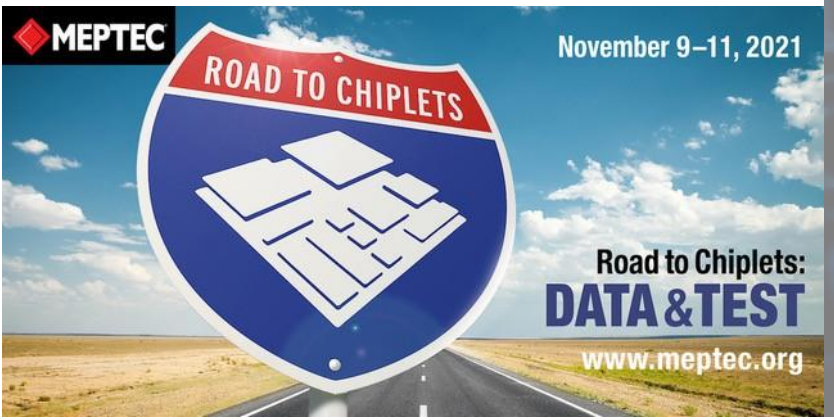
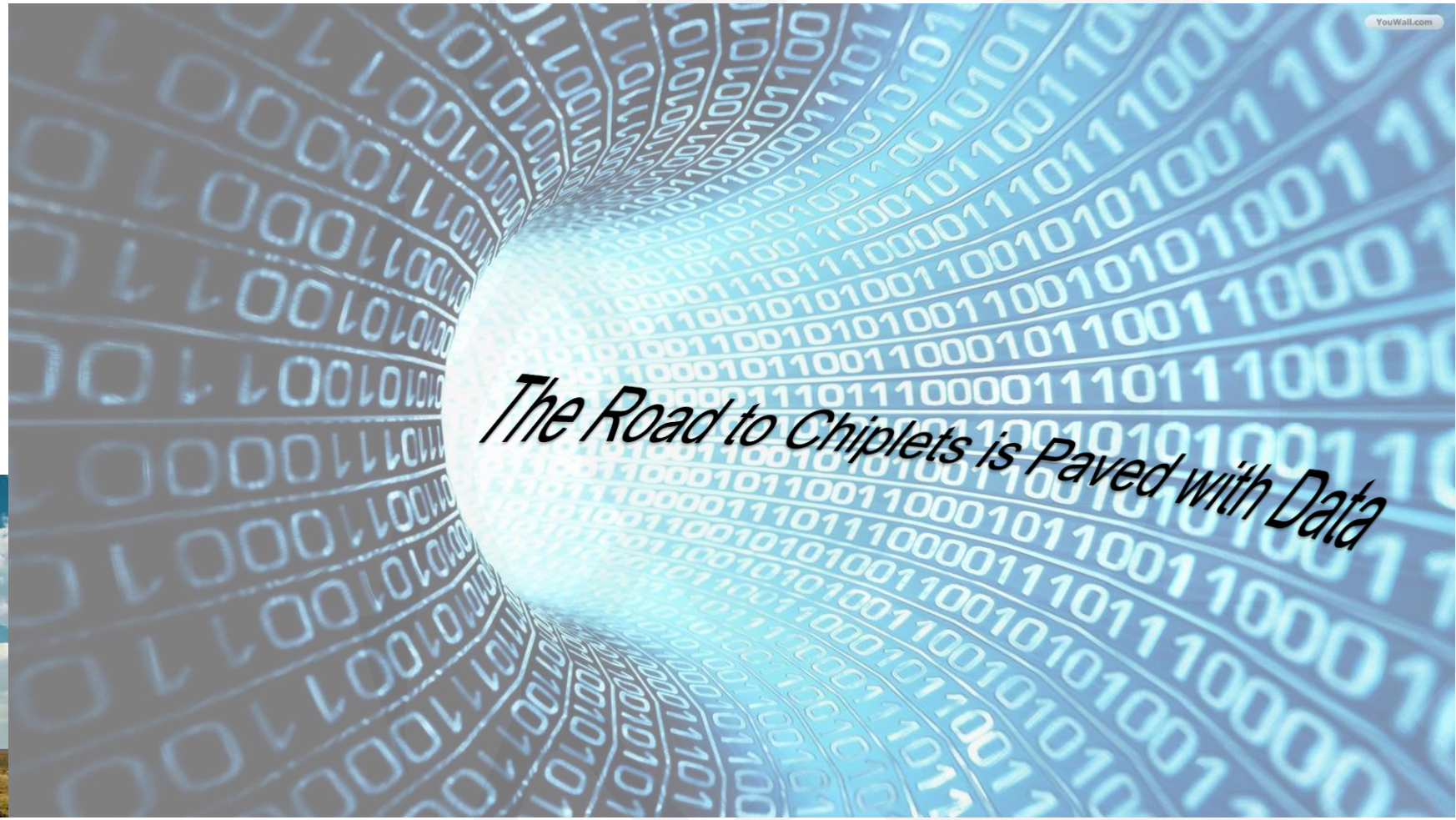
Ken Butler
Strategic Business Creation Manager
Advantest





Advantest Cloud Solutions™

Data Growth: The Tyranny of Numbers

For some time now, electronic man has known how 'in principle' to extend greatly his visual, tactile, and mental abilities through the digital transmission and processing of all kinds of information. However, all these functions suffer from what has been called 'the tyranny of numbers.' Such systems, because of their complex digital nature, require hundreds, thousands, and sometimes tens of thousands of electron devices.

– Jack Morton, VP, Bell Labs, June 1958

Jack Morton NAE page

Fast forward to modern times

In 2014, semiconductor production facilities made 250 billion billion (250 x 10^{18}) transistors. [2021 figure is 1.6x10^{21}]. This was, literally, production on an astronomical scale. Every second of that year, on average, 8 trillion transistors were produced. That figure is about 25 times the number of stars in the Milky Way and some 75 times the number of galaxies in the known universe.

– Dan Hutcheson, CEO, VLSI Research, April 2015

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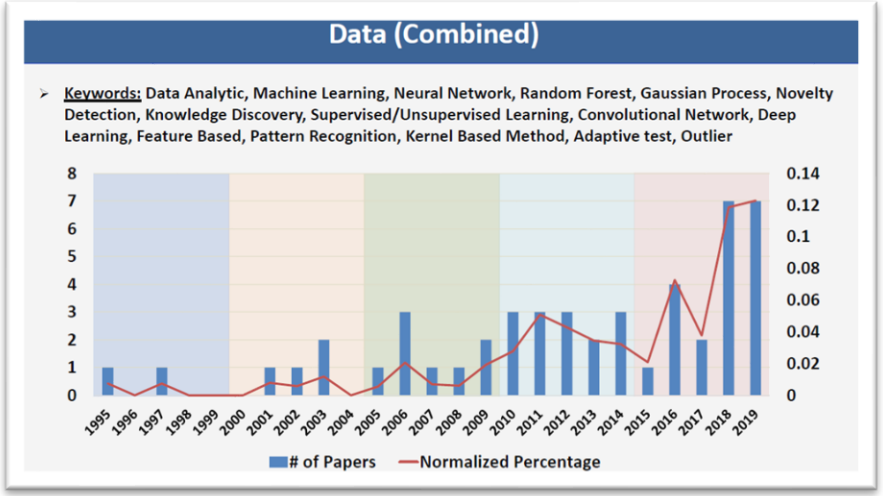
How much test data does generate?

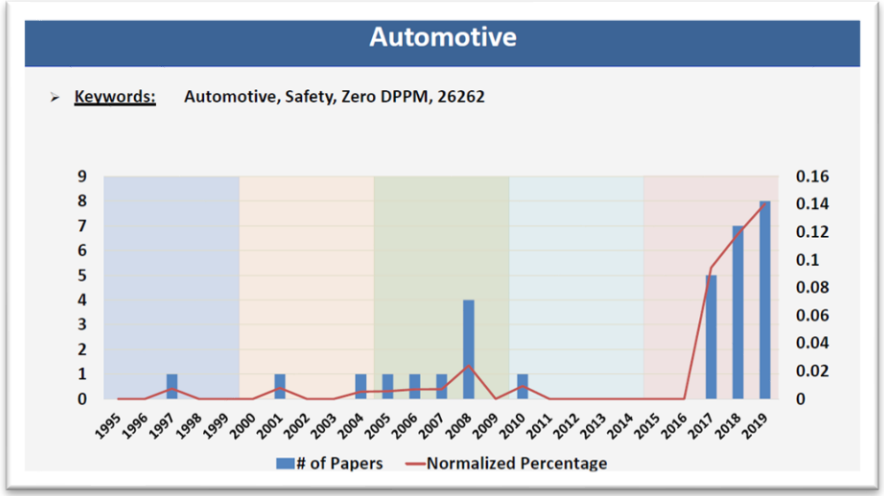
Assuming only 80% of the transistors are tested and each transistor results in just one bit of data, that is >40 Tb per second in 2021!

More Trends Challenging to Test

Trend	Challenges
Growth in automotive sector	• "Zero defects" or parts or billion test escapes • Extended temperature operation • Reliability requirements
Manufacturing disaggregation	• Data movement and data sharing • Information/IP protection
Growth in machine learning/AI methods	• Test time • IP protection
Advanced lithography	• New defect mechanisms • Subtle failures
On-premise to cloud-based solutions	• Data and IP protection • Analytics performance in some applications



International Test Conf analytics papers



International Test Conf automotive papers

Chiplets Impact on Test and Data

Many aspects of test and data influenced by chiplet-based products

- **Larger systems within a package – the amount of test data goes up dramatically**
- **Known good die – ensure that each chiplet is completely functional before integration**
- **Die traceability**
  - Debug, root cause analysis, and in some cases die matching
  - Need improved collection and communication of origin of each chiplet
- **Functional test content (not using design for test [DFT] structures) and system level test increasing**
  - Electrical failure analysis is more complex and data-intensive
- **Need to migrate more test content earlier in the flow**
  - Detect defective units earlier prior to integration, decrease end of line yield loss
  - Requires more correlation work to identify tests at wafer that detect downstream system level failures

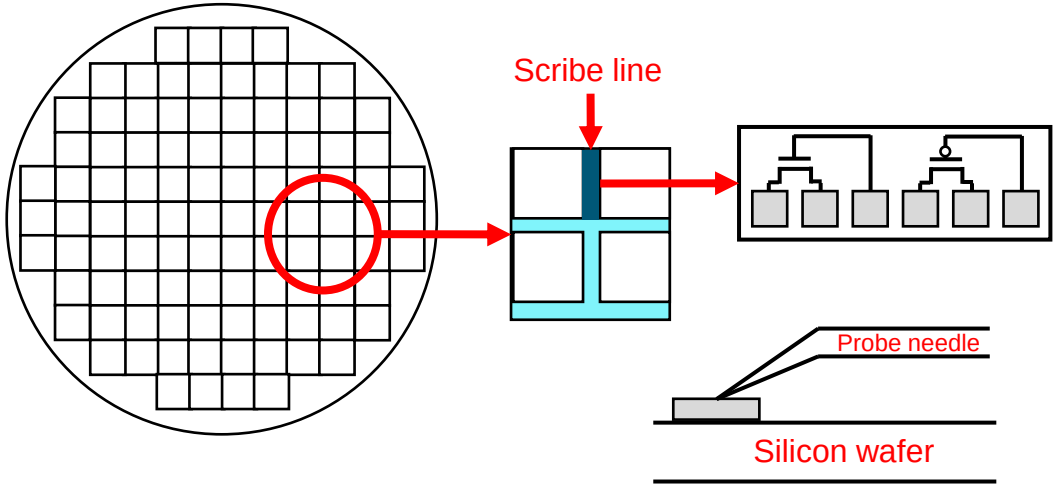
What Are Product Teams Asking For?

Some examples

- **Adaptive e-test solution**
  - Optimize data collection at wafer parametric test
  - Automate root cause analysis, increase throughput at e-test operation
- **Real-time analytics, especially with ML workloads**
  - Speed up complex analytics
  - Improve yield and quality while optimizing test cell utilization
- **Rapid scan or other failure isolation**
- **Screening and real-time test solutions for automotive, other quality-sensitive products**

What Exactly Is E-Test?

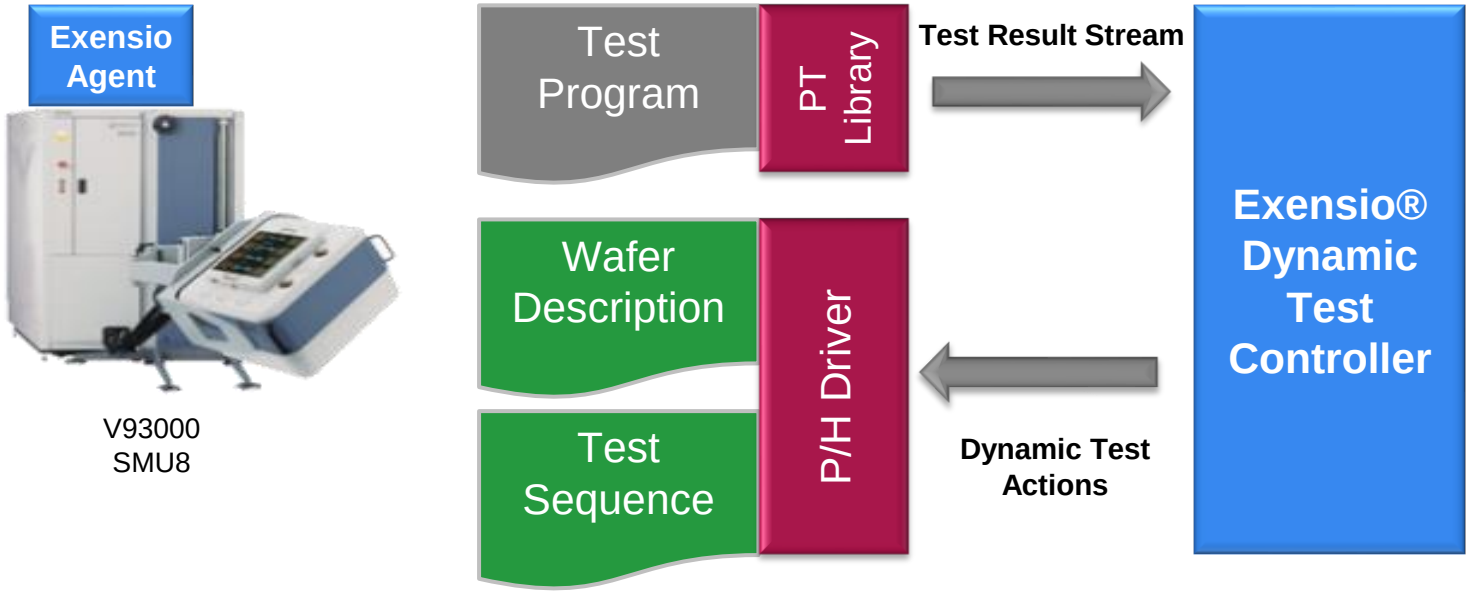
- A rose by any other name…E-Test, parametric test, wafer acceptance test (WAT)
- Primary objective: Discover root causes of device performance deviation
- Test structures in scribe lines between die on wafer
- Limited test of sites across wafer (e. g., 9 or 20 sites)
- Challenge – Minimize downtime, manual analysis when out-of-spec measurements detected



Bhushan M., Ketchen M.B. (2015) Electrical Tests and Characterization in Manufacturing. In: CMOS Test and Evaluation. Springer, New York, NY. https://doi.org/10.1007/978-1-4939-1349-7_7

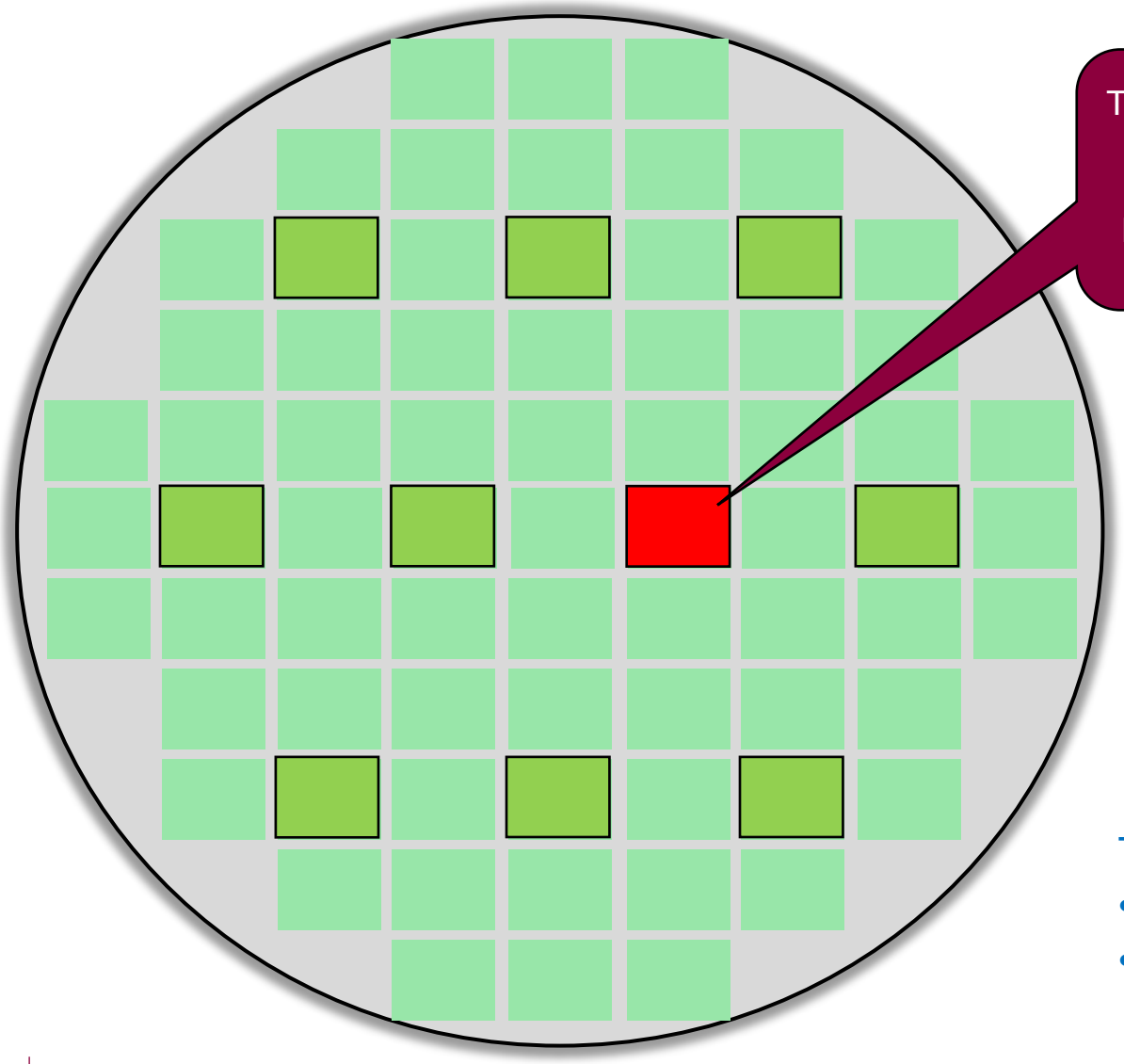
DPT: Dynamic Parametric Test

- Exensio® from PDF Solutions is a portfolio of data analytic & storage products are integrated with the Advantest V93000/SMU8 parametric tester and PDF Solutions Exensio®
- DPT provides a Rules Engine, programmed by the customer, to redirect the wafer flow (test locations, algorithm, test plan) within milliseconds of a qualifying parametric test data point
- The objective is to optimize test time and problem-solving instantly with minimal human interaction required



- Exensio Evaluates Rules
  - Modifies Test Flow
  - Adjusts Test Algorithms
- 93K Executes New Test Recipe

DPT Example: Diode Test, Measure V_D @ I_D = 100 nA



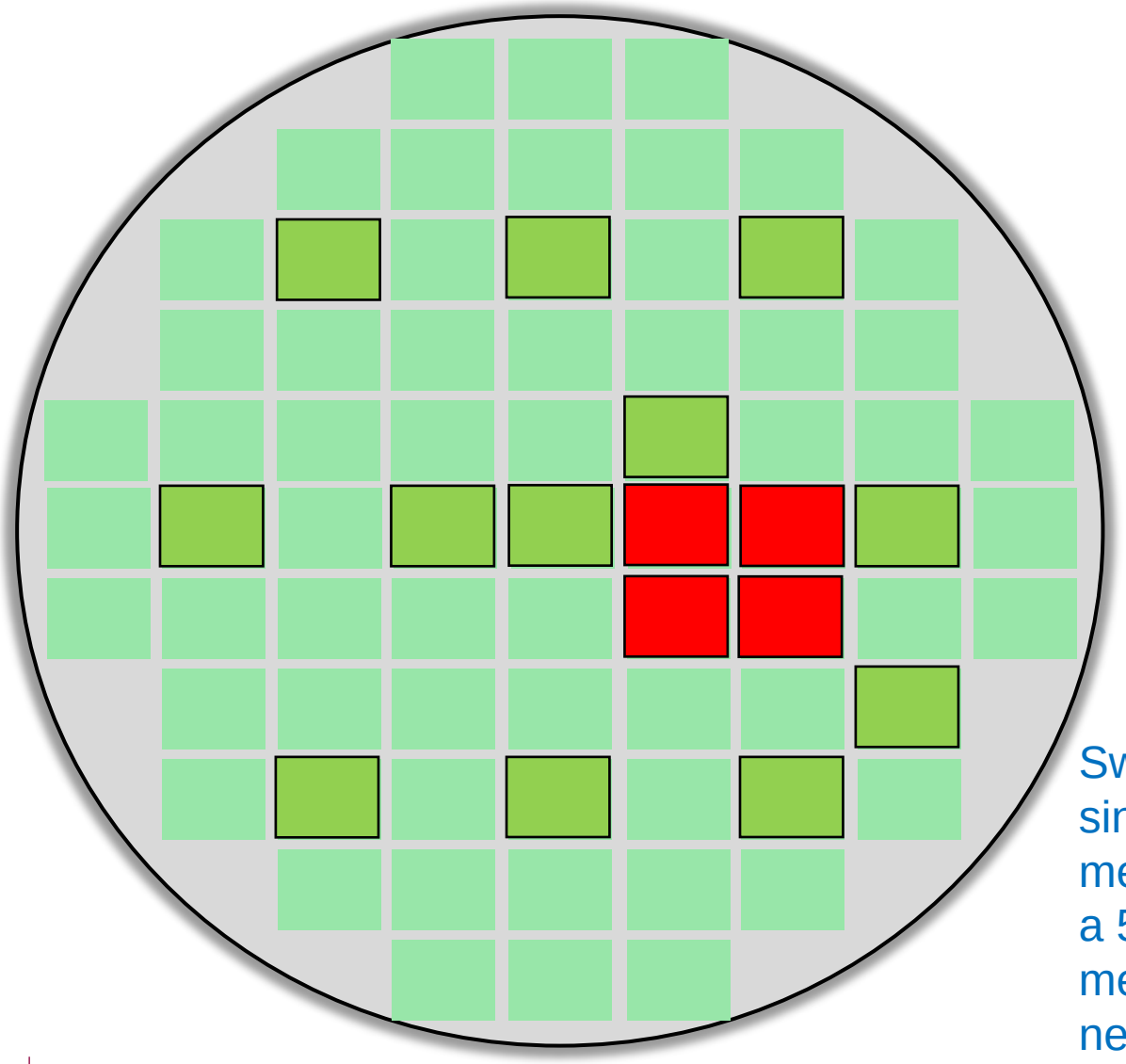
V93000 Data Stream contents during a wafer measurement

Die X-Y	Measure	Other Data
-2, 3,	0.642,	xxx,
0, 3,	0.643,	xxx,
2, 3,	0.644,	xxx,
-3, 0,	0.643,	xxx,
-1, 0,	0.644,	xxx,
1, 0,	0.638,	xxx,
3, 0,	0.643,	xxx,
-2, -3,	0.642,	xxx,
0, -3,	0.643,	xxx,
2, -3,	0.644,	xxx

The Rule & Adaptive Action could be based upon:

- Specs, wafer or lot statistics, process C_{pk} , . . .
- Adaptive Action from Rule trigger could happen instantly, at wafer-end, or lot-end

Adaptive Test Action: Change from Spot to Sweep



Switch from a single spot measurement to a 5-point sweep measurement on new locations

Original Spot Measurement Data

Die X-Y	Measure(Spot)
-2, 3,	0.642,
0, 3,	0.643,
2, 3,	0.644,
-3, 0,	0.643,
-1, 0,	0.644,
1, 0,	0.638,
3, 0,	0.643,
-2, -3,	0.642,
0, -3,	0.643,
2, -3,	0.644,

Root cause isolated as reticle/etch issue!

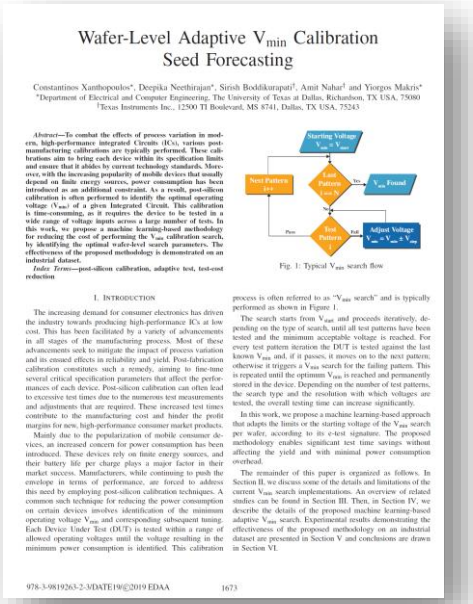
New Adaptive Test Flow

(new test algorithms & die locations)

Die X-Y	Measure(Sweep)
0, 0,	0.643, 0.584, 0.524, 465, 405,
1, 1,	0.642, 0.583, 0.523, 464, 405,
2, 0,	0.638, 0.578, 0.519, 0.459, 0.400,
2, -1,	0.639, 0.579, 0.520, 0.460, 0.401,
1, -1,	0.639, 0.580, 0.520, 0.461, 0.401,
3, -2,	0.642, 0.583, 0.524, 0.465, 0.405,

Adaptive Test and Real-Time Analytics During Test

- **Production test has traditionally been performed as “one size fits all” approach**
  - Inefficient use of valuable test resources, especially vis à vis natural material variation
- **A better approach is to adapt the test flow, contents, limits, etc., to the material at hand**
- **Example use cases**
  - Optimize looped tests which search for minimum voltage, maximum frequency, etc.
  - Use predictive analytics to optimize device tuning/trimming



Wafer-Level Adaptive V_{min} Calibration Seed Forecasting

Constantinos Xanthopoulos*, Deepika Neethirajan*, Sirish Boddikurapati†, Amit Nahar† and Yiorgos Makris*
*Department of Electrical and Computer Engineering, The University of Texas at Dallas, Richardson, TX, USA, 75080
†Texas Instruments Inc., 12500 TI Boulevard, MS 8741, Dallas, TX, USA, 75243

Fig. 1: Typical V_{min} search flow

I. Introduction

2019 DATE Conf.
V_{MIN} search limits prediction

Trim Time Reduction in Analog/RF ICs Based on Inter-Trim Correlation

V. A. Niranjan*, D. Neethirajan*, C. Xanthopoulos†, E. De La Rosa‡, C. Alleyne‡, S. Mier‡ and Y. Makris*
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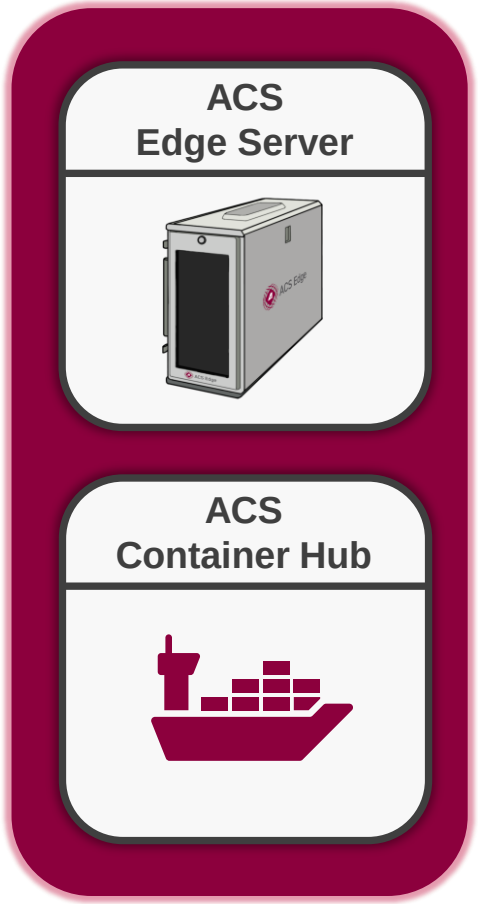
†Advantest America, 12301 Ruta Trace Pkwy, Austin, TX 78727, USA
‡Qualcomm Technologies Inc., 5775 Morehouse Dr., San Diego, CA 92121, USA

I. Introduction

2021 VLSI Test Symp.
Trim solution prediction

ACS Edge

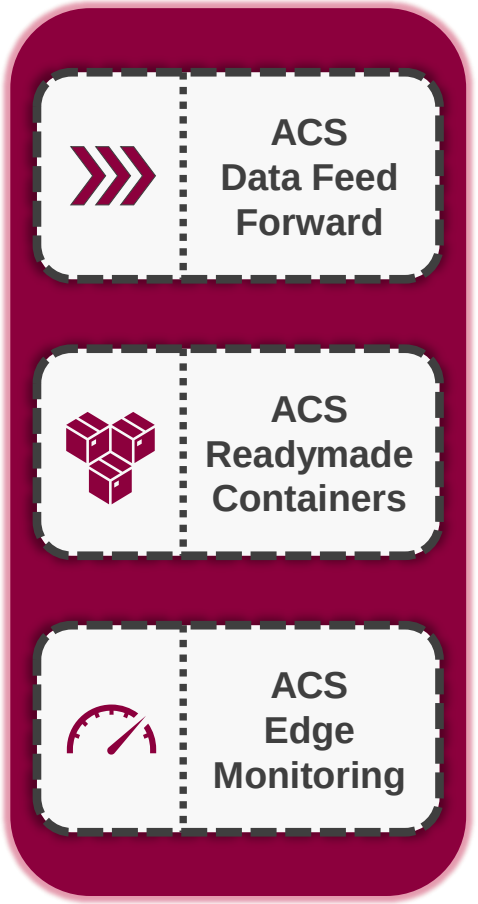
ACS Edge Core Product



A real-time, security-first, cloud connected high performance test cell compute solution

An industry-first, developer centric approach to secure deployment of algorithmic workloads in semiconductor test

ACS Edge Extensions*



Integrated Data Feed Forward/Backward, for complex data-science using other insertion data on demand.

Pre-built solutions, fully vetted and qualified for some of the most complex challenges in semiconductor test

Integrated monitoring of systems and workloads, to improve OEE and diagnose workloads

* Some extensions not available at launch

Success Stories from Two of the Top5 fabless companies

Large Fabless 1

- Large fabless complex digital SoC customer who uses ACS Edge for complex machine learning inferences for **dynamic retest**.
- TensorFlow 2.0 base ML container
- Initial validation & PoC on three-lab based systems in ~2 months
- Successful roll-out to Taiwan-based test house, loading large number of production systems ~6 months
- Initial cost savings estimate due to improved yield > $10's of M / year

Large Fabless 2

- Large fabless complex digital GPU customer who uses ACS Edge for complex machine learning inferences for **tiered binning**.
- PyTorch ML container
- GPU accelerated ACS Edge version (NVIDIA T4)
- Initial validation & PoC phase at Engineering Lab & NPI in Taiwan-based test house
- Customer is reliably able to bin additional premium bin & value tier without increase in CoT
- Production roll-out planned for late 2021

Other Challenges: Data Integration

Breaking down silos

To truly meet the need for end-to-end solutions, data must be integrated from widely varying sources

- Recent example: Prediction of burned wafer probe needles
- Multiple potential root causes – many places to look
- Data often siloed – challenging to tie together for a given product
- Electronic chip ID (ECID) commonplace for digital SoCs, but is non-standard, different for each company

Data origin	Types of data	What to look for
Wafer probe/test cell	• Maintenance records • Inspection • Probe test • Calibration • On-die parametrics • Z-travel and contact force • Thermal sensors • Alarms	• Timing of probe burn events • Calibration issues • Equipment issues • Warping of wafers, boards • Localized heating
Wafer fab	• Equipment • Inspection • In-line scribe test	• Misprocessing • Hot/cold material
Board shop	• Repair records • Board images	• Failing probe counts, locations
Design IT	• Chip layout • Power grid layout • Chip power sims/analysis • On-die sensors	• Low pin count power planes • Localized heating
Test IT	• Program content • Program release artifacts	• Stress test content • Current/power spikes • Incorrect limits/clamps

Conclusions

- Data creation, diversification growing at an exponential rate
  - Test plays a central role in harvesting IC data to feed the entire value chain
  - Chiplet-based products are among the most data-intensive
- Quality requirements increasing, especially in key sectors such as automotive
  - Drives need for advanced techniques to identify at-risk units
  - Machine learning use becoming commonplace at all phases in the product lifecycle
- IC supply chain is disaggregated → data still must be shared securely while protecting IP
- Our industry is responding with innovative solutions – it's an exciting time to work in data science

Acknowledgements

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- Vishnu Rajan
- Andreas Schmidt
- Thomas Zanon

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Thank you!

Questions?

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Thank you sponsors!

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Global Companies Rate Advantest THE BEST ATE Company 2021

Advantest receives highest ratings from customers in annual VLSIresearch Customer Satisfaction Survey for 2 consecutive years.

Global customers name Advantest THE BEST supplier of test equipment in 2020 and 2021, with highest ratings in categories of:

Technical Leadership – Partnership – Trust – Recommended Supplier – Field Service

"Year-after-year the company has delivered on its promise of technological excellence and it remains clear that Advantest keeps their customers' successes central to their strategy. Congratulations on celebrating 33 years of recognition for outstanding customer satisfaction."

— **Risto Puhakka**, President VLSIresearch


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